State-of-the-Art Verification of the Hard Driven GTO Inverter Development for a 100 MVA Intertie

P. K. Steimer, H. Grüning, J. Werninger  
R&D Drives and Power Electronics  
ABB Industrie AG  
CH-5300 Turgi, Switzerland

D. Schröder  
Institute of Electrical Drives  
Technical University Munich  
D-80333 München, Germany

Abstract - The 100 MVA intertie is mainly characterised by the following innovations:
− hard driven GTO (HD-GTO) with a new housing
− series connection of hard driven GTOs
− low-inductive high power HD-GTO inverter valve
− fuseless high power HD-GTO inverter.

The presented hard driven GTO technology allows the robust, reliable and cost-efficient series connection of GTOs. The concept of the 100 MVA intertie, which is based on the HD-GTO technology, is reviewed. The development of the high power HD-GTO inverter module according to a state-of-the-art development process is presented. With the use of a circuit simulator with accurate physical models of the power semiconductors, especially the concept phase, the development phase and the verification phase have been supported.

I. INTRODUCTION

Static frequency converters with high efficiency and state-of-the-art performance can be found today in a lot of applications up to a very high power level. The main applications can be found today in traction, industry, power transmission and power generation. Power electronics products and systems are still in a phase of continuous innovation. In the last decade, a strong technology push was initiated by the GTO technology. In the inverter module the GTO technology asked for a special environment for the semiconductor, like:
− low inductance dv/dt snubbers
− di/dt snubbers
− low inductance DC-link
− reliable GTO drivers (gate units)

The switching frequencies of the GTOs was typically limited due to device and snubber losses to a maximum value of about 300 to 500 Hz.

But regardless of these additional demands, limitations and costs, the GTO technology has found its interesting applications. In a first phase the main applications with a maximum power up to 10-20 MVA were within:
− adjustable speed drives (traction, industry)
− railway interties (3-phase 50Hz/1-phase 16⅔/3 Hz).

In a second phase GTO applications in the power transmission and power generation market with an even higher power level are getting attractive for:
− railway interties
− static VAR compensators
− energy storage systems
− variable speed power generation and
− other FACTS applications

To reach the needed converter ratings of 50-100 MVA a high number of GTOs must be installed. To meet the cost and the reliability requirements of this applications a robust, cost efficient series connection of GTOs is needed.

The concept of the hard driven GTO (HD-GTO), which inherently allows the robust series connection of semiconductors, will be the key innovation and technology for this future applications and markets [1].

II. THE TECHNICAL CONCEPT OF THE 100 MVA INTERTIE

In spring 1994, ABB Industrie AG received the order for an installation of a 100 MVA back-to-back intertie between the 3-phase 50 Hz grid and the one-phase 16⅔/3 Hz railway grid in Germany. ABB was seen by the customer as the clear leader in high power GTO inverter technology. For the first time the series connection of high power GTOs based on the concept of the hard driven GTO (HD-GTO) was offered by ABB. This concept was well received due to its simple and robust solution of the series connection of GTOs. The installation will be handed over to the customer in the autumn 1996.

The technical concept of the railway intertie based on a VSC (Voltage Source converter) has already been applied and is in continues operation for two 20 MVA frequency converters with the Swiss Federal Railway (SBB). The installations at Giubiasco are based on conventional GTO technology without series connection.
For the 100 MVA Intertie the following technological innovations have been added:
- hard driven GTO (HD-GTO) with a new low-inductive housing
- series connection of up to six hard driven GTOs
- low-inductive high power HD-GTO inverter valve
- fuseless high power HD-GTO inverter.

To fulfil the requirements of the customer the following technical concept for the frequency converters (fig. 1) based on a VSC has been chosen:
- The converter on the 3-phase 50 Hz side is based on a conventional anti-parallel 12-pulse thyristor bridge
- In combination with harmonic filters the 50 Hz line impact is minimised to the specified levels.
- The thyristor converter feeds directly into a 10 kV DC-link, which is equipped with an additional 33\(\frac{1}{3}\) Hz filter for the elimination of the power fluctuations generated by the one-phase 16\(\frac{2}{3}\) Hz grid
- The GTO inverter on the railway side consists of 288 hard driven GTOs arranged in 24 fuseless phase modules in a Ns = 4+2 design. Two-phase modules are feeding into a double-fed transformer winding. The twelve windings of the railway side transformers are used to build a 25-level inverter. This multi-level concept allows the filterless operation of the railway side GTO inverter.

Especially in the High Power Inverter Module for the 100 MVA intertie a high degree of innovation was included (hard driven GTO, series connection, new low-inductive design). New methods for the verification of the development already in an early design phase have therefore been investigated.

### III. The Hard Driven GTO

The key innovation of the 100 MVA intertie, the hard driven GTO (HD-GTO) is shown in fig. 2. In Table 1 a comparison of the HD-GTO with a standard GTO can be found. In regards of the high power applications the following points are of high interests
- the storage time of the HD-GTO is reduced to 1 \(\mu\)s
- the dv/dt-snubber and the inverter losses can be considerably reduced due to the completely homogenous operation of the HD-GTO.

the gate-drive power is considerably reduced due to the lower gate turn-off charge.
### Table 1: Comparison between GTO and HD-GTO

<table>
<thead>
<tr>
<th></th>
<th>GTO</th>
<th>HD-GTO</th>
</tr>
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<tbody>
<tr>
<td>Turn-on di/dt (A/µs)</td>
<td>500</td>
<td>3000</td>
</tr>
<tr>
<td>Turn-on energy E&lt;sub&gt;on&lt;/sub&gt; (Ws)</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>Turn-off energy E&lt;sub&gt;off&lt;/sub&gt; (Ws)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>snubber cap. C&lt;sub&gt;s&lt;/sub&gt; (3 kA)</td>
<td>6 µF</td>
<td>1 to 3 µF</td>
</tr>
<tr>
<td>Max turn-off current I&lt;sub&gt;TGQM&lt;/sub&gt; (kA)</td>
<td>3</td>
<td>3 to 6 kA</td>
</tr>
<tr>
<td>Gate drive power (500 Hz)</td>
<td>80 W</td>
<td>30 W</td>
</tr>
<tr>
<td>gate stored charge Q&lt;sub&gt;eq&lt;/sub&gt; (µC)</td>
<td>8000</td>
<td>2000</td>
</tr>
<tr>
<td>Max. turn-off dv/dt (V/µs)</td>
<td>500</td>
<td>1500</td>
</tr>
<tr>
<td>Storage time t&lt;sub&gt;s&lt;/sub&gt; (µs)</td>
<td>20</td>
<td>1</td>
</tr>
</tbody>
</table>

**Figure 2:** Hard driven GTO (HD-GTO) with gate drive

**Figure 3:** Turn off of a hard driven GTO (4.5 kV/3 kA) with a -15V gate drive, C<sub>s</sub> = 3 µF

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### IV. The Physical Models for Power Semiconductors

If circuit simulation of power electronics is considered, there are different proposals for the models of the components. Especially there is a wide range of models for the power semiconductors. On the one hand Spice-models are often proposed because these models can run on a PC and the duration of the simulation of power electronic circuits is short. However, there is one essential drawback: the switching behaviour of the power semiconductors neglects the influence of the low doped zone(s) with normally high level injection, which is one of the main characteristics of the power semiconductor. These Spice-models are based on pure signal processing devices and these components do not include low doped zone(s) [2], [3]. Therefore these Spice-models cannot be used to design power electronic topologies.

Due to this disadvantage the original Spice-models had been expanded to show such principle effects like the reverse recovery. But in these expanded Spice-models the interesting effects are normally implemented in the original Spice-models with additional electronic circuits to mimic the desired effect. Therefore the desired effect is only imitated in a generally narrow operating point. Consequently such solutions are not very well suited for a general circuit simulation with different power semiconductor topologies and in a very wide operating range of the power semiconductors.

Another quite different approach is the device simulation (one-, two- and three-dimensional for each power semiconductor). This approach shows the behaviour of power semiconductors in each detail, which result from the four coupled equations (transcendent differential equations):

- **Poisson’s equation:**
  \[ \nabla D = \rho(x,y,z) \]

- **Current density equations:**
  \[
  J_n = q \cdot \mu_n \cdot E \cdot n + q \cdot D_n \cdot \nabla n \\
  J_p = q \cdot \mu_p \cdot E \cdot p - q \cdot D_p \cdot \nabla p
  \]

- **Continuity equations:**
  \[
  \frac{\partial n}{\partial t} = -R_n + \frac{1}{q} \cdot \nabla J_n \\
  \frac{\partial p}{\partial t} = -R_p + \frac{1}{q} \cdot \nabla J_p
  \]

Additionally we have to consider the ambipolar differential equation (ADE), which is necessary to describe the charging and discharging in the intrinsic or low doped zone.

This equation arises from the elimination of the electric field \( E \) with \( p = n \) in the current equations and the insertion of the resulting ambipolar current density equation for \( J_p \) into the continuity equation for \( p \).
\[
\frac{\delta p}{\delta t} = \frac{\delta D}{\delta x} \frac{\delta p}{\delta x} - D \frac{\delta^2 p}{\delta x^2} + \frac{1}{q} \frac{1}{(b+1)} \frac{\delta b}{\delta x} - R
\]

\[ b = \frac{\mu_n}{\mu_p} : \text{mobility ratio} \]

\[ D = \frac{2 \cdot \mu_n \cdot \mu_p}{\mu_n + \mu_p} : \text{ambipolar diffusivity} \]

\[ R = \frac{p}{\tau_h} + C_A \cdot p^3 : \text{composite recombination rate} \]

Since \( D, b, \tau_{SRH} \) are functions of the local carrier density, the local dopant density and other local parameters, these quantities are also functions of space.

However such simulations are complex, need a powerful computer and are CPU-time consuming; furthermore the number of power semiconductors during one simulation is limited. Due to these results a special solution for the modelling of power semiconductors - the physical modelling - was used for all power semiconductors as for example the main switches like the GTO (or IGBT or MOSFET), the freewheeling and snubber diode.

Physical models start from the geometric structure of the power semiconductors considered, use the semiconductor equations above to cover all physical effects and use the parameters like the geometric data or the doping profiles. But the semiconductor equations result in a set of transcendent equations, which cannot be solved directly. The second decision in the development of physical models was to accept a one-dimensional geometric approach. This decision is especially acceptable for hard driven semiconductors in a very wide range of operating points and applications. But even if only a one-dimensional approach is used, the set of equations remain transcendent.

The third decision in the process of the modelling depends on the desired accuracy of the simulation especially during the switching transients. It is well known that the low doped zones normally reach the high injection level during the on-state. Due to this effect, the ambipolar diffusion equation is solved very precisely with a specific approach for example in the developed models.

In fig. 4 the structure of the model of the power diode and in fig. 5 the GTO structure is shown. The structure of the diode in fig. 4 has only one low doped zone, but the GTO has a low doped p- and n-base. In these low doped zones the ambipolar equation is solved like in device simulation programs by a segmentation of the zone which is time- and position-variant; so with a limited number of segmentations a result with high accuracy is achieved for the low doped zone. The high doped zones are approximated by more simple concentrated models \[4, 5\]. Due to this approach these physical models cover a very wide range of operating points and applications.

These advantageous features of the physical models for power semiconductors, which were developed at the Technical University of Munich, enable the research and development in the industry to use simulation instead of only hardware experiments. For the later verification of the high power GTO inverter development the fitting of the one-dimensional model for the hard driven GTO to the used GTO device was essential. For this work basic dynamic measurements, if possible at different temperature, are fundamental for the fitting process. Additionally basic information like geometry, doping profiles, carrier lifetime profiles from the GTO or diode manufacturer are important. An example of this basic fitting process for a hard driven GTO can be found in fig. 6.

In fig. 6 comparisons of experimental results and simulations at the same temperature and operating point is shown. It can be seen that the experimental result and the simulation have a close correlation. This is an excellent result.

The models had been validated by simulating different topologies like choppers with different snubber, choppers using the active semiconductor as ZVS or ZCS and in a temperature range from 400 K - 100 K, comparing the simulations and the experimental results. Therefore the user can rely on the result of the simulation.
Figure 6:
Comparison of the measurement and the simulation of the HD-GTO turn-off at 25°C and 125°C

This is a chance for the user of these models to simulate unknown topologies or to extend the known topologies into new operating areas. The additional advantage of this procedure is that not measurable signals can be simulated easily, the interdependency of different components or parasitics can be discussed. The same holds true for different sets of parameters of the components. This gives an opportunity to understand the topology much better and optimise it by simulation. The result is a reduction of practical experiments, the risk and the cost.

V. **THE DEVELOPMENT AND VERIFICATION OF THE HIGH POWER INVERTER**

The key technology of the high power HD-GTO inverter for the 100 MVA intertie, the cost-efficient and robust series connection of GTOs, has been prepared by ABB in the early 90s by means of a technology development. A pre-prototype valve with four series connected HD-GTOs was developed and tested at full voltage and current in the power lab (fig. 7). Due to this technology development ABB was able to show in December 1993 the concept of the new high power HD-GTO inverter to potential customers.
For the 100 MVA Intertie the product development of a high power HD-GTO inverter with six series connected 4.5 kV/3kA hard driven GTOs was needed (fig.8). For the product development a development process according to the best practices with predefined phases was followed (concept, specification, development and prototype, verification).

For product development projects a good concept phase is important. Especially in this phase simulation tools are of high importance. In the 100 MVA intertie project a circuit simulator with accurate semiconductor models was used for the first time. This tool was on the one hand used for the further optimisation and the power upgrading of the existing pre-prototype inverter module to the requirements of the 100 MVA intertie. On the other hand the digital circuit simulator was used for the concept definition of the connection of up to 24 high power inverter modules at the same DC-link. Due to the first use of the hard drive special attention was given to the event of pre-flooded freewheeling or snubber diodes. It could be shown that in the case of the switching of a neighbour inverter a current of up to 35 A could exist in the snubber diodes of the di/dt-snubber. In combination with a hard turn-on of a hard driven GTO a possible device failure could be expected. As possible countermeasures the following points were investigated:

- reduction of the turn-on di/dt of the HD-GTO
- RC-snubber on the snubber diodes

This investigations resulted in the adding of one RC-snubber over the diodes of the di/dt-snubber (fig. 9), on the reduction of the turn-on di/dt of the HD-GTO (500 A/µs) and in the definition of the optimum DC-link topology.

The development of the high power inverter module was checked by means of an intensive prototype test program including the following important steps:

- test of pre-flooding of snubber diodes
- high frequency operation in fault cases
- surge current test on GTO
- surge current tests on inverter modules
- type-test including electrical and thermal verifications (fig. 10)
- operational tests with no redundancy (Ns = 4+0)
- EMC-tests
The prototype tests were supported by the digital circuit simulator with accurate power semiconductor models. A complete simulation of the HD-GTO high power inverter was prepared. This simulation model of the inverter was fitted during the prototype measurements by defining and adjusting all the important stray reactances of the valve. This digital circuit simulator was used for the following verification tasks:

- verification of the electrical and thermal design of non-measurable quantities, like for example the current of the snubber diodes
- check of the influence of device tolerances including passive components.

In Fig. 11 an example of a worst case simulation by means of the digital circuit simulator is presented. This simulation was used to check the maximum allowable DC-Link voltage of the high power inverter. As worst conditions the following was assumed:

- maximum DC-link voltage of 12 kV (+20%) 
- maximum storage time difference of the GTOs of 400 ns
- Max. tolerance of the snubber capacitors of ± 5%.

Figure 11: Maximum dynamic GTO voltage in worst case condition

As can be seen the maximum dynamic GTO voltage is in this simulated worst case condition below the limit of 4500 V (fig. 11).

VI. THE FIRST INSTALLATION OF THE HIGH POWER INVERTERS

After completing the verification of the high power inverter modules the release for production was given. Each of the 288 GTOs for the high power inverters did go through the incoming inspection in combination with the corresponding gate unit. One single failure was encountered. Each of 24 high power inverter modules for the 100 MVA installation did complete successfully its routine test including a 3 hours operational test at full voltage, current and 150 % of the nominal switching frequency.

VII. CONCLUSION

The hard driven GTO is the key technology for the series connection of high power GTOs. The hard driven GTO works during turn-off very homogenous and the device can be stressed up to the physical limits of silicon. This homogenous operation allows the use of a state-of-the-art device and inverter simulation based on physical models of the semiconductors. The use of these tools already in an early design phase reduces the risks and the time-to-market. The development process, supported by modern simulation tools, will allow to follow quickly the expected further improvements in the hard driven GTO device and inverter technology especially in direction of lower costs per MVA, lower losses, higher switching frequencies and higher inverter efficiency [6]. These further improvements will have considerable impact on the performance and economy of converters with series connected GTOs as needed in future FACTS applications.

REFERENCES


