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Surge Arrester based Load Commutation Switch for Hybrid HVDC breaker and MV DC breaker

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Abstract

In this paper, the switching behavior of a combination of series and parallel connected IGBTs with a parallel metal oxide (MO) surge arrester is investigated. This configuration is for use in medium and high voltage DC-breaker applications. The focus of this paper is on the application and operation of an auxiliary power electronic switch, referred to as the load commutation switch (LCS), for the hybrid HVDC breaker (HHB). The switching behavior of a state of the art SPT+ IGBT is compared to the switching behavior of the Bi-Mode Insulated Gate Transistor (BIGT). In addition design aspects of the LCS are discussed.

1 Introduction

HVDC breaker are coming more and more important in the context of multipole dc-grids in Europe and China. In this context, the hybrid HVDC breaker (HHB) is a promising solution [1]; [2]. Fig. 1 shows the schematic of the hybrid HVDC breaker. It consists of an ultra-fast (mechanical) disconnector (UFD), the LCS and the main breaker (MB). The current flow during normal operation is shown in Fig. 1. Fig. 2 shows the current after turn-off of LCS and the UFD. The current is turned off by the MB in the end.

As shown in Fig. 1 the LCS and MB have to be bi-directional. With the use of an RC-IGBT as introduced in [1], referred to as the Bi-Mode-Insulated-Gate-Bipolar-Transistor (BIGT), there is no need of discrete diodes as known from standard modules. With this, the silicon area of the entire breaker (LCS and MB) can be reduced by a factor of two by applying the BIGT compared to the standard diode and IGBT approach. This is a huge advantage when it comes to footprint and space requirements.

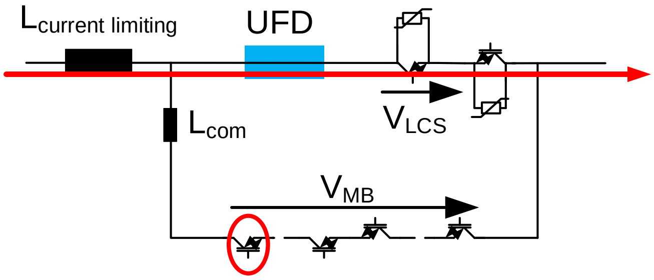

Fig. 1: Current flow during normal operation

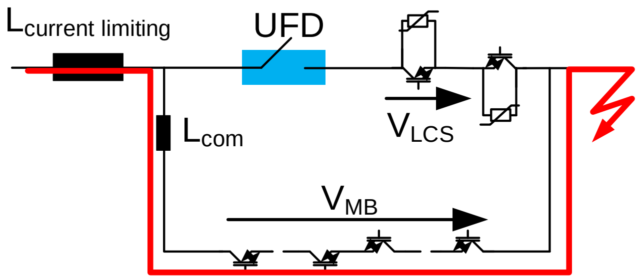

Fig. 2: Current flow after commutation

In the following, the design of a MO surge arrester based LCS for the HHB will be discussed. The switching behavior of an IGBT with a parallel connected MO surge arrester has already been investigated in [5]. Hence, this paper will focus on system design aspects and switching behavior of parallel and series connected BIGT and state of the art SPT+-IGBT with parallel connected MO surge arresters.

In addition, the influence of the chosen MO surge arrester voltage on the switching behavior is also investigated.

2 General principle of operation

Fig. 3: shows a simplified MO surge arrester current and voltage waveform during turn-off of the LCS. The current commutates into the arrester branch by turning off the semiconductor. The inductance L in the arrester loop is neglected and therefore the voltage overshoot at t_1 is not shown.

As this voltage peak is strongly dependent to the semiconductor characteristics, gate drive and stray inductance from arrester to semiconductor, it is directly related to the mechanical design. This has to be taken into account during the design phase to guarantee sufficient margin to the maximum semiconductor voltage.

Important time instances include the following:

$t=t_1$: commutation of current from IGBT to arrester is completed. Full current is flowing in the arrester.

$t=t_2$: commutation from LCS to main breaker is completed. Full current is flowing in MB. Only residual current of arrester (<1A) is flowing in fast mechanical disconnector – LCS branch. Operation of mechanical disconnector can be initiated.

$t=t_3$: Mechanical disconnector operation not completed. LCS has to block the MB on-state voltage.

$t>t_4$: Mechanical disconnector operation completed. Mechanical disconnector takes up voltage.

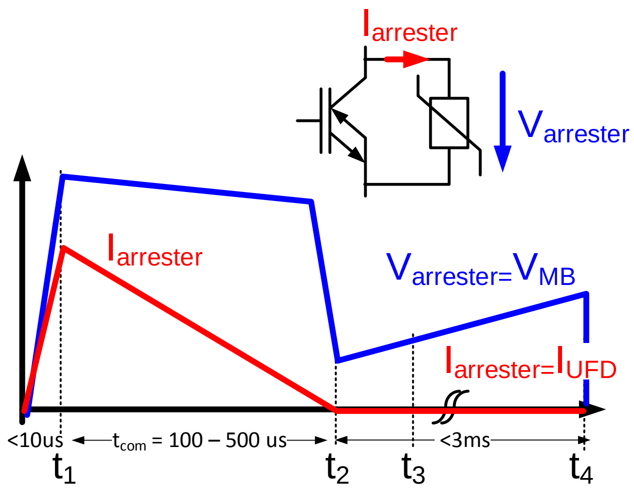

Fig. 3: Arrester voltage and current

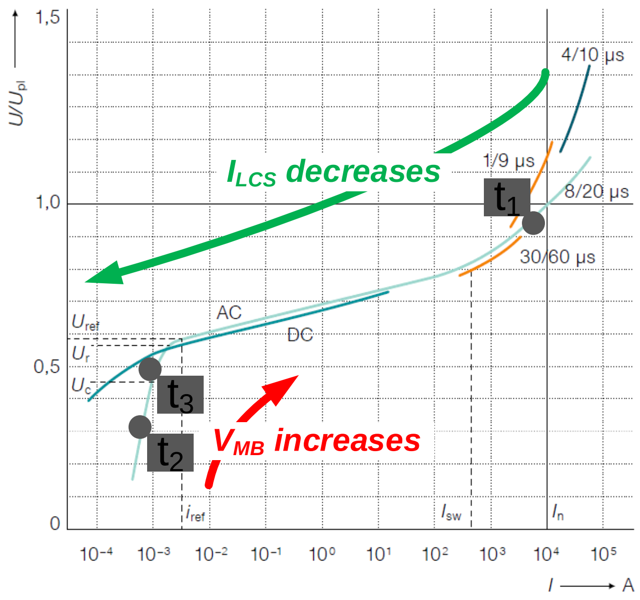

Fig. 4: Voltage vs. current characteristic of MO surge arrester

Fig. 4 shows a typical V-I characteristic of a MO surge arrester. As it can be seen from Fig. 3 the LCS is is decrease by the arrester voltage. This voltage has to be high enough to enable fast commutation but also below the semiconductor voltage rating. After commutation, the UFD requires time to open, hence the LCS has to block the on-state voltage of the MB for a few milliseconds. As the UFD can only handle a few ampere, the arrester current between t_5 and t_6 has to be kept in the range of a few 100mA per paralleled branch. If the number of arresters is chosen bo be too small for static blocking, the current may commutate back to the LCS before the UFD opens or the UFD is damaged due to a too high current. In Figure 5, an example of this situation can be observed. With only 2 arresters in series the current starts to commutate back at around 2.5 ms due to a too high main breaker voltage. Increasing the number of arresters to 3 leads to a stable commutation in this example.

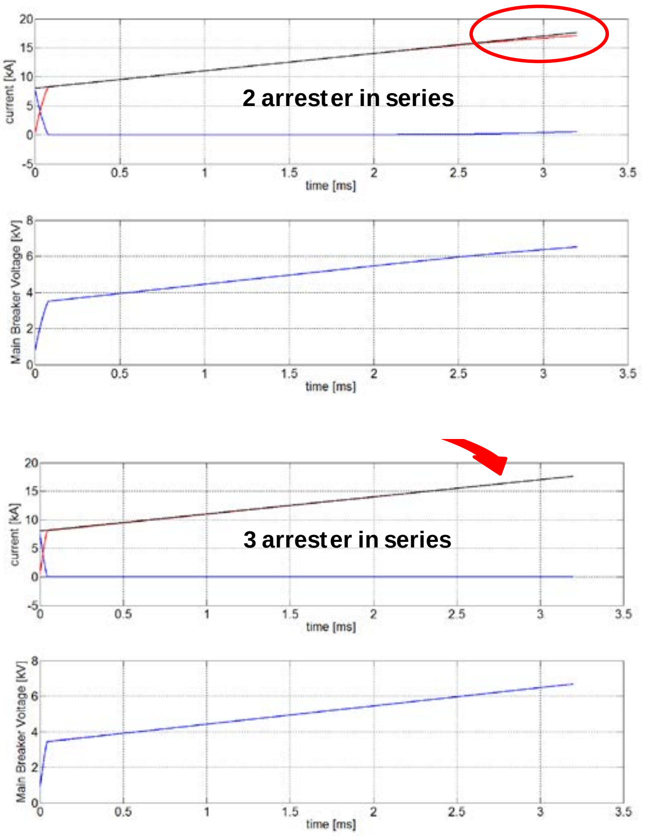

Fig. 5. Influence of number of arresters for “static” blocking. Top: 2 arresters in series / bottom: 3 arresters in series

3 Switching behavior

3.1 Influence of the arrester voltage on tur-off behavior

In this section, the switching behavior of a semiconductor with a parallel connected MO surge arrester for different residual voltages of the MO surge arrester will be discussed. In addition, the switching behavior of a state of the art SPT+ IGBT and a BIGT with parallel connected MO surge arresters will be compared.

Figure 6 shows the turn-off waveform of a 4.5kV SPT+ IGBT with a parallel connected MO surge arrester with different residual voltages. For the MO surge arrester with a residual voltage of 2.8 kV at 2kA the turn-off is very soft due to a large tail current. Compared to that with a residual voltage of the MO surge arrester of 4.1kV at 2kA the current snaps-off due to the fact that the electric field permeates the field stop layer of the SPT+ IGBT.

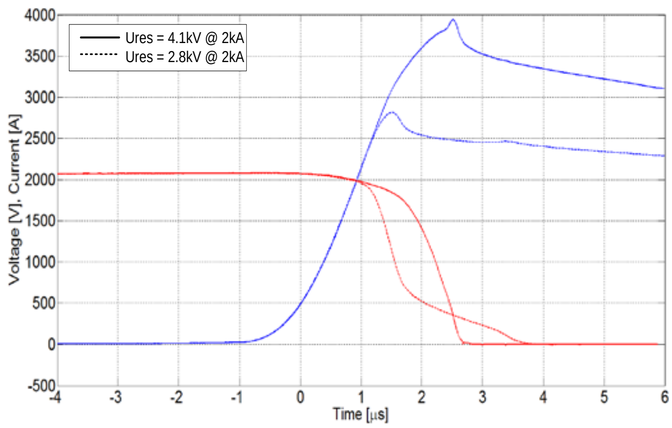

Fig. 6. Turn-off of a 4.5kV SPT+ IGBT with different arresters

3.2 Comparison between standard IGBT and BIGT

In Figure 7 the turn-off switching waveforms for 1kA and 2kA of the 4.5kV SPT+ IGBT can be seen. Figure 8 shows the turn-off switching waveform for 2kA and 4kA across the BIGT. As the BIGT has twice the number of chips as the IGBT (due to the integration of Diode and BIGT into one chip), the turn-off current per chip is the same for IGBT and BIGT when the turn-off current of the BIGT is double the turn-off current of the IGBT. A general discussion about the switching behavior of the IGBT with paralleled arresters can be found in [5]. Hence, in this paper the focus is on the difference between the IGBT and the BIGT and the influence of the MO surge arrester residual voltage. As it can be seen from Figure 7 the SPT+ IGBT shows a snap-off even at half of nominal current. This is due to the high arrester clamping voltage, which causes the electric field to penetrate the field stop layer. It can be seen in Figure 8 that the turn-off behavior of the BIGT is much softer compared to the conventional SPT+ IGBT. The BIGT exhibits a soft turn-off behavior in IGBT-mode. This is due to its dynamic avalanche, which limits the dv_{CE}/dt and the electric field in the device. As it can be seen from the waveform in Fig. 7 and Fig. 8 the collector-emitter voltage where the dynamic avalanche starts (change in dv_{CE}/dt) is much lower with the BIGT. The reason for this is an inhomogeneous current distribution inside the BIGT. This causes a higher hole density in regions with higher current and consequently a higher gradient of the electric field [3].

The benefit of the softer turn-off behavior is that the BIGT can be used with MO surge arrester with higher residual voltage compared to a conventional SPT+ IGBT. This will typically reduce the number of series connected devices compared to a solution with and SPT+ IGBT.

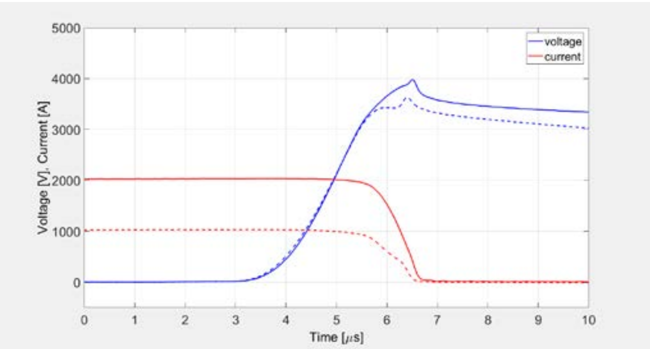

Fig. 7. Turn-off waveforms of a 4.5kV SPT+ IGBT

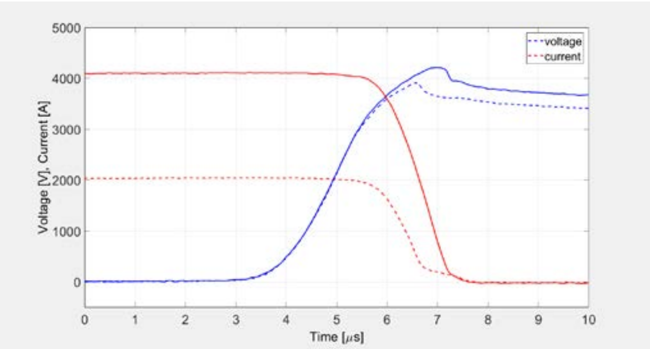

Fig. 8. Turn-off waveforms of a 4.5kV BIGT

4 Switching behavior in series and parallel connections

4.1 Series Connection

As the residual voltage of a MO surge arrester is in the range of ±5% of the nominal value, the series connection of MO surge arresters is not critical in terms of overvoltage protection of series connected semiconductors. In worst case conditions the voltage difference is 10%.

As the residual voltage of the MO surge arrester is chosen in a range far below the maximum blocking voltage and the switching losses of the semiconductor are negligible, the series connection of semiconductors with a parallel connected surge arrester for each position is uncritical in the application of a load commutation switch in the HHB.

4.2 Parallel connection

In contrast to a series connection of surge arresters, connecting them in parallel is a known problem due to the high nonlinearity of the arresters. With a nonlinearity coefficient of $\alpha \approx 30$ in the region of switching current impulses on the voltage-current characteristic, a difference of 5 % in the residual voltage would lead to a current sharing ratio of 1:4 between the surge arresters. Therefore, it is absolutely necessary to perform a current sharing measurement on all MO arresters that are intended to work in parallel. The manufacturer has to be informed when the order is made if the user intends to connect MO arresters in parallel. [8]. As a consequence it is very important from an application standpoint to carefully investigate the semiconductor behavior with parallel connected MO surge arresters and matrix (parallel and series) connection as in the LCS.

In Fig. 9 the parallel connection of BIGT with a MO surge arrester is shown. The turn-off waveforms for this configuration are shown in Fig. 10. Observe that the different residual voltages of the MO semiconductors results in a difference in the voltages during turn-off and after. The difference in voltages will cause a commutation of the current from one branch to the other dependent on the difference in residual voltage and the size of the inductances between the paralleled branches $L_{\sigma1}$ and $L_{\sigma2}$ in Fig. 9.

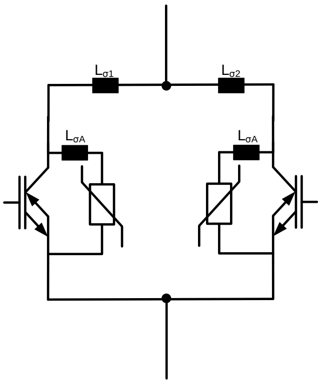

Fig. 9: parallel connection of two arresters

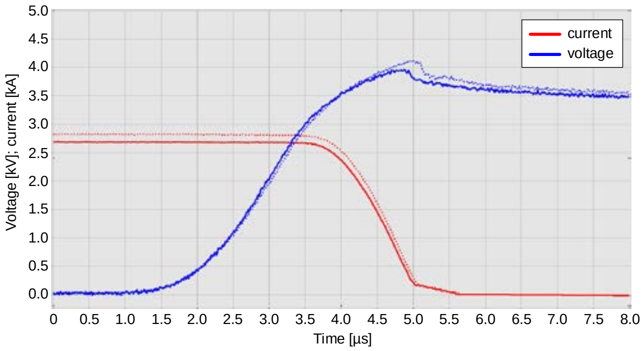

Fig. 10: turn-off waveform of two parallel connected IGBT with individual MO surge arrester in parallel

For the tests shown in Fig. 10 the current distribution between the two parallel branches is less than 10%. This was realized by optimizing the mechanical setup to equalize the inductance $L_{\sigma1}$ and $L_{\sigma2}$ as much as possible.

4.3 Matrix connection

In the case of several parallel branches in the LCS the design of the matrix connection of semiconductors with a paralleled surge arrester has to be solved with caution. The first possible option of the arrester placement is shown in Fig. 11. In this case no paralleling of arresters is necessary. The disadvantage of this solution is the complex mechanical design in case several parallel branches have to be connected. In addition to that, the stray inductance $L_{\sigma Ai}$, between semiconductor and MO surge arrester will be quite high and increases with the number of paralleled semiconductors. Furthermore, the setup does not scale well in terms of current capability.

In contrast Fig. 12 shows a concept where several surge arresters have to be connected in parallel. The advantage of this solution is that the surge arrester can be placed very close to the semiconductor, and hence a very low stray inductance $L_{\sigma A}$ can be achieved. One major disadvantage of the solution shown in Fig. 12 is that a derating of the MO surge arrester has to be done which results in an over-dimensioning of the individual MO surge arrester. The current misdistribution due to different voltage characteristic can be reduced by inductances $L_{\sigma i}$, decoupling the parallel branch from each other.

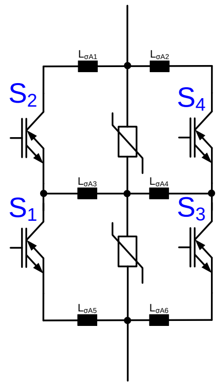

Fig. 11: only series arrester connection

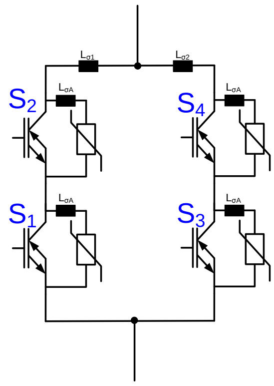

Fig. 12: series and parallel connection of arrester

In Fig. 13 the turn-off behavior of the configuration in Fig. 12 can be observed. As shown before the current misdistribution is below 10%. Due to the differences in the residual voltages of the MO surge arresters, the overshoot and the voltage after commutation are different for the 4 semiconductors. However these differences are not critical for the semiconductors.

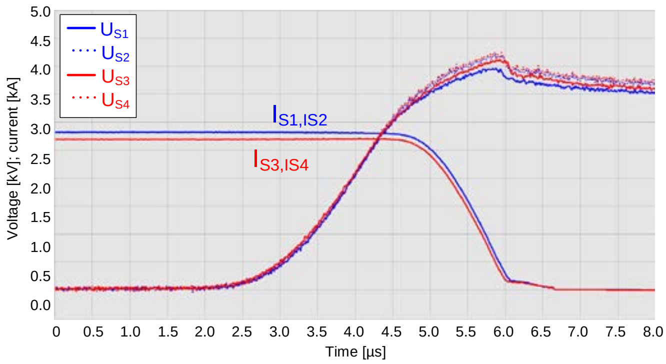

Fig. 13: turn-off waveforms of 4 semiconductors with paralleled surge arrester as in Fig. 12.

5 Summary

In this paper a MO surge arrester based Load Commutation Switch for the application in a Hybrid HVDC breaker has been presented.

The advantages of the BIGT over a conventional IGBT/Diode module were shown to be larger silicon area due to the integration of IGBT and diode and a softer turn-off behavior. This has been evaluated by calculations and measurements.

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