3300V HiPak2 modules with Enhanced Trench (TSPT+) IGBTs and Field Charge Extraction Diodes rated up to 1800A

Chiara Corvasce, Maxi Andenna, Sven Matthias, Liutauras Storasta, Arnost Kopta, Munaf Rahimo, Luca De-Michielis, Silvan Geissmann, Raffael Schnell
ABB Switzerland Ltd. Semiconductors, Fabrikstrasse 3, 5600 Lenzburg, Switzerland
e-mail: chiara.corvasce@ch.abb.com

Abstract

In this paper, we introduce the new generation 3300V HiPak2 IGBT module (130x190)mm employing the recently developed TSPT+ IGBT with Enhanced Trench MOS technology and Field Charge Extraction (FCE) diode. The new chip-set enables IGBT modules with improved electrical performance in terms of low losses, good controllability, high robustness and soft diode recovery. Due to the lower losses and the excellent SOA, the current rating of the 3300V HiPak2 module can be increased from 1500A for the current SPT+ generation to 1800A for the new TSPT+ version.

1. Introduction

Over the past two decades, the IGBT and antiparallel diode have experienced important performance breakthroughs due to improved device processes and design concepts. Nevertheless, further development work has shown the potential to achieve higher power densities, improved controllability and robustness. The trend for lowering the on-state losses of IGBTs has remained one of the main goals of this device concept development. After the introduction of the Field Stop (FS) / Soft-Punch-Through (SPT) buffer structures for providing thinner structures for low losses, the focus in recent years has shifted primarily towards further improvements on the MOS cell design with important steps made on both Planar and Trench cell concepts [1].

The fast diode also underwent similar developments to match the IGBT capabilities through new anode and buffer designs combined with optimized lifetime control for achieving low losses, soft recovery and high SOA capability.

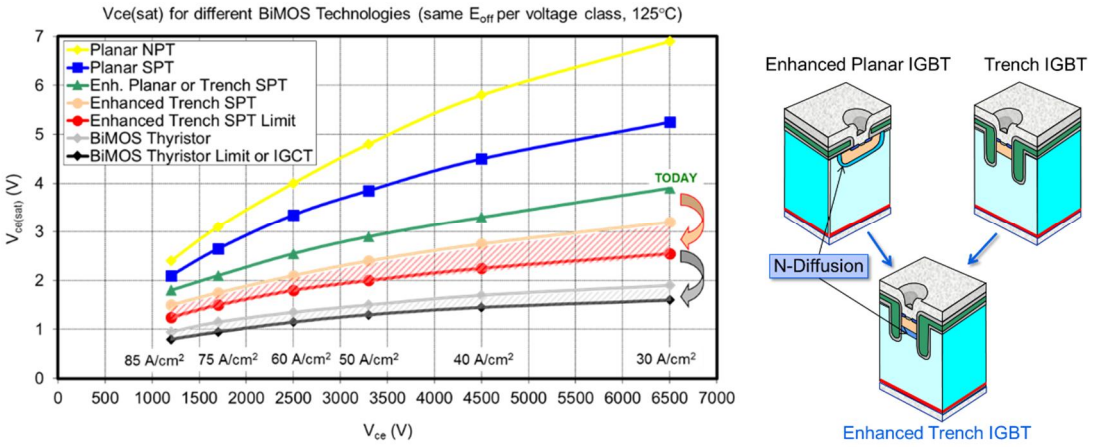

Fig. 1. IGBT technologies and impact on on-state losses for different voltage ratings.

Figure 1 shows an estimation of the on-state V_{ce_sat} loss reductions per voltage class with each generation of IGBT technology. For high voltage devices (>2kV), Enhanced Planar (EP) IGBT or Trench IGBT MOS cell concepts are employed on SPT structures demonstrating similar power ratings and loss performance. Nevertheless, for lower voltage devices (<2kV), the Enhanced Trench MOS cell employing an n-enhancement layer in the active trench region is already an established technology [2]. It is important to point out that trench based IGBTs, especially for higher voltages, exhibit an inherently higher effective gate input capacitance when compared to planar IGBTs which results in less controllability for optimum switching performance during IGBT turn-on [3][4]. The new TSPT+ presented in this paper is overcoming this negative aspect while offering a low loss performance and therefore provides an ideal solution for the next generation high voltage IGBTs [5].

For the anti-parallel diode, the losses and recovery softness remain the crucial performance targets in order to match the performance of the new TSPT+ IGBT. The FCE concept enables soft recovery under critical conditions in combination with low losses without compromising ruggedness [6].

2. New technologies and design elements

2.1. TSPT+ IGBT technology

In order to achieve the targeted enhanced carrier concentration near the trench emitter, aimed to reduced losses, the TSPT+ uses a striped architecture for the active Trench MOS Cell in combination with an n-enhancement layer encompassing the p-channel regions, as shown in Fig. 2.

A floating p+ well, deeper than the trench depth, is introduced in the region between active cell pairs and its capacitive coupling to the emitter potential node is optimized in order to achieve a low effective gate input capacitance compared to state-of-the-art trench IGBT designs while providing optimum reverse blocking capability. Moreover, the enhancement layer is used outside the trench MOS cell to separate the active trench gates from the floating deep p+ well. Such feature allows the reduction of the hole accumulation in the regions between active cells during turn-on switching, which plays a crucial role in defining the Miller capacitance and the consequent dI/dt.

The combination of the described enhanced trench cell architecture with the already well-optimized SPT buffer technology enables the TSPT+ to provide excellent losses performance, smooth switching behavior and high turn-off ruggedness.

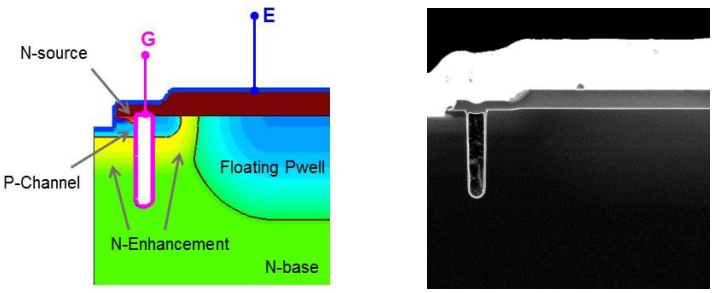

Fig. 2. Schematic and SEM cross section of half pitch TSPT+ IGBT cell

2.2. Field Charge Extraction Diode with Field Shielded Anode

Figure 3a shows the schematic cross-sections of the active area of the Field Shielded Anode (FSA) diode [7]. A high p+ doping forms the anode contact and a deep diffused p- buffer anode supports the electric field during blocking. An n-buffer layer is introduced at the cathode and the high n+ doping forms the contact. Deep levels generated by heavy ion-irradiation tailor the static and dynamic properties.

In contrast to the uniform backside contact of the FSA diode, the cathode of the FCE diode consists of a two-dimensional lattice of p+ islands embedded in the high n+ cathode doping (Fig. 3b and 3c). At the end of the recovery phase, when the electric field gets close to the cathode, the gain of the internal bipolar transistor increases and triggers an injection of holes from the p+ areas. This additional supply of holes enables a soft reverse recovery by preventing the stored charge to get too small to keep up a continuously decreasing reverse current as the electric field propagates towards the cathode, which would result in a current snap-off.

On the other hand, the forward voltage of the FCE diode depends on the buffer concentration, and on the area ratio of the p+ and n+ cathode regions: the larger the p+ area the more pronounced is the impact on the forward voltage V_F drop. By a thinner silicon and an optimum buffer design combined with a p+ area, which is kept less than 10% of the full diode area, the 3.3kV FCE diode is able to provide a forward voltage drop, which is only 50mV higher than the FSA diode platform for an improved softness behavior and with comparable blocking and SOA capability.

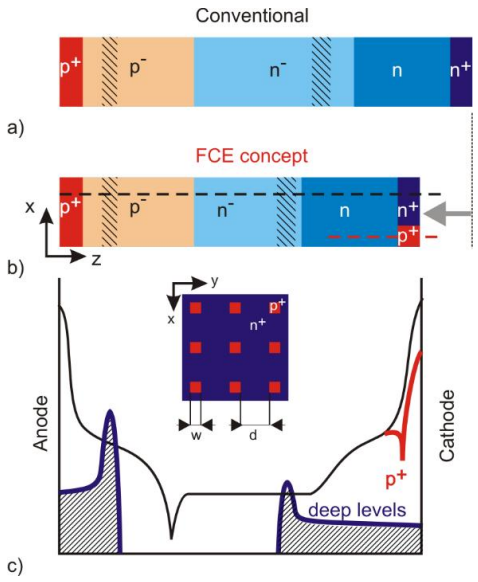

Fig. 3. Schematic drawing of the diode structure. a) Cross-section of the active area region of FSA diode b) Cross-section of the FSA with FCE concept using p+ areas at the cathode side. c) Schematic doping profiles with deep levels. In the inset: backside of the diode with the p+ islands in the n+ cathode contact. The width w and the distance d are critical design parameters for the performance.

3. Electrical performance of the 3.3kV HiPak2 module

The new 3.3kV HiPak2 module employing TSPT+ IGBT and FCE diode technologies is rated 1800A and specified for operating at a junction temperature of T_j=150°C. On module package side, the substrate layout is optimized to incorporate 20% more diode active area so that the

diode performance can keep up with the increased current rating of the TSPT+ IGBT. This section illustrates the results of the static and dynamic measurements carried out to assess the module performance.

3.1. TSPT+ IGBT characteristics and losses

In Fig. 4, the on-state curves of the 3.3kV TSPT+ IGBT are shown compared to the SPT+ characteristics. The typical on-state voltage drop at a nominal current of 1800A and T_j=150°C is 2.8 V. The TSPT+ IGBT shows a positive temperature coefficient for V_{ce_sat}, starting already at low currents, which enables a good current sharing capability between the individual chips in the module.

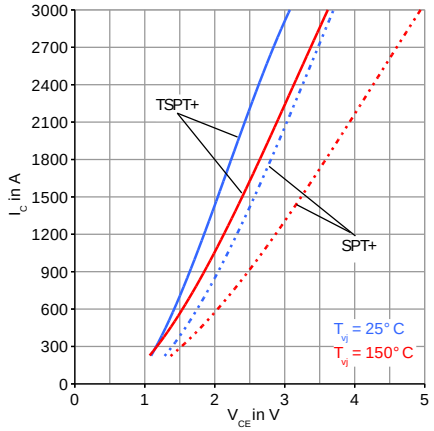

Fig. 4. HiPak2 Module conduction characteristics: 3.3kV TSPT+ IGBT compared to SPT+.

The turn-off waveforms shown in Fig. 5 are measured under nominal conditions, i.e. I_C=1800A and V_{CE}=1800V. In this test, the module is turned off using an external gate resistor $R_{g,off}$=1.5Ohm and a stray inductance L_S=100nH which results in a voltage rise with dV/dt=2230V/us. The optimized n-base region combined with the SPT buffer allows the collector current to decay smoothly, ensuring soft turn-off behavior without excessive voltage peaks or oscillations.

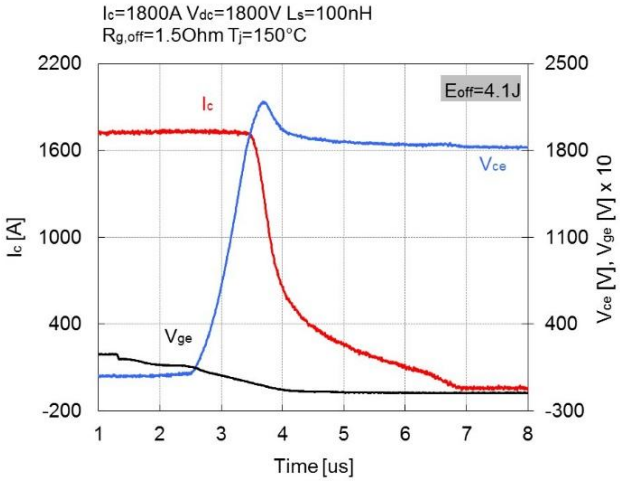

Fig. 5. 3.3kV TSPT+ IGBT turn-off under nominal conditions measured on module level.

The trade-off curves between the IGBT on-state voltage drop and the turn-off losses are presented in Fig.6 where the TSPT+ technology is compared to the SPT+ at the nominal current rate of the new module (1800A).The different sets of points on the technology curves correspond to IGBTs with different anode emitter efficiencies. The TSPT+ IGBT exhibits approximately 20% lower on-state voltage drop for the same turn-off losses as compared to the standard SPT+ technology.

In order to reduce the influence of the Miller capacitance on the turn-on speed, a gate emitter capacitor C_{ge}=330nF is used to characterized the turn-on switching. Since the external gate-emitter capacitance slows down the switching behavior of the IGBT, a gate resistors value $R_{g,on}$=1Ohm is used as an optimum driving condition.

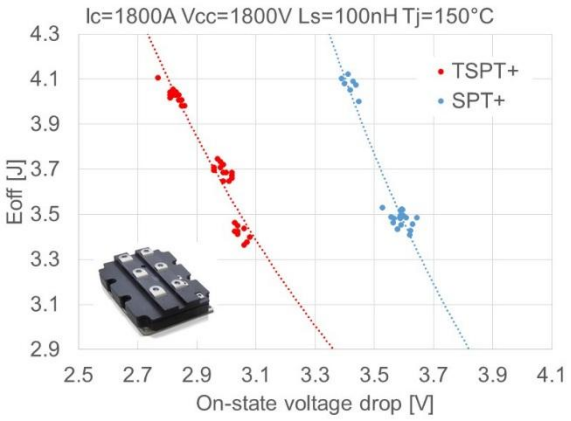

Fig. 6. 3.3kV IGBT technology curve: TSPT+ compared the SPT+ at I_c=1800A.

Figure 7 shows the turn-on waveforms under the mentioned gate driving conditions, which, in combination with the low FCE diode losses, brings the turn-on switching losses down to a typical value of 2.8J at T_j=150°C.

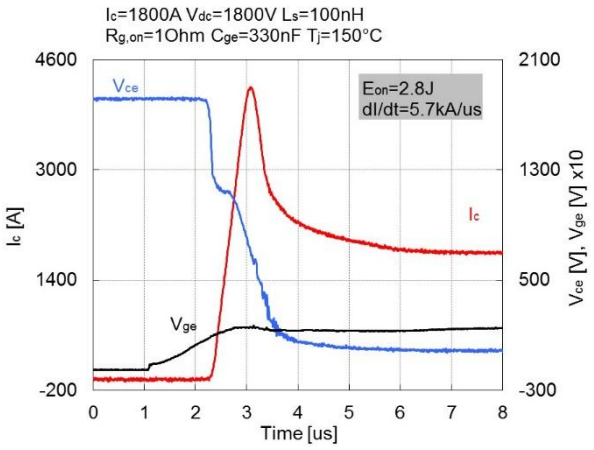

Fig. 7. 3.3kV TSPT+ IGBT turn-on under nominal conditions measured on module level.

3.2. FCE diode characteristics and losses

In Fig. 8, the on-state characteristics of the 3.3kV FCE diode are shown. Due to the advanced plasma shaping utilizing double local lifetime control by irradiation, the diode has a positive temperature coefficient of V_F starting from I_F= 1200A. At rated current and T_j=150°C, the diode shows a typical on-state voltage drop of 2.3V.

The reverse recovery waveforms of the diode under nominal switching conditions is presented in Fig. 9. By carefully designing the cathode-sided lifetime irradiation peak, a short but still smoothly decaying current tail was achieved.

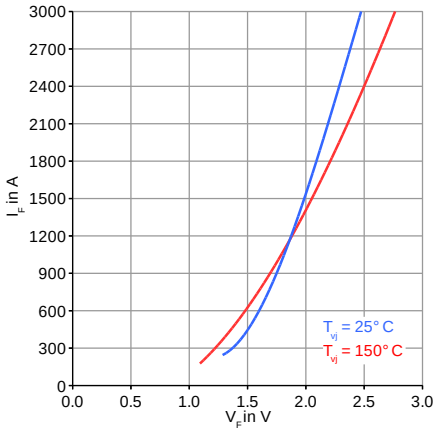

Fig. 8. Forward characteristics of the 3.3kV FCE diode (module level measurements).

Under nominal conditions and using $R_{g,on}$=1Ohm and C_{ge}=330nF, the diode recovery losses are 2.5J at T_j=150°C. Thanks to the high ruggedness and soft recovery behavior of the FCE technology, the diode can be switched with a high dI_F/dt of 5700A/us.

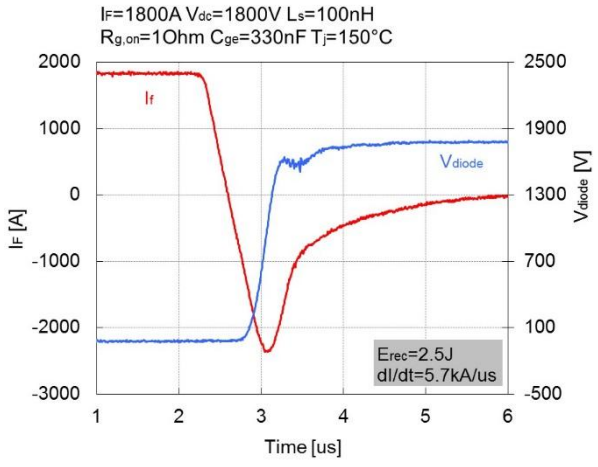

Fig. 9. 3.3kV FCE diode reverse recovery under nominal conditions measured on module level.

3.3. IGBT turn-off and short circuit ruggedness

The cell architecture of the TSPT+ IGBT technology has been designed with respect to the cell cross section and in the direction perpendicular to the cell stripes in order to keep the high standard of turn-off ruggedness shown from the SPT+ generation. Figure 10a shows a turn-off waveform at module level, where a current of 10105A, which corresponds to more than five times the nominal current, is switched-off against a DC-link voltage of 2500V at a junction temperature of 150°C. The test is performed with an external gate resistance of 1.5Ohm and a stray inductance of 100nH without using any clamp or snubber.

The TSPT+ IGBTs are capable of sustaining a long period of strong dynamic avalanche during the turn-off transient showing an excellent SOA capability with a maximum turn-off peak power P_{pRec}=26.8MW.

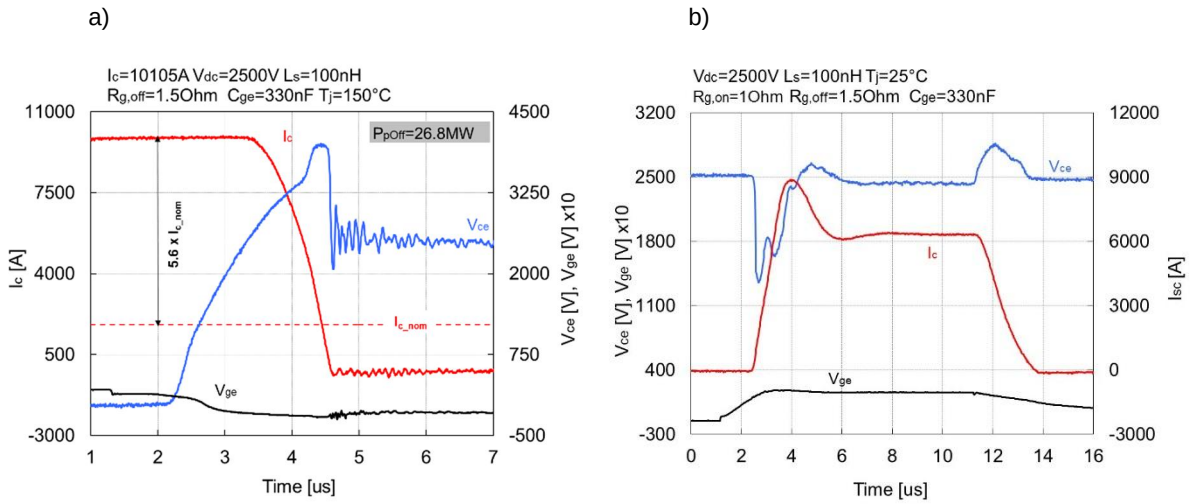

Fig. 10. 3.3kV TSPT+ IGBT module: a) turn-off under extreme SOA conditions b) short circuit under nominal SOA conditions.

The short circuit waveforms of the 3.3kV TSPT+ module measured at room temperature are shown in Fig. 10b. The SPT-buffer and the anode emitter efficiency of the IGBT have been optimized for the targeted short-circuit ruggedness to withstand a short circuit at V_{GE}=15V for all DC-link voltages up to 2500V and junction temperatures up to T_j=150°C.

3.4. FCE diode softness and reverse recovery ruggedness

The diode recovery waveforms in Fig.11a show the comparison of the snap-off behavior at T_j=150°C of the FSA and FCE diode when used as freewheeling diodes for the TSPT+ IGBT in the adverse conditions of very low current (I_F=30A) and very fast IGBT turn-on switching speed ($R_{g,on}$=0.666Ohm). A snap-off at the end of the tail phase is present for both diodes. However, the overvoltage for the FCE is 250V lower than for the FSA, which enables to operate it within the specification of the rated voltage. The beneficial effects of the p+ island hole injection is clear in the oscillations following the main peak which are immediately damped to the DC-link voltage in the case of the FCE.

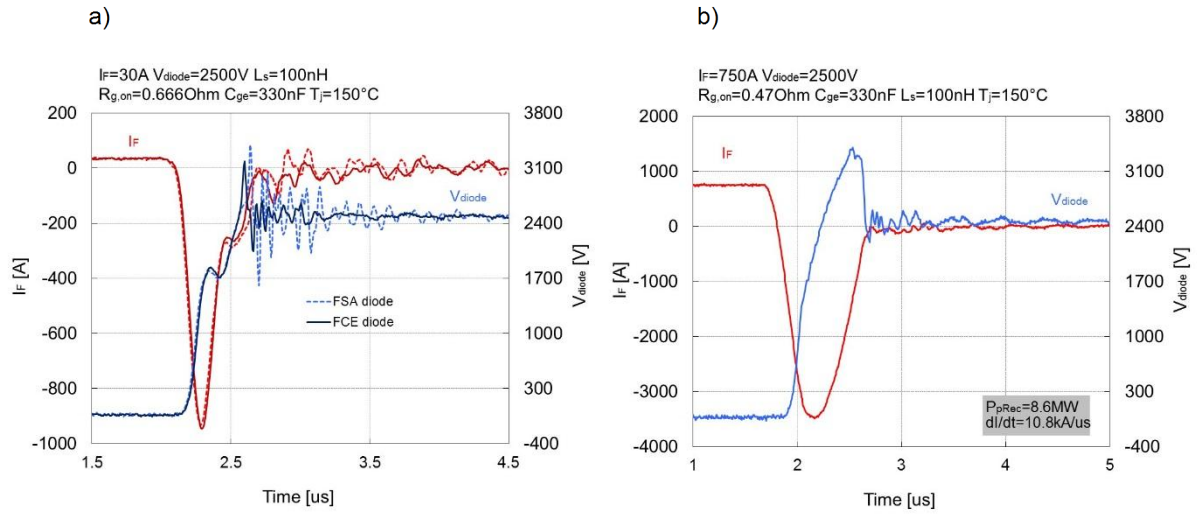

Fig. 11. 3.3kV HiPak2 1800A FCE diode: a) turn-off under snap-off conditions comparing FSA and FCE diode as auxiliary device for TSPT+ IGBT b) 3.3kV FCE diode turn-off under SOA conditions.

The diode reverse recovery SOA module test measured with a forward current of 750A and a DC-link voltage of 2500V is presented in Fig.11b. The diode is switched under extreme conditions at T_j=150°C using an external gate resistor of 0.47Ohm, which results in a switching speed of 10800A/us and a peak power of 8.6MW.

4. Conclusions

A new 3300V, 1800A HiPak2 IGBT module employing the TSPT+ IGBT with Enhanced Trench MOS technology and Field Charge Extraction FCE diode has been presented. Due to the advanced IGBT and diode device technologies, the module offers exceptionally low losses and high Safe Operating Area. Smooth switching characteristics and high dynamic ruggedness have also been demonstrated. The new module will provide high voltage system designers with enhanced current ratings and open possibilities for optimized designs. In the future, the new chip technologies will also be extended to higher voltage classes up to 6.5kV and employed in next generation modules, including the LinPak platform [8].

References

[1] Rahimo, M et al. “Novel Enhanced-Planar IGBT Technology rated up to 6.5kV for Lower Losses and Higher SOA capability” Proc. ISPSD’06, Italy.
[2] K. Nakamura et al, Proc. “Wide cell pitch 1200 V NPT CSTBTs with short circuit ruggedness” Proc. ISPSD’01, Japan.
[3] K. Nakamura et al, “Wide Cell Pitch LPT(II)-CSTBTTM(III) Technology Rating up to 6500V for Low Loss” Proc. ISPSD’10, Japan.
[4] Y. Toyota et al, “Novel 3.3kV Advanced Trench HiGT with Low Loss and Low dv/dt Noise” Proc. ISPSD’13, Japan.
[5] M. Andenna et al, “The Next Generation High Voltage IGBT Modules utilizing Enhanced-Trench ET-IGBTs and Field Charge Extraction FCE-Diodes” Proc. EPE`14, Finland.
[6] S. Matthias et al, “Field Shielded Anode concept enabling higher temperature operation of fast diodes” Proc. ISPSD’11, USA.
[7] S.Matthias et al, “Inherently Soft Free-Wheeling Diode for High Temperature Operation” Proc. ISPSD’13, Japan
[8] S.Hartmann et al. “The LinPak high power density design and its switching behavior at 1.7kV and 3.3kV” Proc. PCIM’16, Nürnberg.