High-Power SiC and Si Module Platform for Automotive Traction Inverter

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Published at PCIM Europe 2019, www.pcim-europe.com

Abstract

A novel power semiconductor module platform for the automotive powertrain is presented in this paper. Mold modules are designed for symmetric and minimized parasitics by applying alternating and multilayer current routing. All interconnects are solder-free to provide superior reliability, and to meet present and future automotive requirements, e.g., passing 1000 temperature shock cycles in the range of -40 to 150 °C. SiC or Si devices are packaged in the same external outline offering a simple scalability for inverter classes in the 150 – 350 kW power range. A screw-less and O-ring-less 3-phase inverter module is achieved by a laser welding of the mold modules to a low-cost Al cooler enclosure.

1 Introduction

The recent electric vehicle (EV) outlook from the International Energy Agency projects a rapid growth of global vehicle stock from 3 million vehicles in 2017 up to 228 million electric vehicles by 2030 (excluding two- and three-wheelers, EV30@30 scenario) [1]. This tremendous growth will come along with the need for cost-effective and reliable power electronics converters within the electric powertrain of hybrid, plug-in hybrid, and battery-electric passenger vehicles, as well as light-commercial vehicles, buses, and trucks.

In the context of this paper, a focus is set on the traction inverter which is a key component that drives the electric motor and feeds back regenerative energy into the battery. At the heart of the inverter are power semiconductor devices arranged in multi-chip power modules that control the motor torque and speed via pulse width modulation. Such semiconductor modules have been optimized over decades to satisfy the needs of industrial applications, however, new aspects get important for the automotive segment [2].

Costs: Generally, cost reduction is the dominant development target and biggest challenge since the automotive environment is extremely sensitive to component cost. Low-cost power module materials and interconnect technologies, as well as manufacturing processes for fast and automated volume production are required. In addition, system design approaches compromising component vs. system cost are important, e.g., by optimizing powertrain efficiency vs. battery costs in drive-cycle load profiles.

Finally, it should be considered also that premium EVs, buses and trucks might take a different technology path valuing reliability and peak performance higher than mass-volume passenger EVs. Therefore, it is required to understand the performance and physics-of-failure of the various packaging technologies to optimize the cost - reliability ratio for a given application.

Power density and integration: Power modules must be optimized for mechanical integration into highly compact inverters that are mounted in space-restricted engine compartments of EVs. Strategies for power module footprint reduction are the expansion of current routing into the third dimension, the improvement of the cooling path to reduce chip area, and the high-temperature operation of novel wide-bandgap (WBG) semiconductors to extract more power from the same outline [3]. Furthermore, any mounting overhead on system level like screwing, clamping, plugging, etc. should be eliminated or reduced to a

minimum. This goes along with the trend to integrate the power inverter with the electric motor into a single unit to eliminate interfaces and make use of common infrastructure (structural, cooling, busbars).

Reliability: Today's standard industrial interconnect technologies might turn out to be a serious bottleneck to achieve automotive performance requirements [2]. This results from harsh environmental conditions (ambient temperatures, severe vibrations, humidity, salt and water spray), strong cyclic loads (e.g., grade 0 automotive temperature shock cycling with compliance for 1000 cycles in the range of -40 to +150 °C) and future trends of miniaturization, integration to the electric motor and high-temperature operation.

In addition, it is expected that the automotive market dominance will significantly drive innovation and lead to accelerated implementation of new materials and manufacturing methods, which need to be carefully assessed with respect to reliability issues. Examples are the deployment of fast-switching WBG devices, application of new bonding technologies like planar topside bonding, sintering, PCB embedding, etc., and the implementation of heterogenous integration of passives, diagnostics sensors, drivers, transceivers, and other on-board components. Finally, commercial vehicles like buses and trucks are designed for longer lifetime than passenger EVs, e.g., 60'000 vs. 7'000 hours, and the resulting increased reliability demands need to be considered.

2 Power module design concept

A SiC / Si power module platform was developed in this study to address automotive performance requirements. The design approach is characterized by the following key features:

Mold modules: To address the cost issue, a mold module approach has been selected that does not require any housing. In addition, the mold encapsulation provides 1) good environmental protection by low moisture absorption and water vapor diffusion, 2) good cycle reliability by its hard-mold, compressive and low-coefficient of thermal expansion (CTE) encapsulation, and 3) excellent protection against shock, vibration and handling damage.

Solderless interconnections: A completely solder-free power module is realized for the highest cycle reliability and robustness standards. In fact, all interconnections are either sintered or welded. Furthermore, this approach allows for a superior manufacturing throughput, because the sintering of all power module components can be realized in a single process step.

Minimized parasitic inductances: To allow for SiC fast switching, power loop and gate loop inductances as well as coupling coefficients are rigorously minimized. This is achieved by applying a systematic alternating (+/-/+) signal routing of power- and gate circuitry to substrate and terminals, and by using multilayer signal distribution inside the module.

Screw-less cooler integration: A low-cost cooler enclosure is realized by laser welding of mold modules into a structure based on cheap embossed Al sheets. In this manner, a compact 3-phase inverter module is achieved without the need for screwing or clamping of O-ring sealings that could pose a risk of leakage.

Scalability: The proposed power module offers several aspects of scaling. First, two different substrates are applied to assemble either a high-power SiC, or a lower-power Si version for the identical external outline. Second, due to a special symmetric substrate layout, further power scaling is possible by adding or removing chips along the length of the module (x-direction in Fig. 2) without impacting stray inductances and coupling coefficients. Finally, module cost can be scaled by applying different power module component materials (substrates, baseplates, bond materials) to optimize for the right cost-performance ratio for the specific target vehicle.

3 Half-bridge module design

The mold modules are designed in half-bridge configuration. Two different types were developed, a 900 V SiC version for screw attachment to the cooler, referred as Generation 1 (Gen 1), see Fig. 1, and a 1200 V SiC and Si version for direct cooler bonding, referred as Generation 2 (Gen 2), see Fig. 2. Both types were designed using similar packaging technologies and materials.

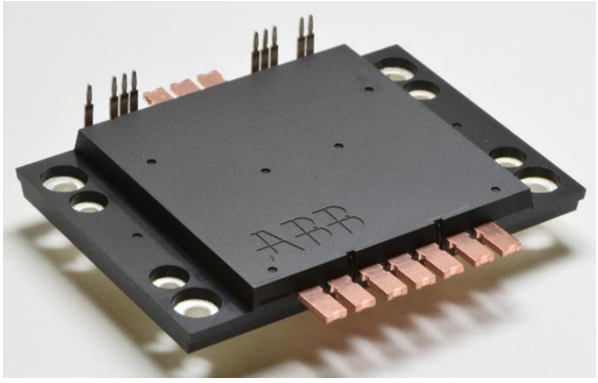


Fig. 1: 900 V SiC mold module, Gen 1 design.

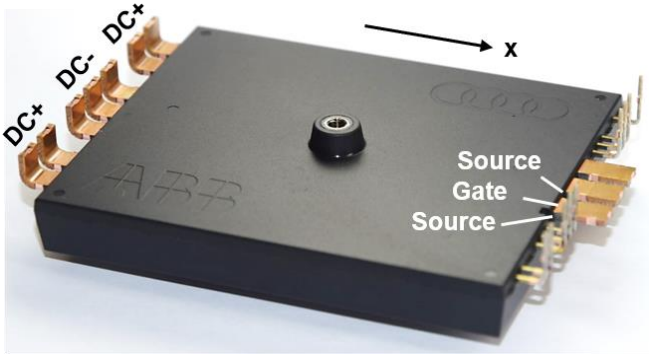


Fig. 2: 1200 V SiC and Si mold module, Gen 2 design.

The half-bridge modules are based on the following components:

1) A CTE-matched pin-fin baseplate made from AlSiC with a pin-field optimized for maximum heat transfer and small temperature differences between parallel chips is applied to support a homogeneous current sharing [4].

2) A main ceramic substrate made from Si_3N_4 is bonded to the baseplate by Ag-sintering.

3) Semiconductor dies, NTC temperature sensor and external per-chip gate resistors (only SiC version) are Ag-sintered to the main substrate.

4) Top plates made from Cu are Ag-sintered to the power semiconductor chip top surface to enable high-reliability Cu source wire bonds. Al is used for the remaining bond wires (gate, auxiliary source, substrate-to-substrate bonds), see Fig. 3.

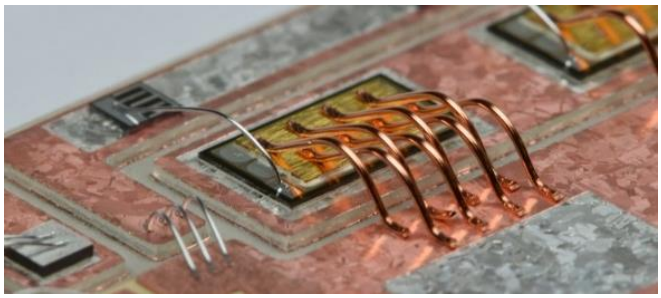


Fig. 3: Cu source wire bonding on top plate; Al wire bonding for gate, auxiliary source (not shown in figure), NTC (bottom left) and interconnects on substrate.

5) Al_2O_3 second-level substrates are Ag-sintered to the main substrate and used for low-inductance current routing of the control signals.

6) Cu power terminals and auxiliary terminals with press-fit pins are bonded to the main substrate by ultrasonic welding, see Fig. 4.

7) The module is encapsulated by an epoxy-based transfer mold material with optimized CTE. A screw thread is embedded in the mold compound that allows tight fixation of the gate driver board and alignment of the modules during assembly on the cooler enclosure.

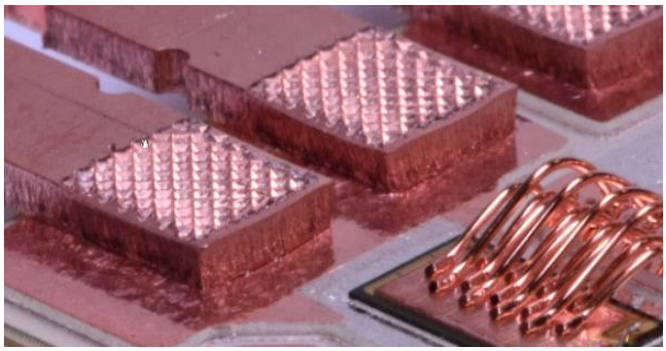


Fig. 4: Ultrasonic welded leadframe terminals.

The substrate and terminal design was carefully optimized to achieve symmetric and minimized stray inductances and cross-coupling. This is achieved by the following design approaches, see Fig. 5:

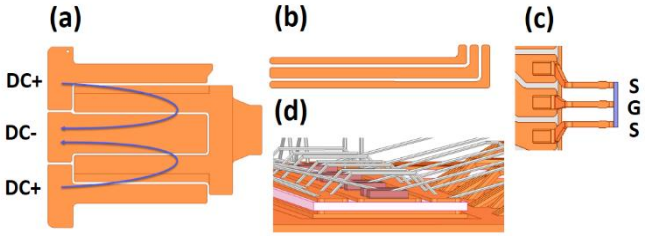


Fig. 5: (a) Alternating current routing for DC+ / DC- current path; (b) and (c): Kelvin source and alternating control signal routing on substrate and terminals; (d) Multilayer signals on second level substrate for minimal magnetic coupling into the gate - source control loop.

The DC commutation loop and the gate loops of the half-bridge module are arranged in an alternating design so that the magnetic fields cancel out to a large extent. In addition, a control signal distribution on second level substrates reduces the cross-coupling from the power into the control loop.

Electromagnetic parasitic inductances were calculated by using the simulation tool ANSYS Q3D. Table 1 provides the results of this calculation specifying the commutation loop inductance $L\sigma$, the gate inductance L_G, and the mutual inductances M for power-gate loop cross-talk. Note that due to the large IGBT chip size, the alternating DC+ / DC- current routing (Fig. 5a) on the substrate was not possible for the Gen 2 Si version. This explains the higher L_σ for the Si module. In addition, the 900 V SiC Gen 1 module has lower L_σ because terminal clearance and creepage distances are smaller, as the module targets a 400 V DC-link only (as compared to 800 V for Gen 2).

Module	L_σ, nH	L_G, nH	M_{avg}, nH	ΔM_{max}, nH
Gen 2 SiC	6.2	HS: 17 LS: 23	HS: -0.02 LS: -0.05	HS: 0.06 LS: 0.11
Gen 2 Si	9.5	HS: 14 LS: 17	HS: -0.02 LS: -0.18	HS: 0.07 LS: 0.04
Gen 1 SiC	4.5	HS: 11 LS: 15	HS: -0.24 LS: -0.20	HS: 0.02 LS: 0.10

Table 1: Simulated parasitics for different module types; L_σ: commutation loop inductance, L_G: gate loop inductance, M_{avg}: average mutual inductance across parallel chips (cross-talk), ΔM_{max}: max. spread of mutual inductances between parallel chips; HS: high-side; LS: low-side of module.

Beside the small commutation loop inductances, it is a desired feature of the given designs that gate inductances and mutual inductances are small and symmetric across parallel chips allowing for fast and balanced switching. A simulation of the per-chip switching transients for the SiC Gen 2 module is shown in Fig. 6. Note that the data indicates a small difference of chips 1 - 4 vs. 5 - 8. This comes from the die arrangement in two rows leading to slightly different coupling and gate inductances.

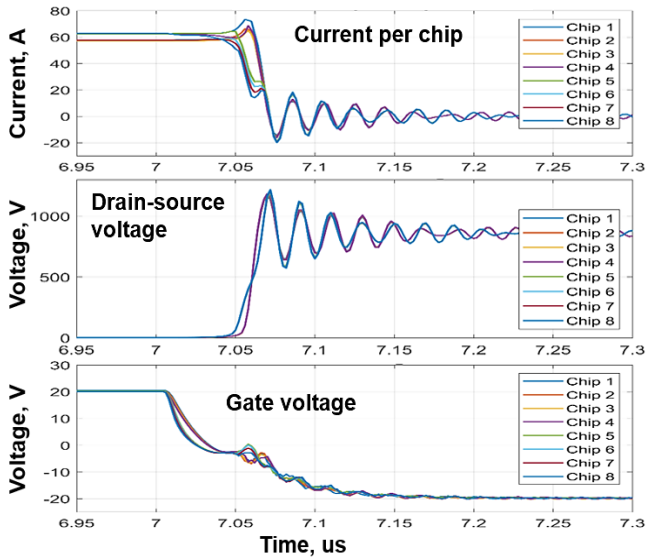


Fig. 6: Simulated switching waveforms for turn-off event based on parasitics extracted at 100 MHz; High-side chips of Gen 2 SiC module are plotted.

4 Packaging technologies

The packaging technologies used for assembly of the half-bridge modules are described in detail in [5], [6], and [7], a summary is given here:

Die attach: SiC and Si chips were sintered on Si_3N_4 ceramic substrates with Ag or NiAu surface plating. We used nano-particle based Ag materials sintered at pressures ranging from 10 to 20 MPa and temperatures around 250 °C. A pick & place tacking process was used for accurate alignment, and chips and top plates were sintered in a single step. Thermal shock cycling tests between -40 °C to 150 °C with a dwell time of 5 minutes at each temperature were conducted to verify the sinter bond quality. After regular intervals of cycles, the samples were inspected using scanning acoustic microscopy (SAM) to detect any delamination or degradation of the bond layers. An example for such an SAM inspection of SiC MOSFETs is shown in Fig. 7.

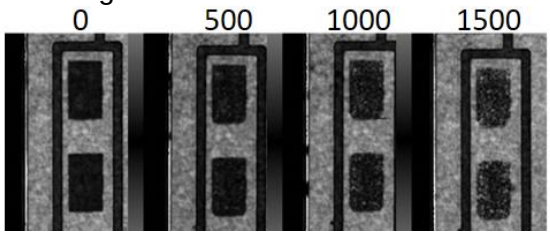


Fig. 7: Die attach during shock cycling inspected with SAM. Values on top of the scans indicate the number of thermal shock cycles -40 to +150 °C.

Topside interconnection: It is well known that apart from the die attach, the chip topside interconnection is a main limiting factor for the lifetime of power semiconductor devices in active load cycling conditions. To improve this issue, we have focused on an approach of sintering a top plate on devices with standard Al metallization and NiAu plating. The top plate acts as a buffer and allows for Cu wire source bonding with superior power cycling lifetime [8]. Different materials (Cu, Mo) and thicknesses (50 µm, 70 µm, 100 µm, 150 µm, 200 µm) have been tested [5]. As a conclusion, a top plate made of Cu or Mo in the thickness range of 50 – 100 µm showed the best reliability in thermal shock cycling (Fig. 8).

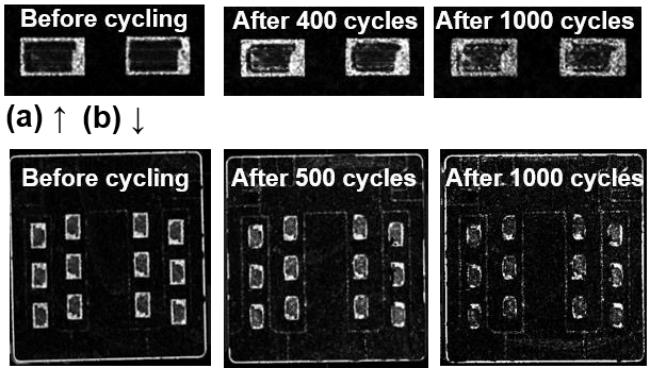


Fig. 8: Top plate attach during shock cycling inspected with SAM: (a) 50 µm Cu top plate, (b) 100 µm Mo top plate; Cycling -40 / 150 °C, 5 min.

Cu wire bonding: Heavy Cu wire bonding has been proven to be a superior alternative to Al wire bonding with greatly improved power cycling

lifetimes (due to the higher electrical and thermal conductivities and greater mechanical strength of Cu). However, the process comes with some challenges such as high bond forces, narrow process window, influence of top plate material, thickness and surface properties, as well as accelerated tool wear. We have developed a 300 µm Cu wire bonding process that was optimized by pull and shear testing. A special focus was dedicated to identify the best compromise for the bond force to avoid cratering and chip topside damaging (gate-source short), and to achieve sufficiently high shear forces.

Power cycling: First power cycling tests of Gen 1 modules assembled with single dies have been conducted to verify the overall topside reliability. SiC MOSFETs from two different vendors were cycled using the following parameters: t_{on} = t_{off} = 1 s, ΔT = 100 ± 2 K, $T_{j,max}$ = 200° C, I ≈ 80 A = const., failure criterium: forward voltage drop (heating voltage) V_{ds} + 20%. Detailed results of this study will be published elsewhere [9], the main results are summarized as follows: Whereas Al wire bond reference modules failed at around 20'000 cycles, the sintered top plate and Cu wire bonded modules were able to reach more than 1'000'000 cycles without failure. Typical data of V_{ds} across 1'200'000 cycles is shown in Fig. 9.

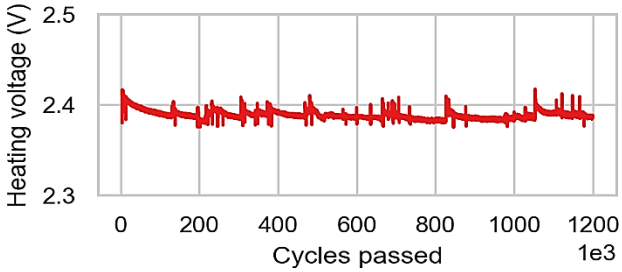


Fig. 9: Power cycling of Gen 1 module: Forward voltage drop is plotted over 1.2 M cycles 100 – 200 °C; Test conducted at Fraunhofer IISB, Germany.

Beside the long-runners in power cycling there was also a sub-population of samples failing earlier with a gate-source leakage issue. Failure analysis is currently still ongoing and we suspect that the root cause might be a pre-damage of chips by an inappropriate manufacturing, or an aging mechanism potentially leading to SiC die cracking (Fig .10).

Substrate attach: Among the different ceramic substrate materials commonly used for high-power semiconductor modules, Al/AlN DBA and Cu/Si_3N_4 AMB substrates have been reported to achieve the highest thermal cycling capabilities. Since Al metallization can be problematic for the ultrasonic

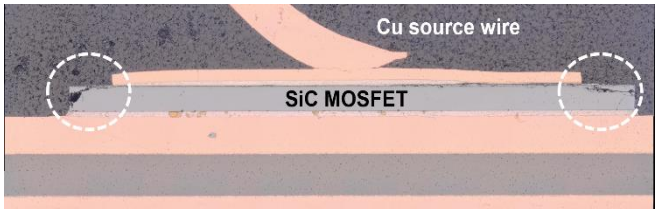


Fig. 10: Sample with die cracks after power cycling.

welding of Cu terminals, a Si_3N_4 AMB substrate was selected. In addition, to achieve highest-level reliability when targeting high-temperature operation of SiC, we have chosen to develop a substrate sintering process.

First, different baseplate materials (Al, Cu, AlSiC), different bond line thicknesses (20 and 40 µm) and different sinter materials (Ag film, Ag preform with metal core) were tested by thermal shock cycling [6]. It turned out that the metal-core sinter preform and an AlSiC baseplate provide best reliability performance. Figure 11 shows the result of this process optimization. Virtually no delamination of the substrate-to-baseplate attach was found after 1000 thermal shock cycles both from −40 °C to 150 °C and from −5 °C to 200 °C, as well as high-temperature storage tests for 1000 hours at 200 °C and 225 °C.

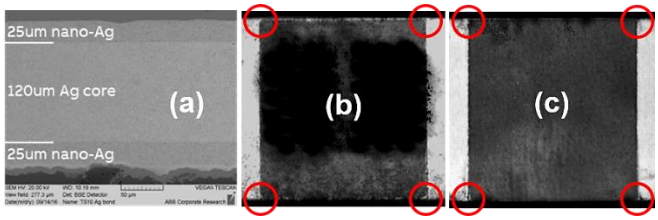


Fig. 11: (a) Cross section of sintered Ag preform with metal core, (b) SAM image after 1000 cycles -40 /150 °C, (c) SAM image after 1000 hours hot storage at 225 °C; Red circles highlight substrate edges most susceptible to cycling delamination and bond layer cracking.

In addition, a -50 / 175°C thermal shock cycling experiment was conducted to compare the performance of the Gen 2 SiC module to a standard industrial / automotive module based on a SnAgCu soldered Al_2O_3 DBC substrate on a Cu baseplate (Fig. 12). Whereas the standard module fails already after 100 cycles, the sintered module did not show any indication of bond layer aging after 1000 cycles. This underlines the superior reliability performance of the chosen approach.

Terminal attach: Leadframe terminals are bonded to the substrate by an ultrasonic welding process. Leadframe materials, bond foot geometry and substrate metallization were optimized to achieve large-area, high-reliability welding joints.

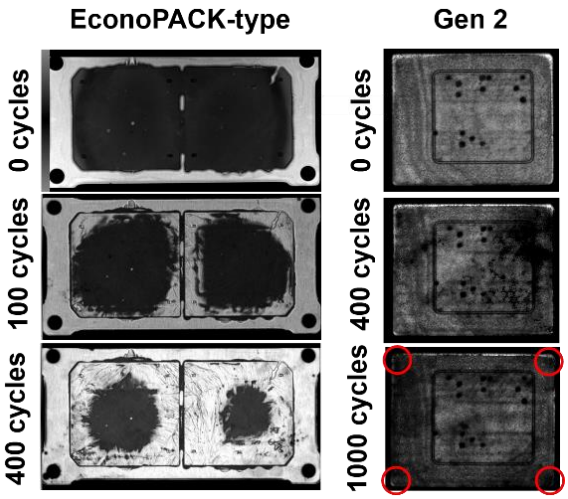


Fig. 12: Shock cycling -50 / 175 °C (35 min dwell time) for EconoPACK-type vs. Gen 2 SiC module.

Mold encapsulation: Transfer-mold encapsulated modules are attractive for automotive applications since they offer benefits with respect to cost (no housing required), cycle reliability (hard mold, compressive encapsulation), environmental withstand (low moisture absorption), and mechanical robustness (vibration, shock and handling). As reported in [7], the mold compound adhesion is identified as a key issue for large-area transfer molding, and usage of a suitable material is very important. We selected a multi-aromatic ring resin epoxy compound with a very small stress – resistance ratio, defined as the product of CTE and flexural modulus over the product of adhesion strength and flexural strength.

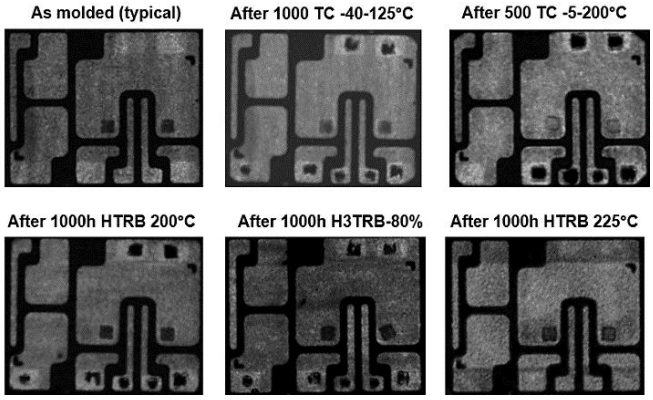


Fig. 13: SAM inspection of mold compound adhesion after different long-term aging tests. A test module with an over-molded volume of 80 x 65 x 5 mm^3 was applied in these experiments [7].

By this selection, Gen 2 modules passed 1000 cycles of air-to-air cycling -40 / 125°C with a 20 min dwell time without any delamination of mold compound. In addition, as can be seen in Fig. 13, molded test modules (as described in [7]) passed also 500 cycles -5 / 200 °C, 1000 hours of hot storage at 200 °C, 1000 hours of hot & humid storage at 85 °C / 85 % relative humidity, but could not keep adhesion for a storage test at 225 °C. Novel resin materials are required for operation at such high temperatures.

Finally, surface oxidation of epoxy material might pose another risk. Figure 14 shows a cross-section of a part of a test module that was stored at 200 °C for 1000 hours. The surface oxidation layer has a thickness of 70 μm.

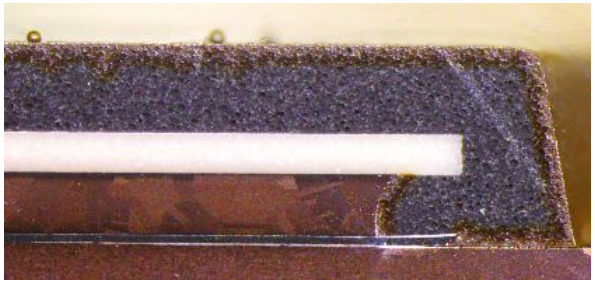


Fig. 14: Surface oxidation of mold compound after 1000 hours of hot storage at 200 °C.

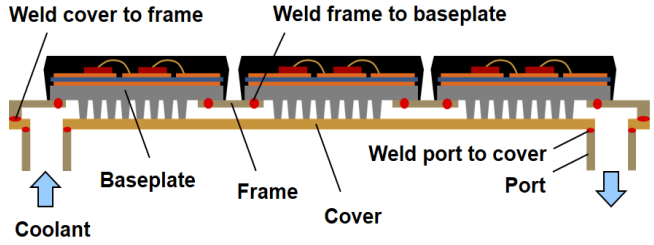
5 Three-phase inverter module and cooler design

Water-glycol cooling of power semiconductor modules by means of pin fins has become a preferred way in the thermal management of traction inverters of EVs. Pin fins are either integrated in the module's baseplate for direct cooling, or are part of a separate, closed cooler, to which the modules are attached.

Bonded cooler enclosure: Whereas the Gen 1 module was designed for screw attach and sealing by an O-ring, the Gen 2 module has the full cooler metallurgically bonded to the mold modules. Such an approach has the advantages that the 3-phase module gets more compact (space for screws, washers and O-rings omitted), that the number of screws in the inverter can be drastically reduced, and that reliability / quality management concerns related to the O-ring sealing are eliminated.

Serial vs. parallel flow: Detailed information on the methods of pin-field optimization of our module baseplates can be found in [4]: To select the pin geometry and flow configuration, an optimization based on analytical, 3D heat-conduction, and 3D conjugate heat-transfer modeling was applied. We concluded that a serial flow configuration along the three half-bridge modules performs better than parallel flow with an estimated 65% higher heat transfer coefficient. Parallel flow does not make use of the allowed pressure drop and yields slow flow velocities preventing turbulent flow [4].

Cooler design and assembly: The cooler assembly concept and final inverter module with cooler are shown in Fig. 15. The cooler consists of three basic parts: 1) An Al frame plate that is laser-welded to the mold modules in a first step, 2) an Al cover plate that is welded to the frame in a second step, and 3) fluid ports that are welded to the cover in a final step.



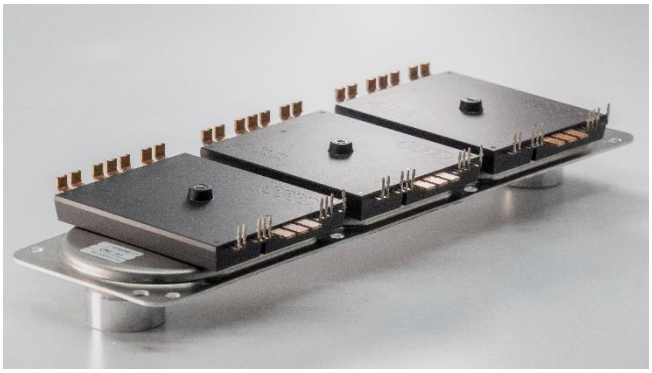


Fig. 15: Cooler schematics and 3-phase power module.

A critical bonding process is the welding of the cooler frame to the mold module baseplates. Heat input during this welding step must be minimized to avoid thermal damaging of the modules. Due to this reason, laser welding has been chosen since it is an exceptionally fast process, limiting the temperature rise at the mold compound side of the power module to less than 200 °C. Careful process optimization and well-designed jigs are required to achieve a fluid-tight joint with high process repeatability. As an example, material cracks within the welded bond lines may occur that can lead to coolant leakage, see Fig. 16.

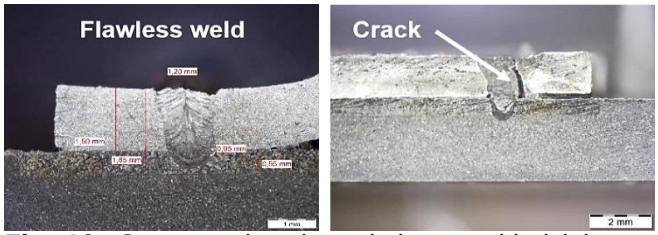


Fig. 16: Cross-section through laser-welded joint on AlSiC baseplate: Flawless weld (left) vs. weld with an internal crack formation (right).

Cooler validation: Heat-transfer modeling and simulations were verified using infrared (IR) thermography on open modules without mold compound. Typically, we found deviations as small

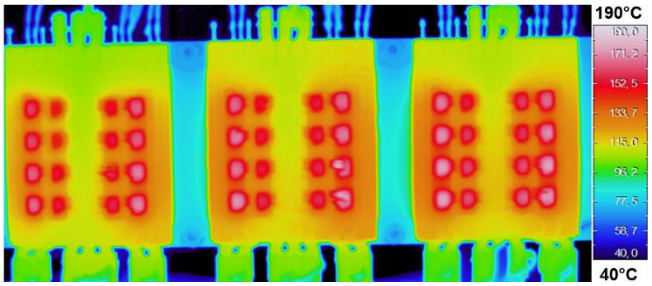


Fig. 17: Infrared thermography of 3-phase Gen 2 SiC inverter module assembled without mold compound; Both, HS and LS chips are powered with a DC current of 600 A.

as 10% between simulated and measured chip temperatures. Fig. 17 shows an example of an IR measurement for the Gen 2 SiC module.

6 Switching losses and rating

Double-pulse testing was conducted to determine the switching losses and to assess the power rating to the different module variants. Tests were performed in the temperature range from -20 to 150 °C at DC-link voltages up to 850 V, and for currents up to 600 A. Switching waveforms for a Gen 2 SiC hard switching are shown in Fig. 18.

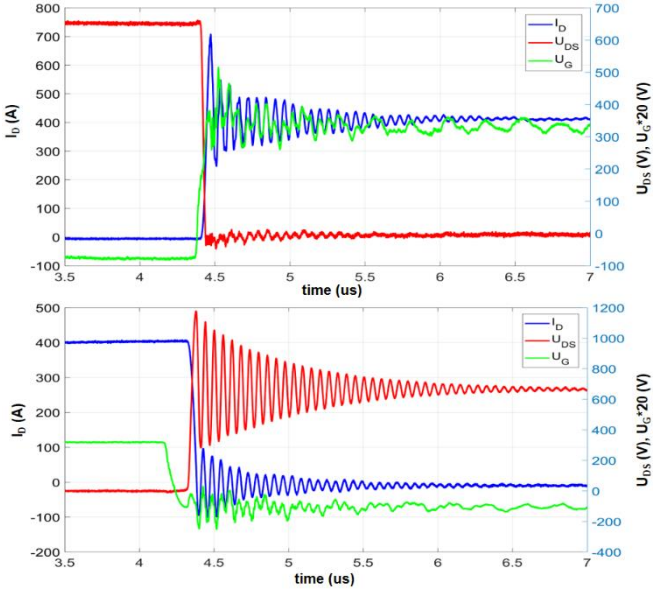


Fig. 18: Turn-on (top) and turn-off (bottom) switching waveforms of SiC Gen 2 module at 25°C; blue: current, red: voltage, green: gate voltage.

The measurement of Fig. 18 was done at a DC-link voltage of 650 V, a current of 400 A, a temperature of 150 °C, a gate resistance of R_G = 0 Ω (hard switching) and for a stray inductance of the test setup of about 30 nH. Pronounced oscillations results from the fast switching combined with the high stray inductance of the tester. It is therefore important to operate the module in a low inductive inverter environment for optimal performance. In

general, however, the traces are quite clean. This is especially important for the critical gate voltage trace (to avoid parasitic turn-on and other issues). Switching losses as measured by double-pulse testing are reported in Table 2. SiC losses are given for a gate resistance of 1.7 Ω, and for a hard-switched configuration with 0 Ω. In addition, Gen 2 Si losses and Gen 1 SiC losses (at a DC-link of 400 V) are given. Note that tests were performed with different double-pulse setups and gate drivers which makes a direct comparison difficult.

Module type	R_G [Ω]	E_{on} [mJ]	E_{off} [mJ]	E_{rr} [mJ]
SiC Gen 2	1.7	17.8	6.9	-
SiC Gen 2	0.0	1.4	10.8	-
Si Gen 2	0.0	23.9	71.1	50.1
SiC Gen 1	1.3	3.7	4.1	-

Table 2: Switching losses measured by double-pulse testing; Gen 2: U = 800 V, I = 400 A, Gen 1: U = 400 V, I = 400 A; T = 100 - 150 °C; R_G: total chip-external gate resistance.

Finally, using these switching and on-state losses, a module rating for the SiC and Si module can be extracted for a pulse-width modulated inverter with continuous modulation and without injection of the third harmonic [10]. This data is plotted as a function of switching frequency in Fig. 19.

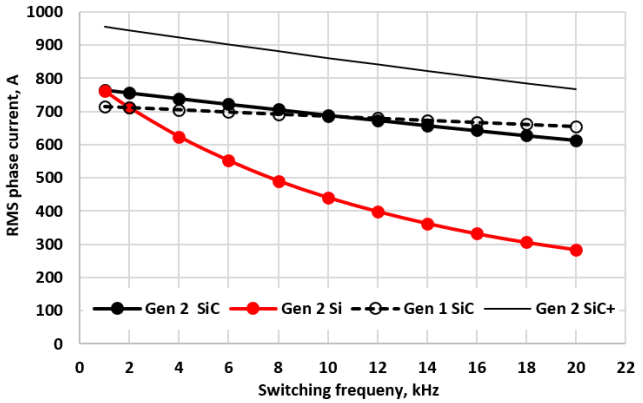


Fig. 19: Power module rating as a function of switching frequency. Data is given for Gen 2 SiC and Si modules at 800 V, and for Gen 1 SiC at 400 V; Gen 2 SiC+: One additional row of chips; R_G = 1.7 Ω / 0 Ω for SiC / Si; Modulation: cos φ = 0.825, mod = 0.95; Cooling: T_{inlet} = 65 °C, flow rate 10 l/min / 7 l/min for SiC / Si.

As we can see, the power rating is a function of the applied switching frequency. At 20 kHz the SiC version achieves 2.2 times higher current than the Si version with the same module footprint. This factor falls to about 1.6 at 10 kHz. In addition, a rating for a scaled Gen 2 SiC+ module is shown, where one row of chips is added, increasing the module length by ~10 mm and extending the current capability to the 800 – 900 A region.

7 Conclusions

An automotive SiC and Si power module platform targeting inverter classes of premium and commercial EVs in the power range of 150 – 350 kW was presented in this paper. Mold modules are bonded to an integrated cooler enclosure that allows for a compact, and screw-less inverter design. High-reliability packaging technologies are employed enabling operation up to T_j = 200 °C.

8 Acknowledgements

The authors want to thank Mr. Fabian Dresel from Fraunhofer IISB for power cycling tests and data.

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