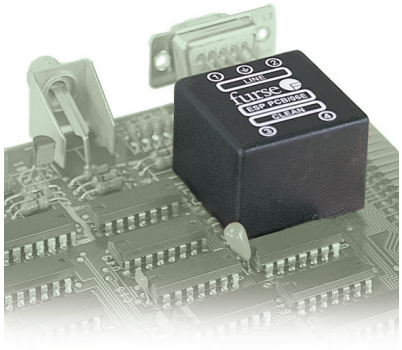
DATASHEET

Data and signal protection

ESP PCB/E Series



Combined Category D, C, B tested protector (to BS EN 61643) for 'through hole' mounting directly onto the PCB of data communication, signal or telephone equipment which require a lower in-line resistance, an increased current or a higher bandwidth than the PCB/D Series. Available for working voltages of up to 110 Volts for AC & DC power applications up to 1.25 Amps. For use at boundaries up to LPZ 0 to protect against flashover (typically the service entrance location) through to LPZ 3 to protect sensitive electronic equipment.**

Features & benefits

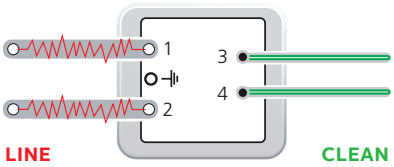
- Suitable for wave soldering
- Very low let-through voltage (enhanced protection to IEC/BS EN 62305) between all lines - Full Mode protection
- Full Mode design capable of handling partial lightning currents as well as allowing continual operation of protected equipment
- Repeated protection in lightning intense environments
- Very low (1 Ω) in-line resistance for resistance critical applications
- High (1.25 A) maximum running current
- Higher bandwidth enables higher frequency data communications
- 2 pin clean end and 3 pin line end to ensure correct insertion

Installation

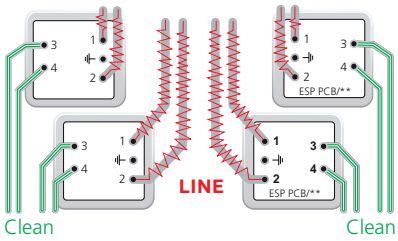
Connect in series, soldering pins direct onto PCB. Tracks to line and earth pins should be as wide as practical (see Furse Application Note AN003). Dirty (line) tracks should be routed parallel and as close together as possible. This should also be implemented on clean tracks, however clean tracks should never be routed close and parallel to line tracks or dirty barrier earth connections as earth connections as transients can be re-introduced after the protector due to electromagnetic coupling.

The use of an earth layer or plane is highly recommended as this reduces the electromagnetic field produced by a transient discharging to earth considerably, and hence the chance of the transient being picked up on clean tracks.

Maximum line to clean separation. Large input tracks and pads (using top and bottom copper layers). Earth pin is bonded to an earth layer/ plane.



All dirty (line) incoming tracks are separated from the clean output tracks, individual line and clean tracks are routed close together. Earth pins are bonded to an earth layer/plane.



ESP PCB/E Series - Technical specification

Electrical specification	**ESP PCB/06E**	**ESP PCB/15E**	**ESP PCB/30E**	**ESP PCB/50E**	**ESP PCB/110E**
ABB order code	7TCA085400R0039	7TCA085400R0153	7TCA085400R0043	7TCA085400R0156	7TCA085400R0041
Nominal voltage[1]	6 V	15 V	30 V	50 V	110 V
Maximum working voltage *Uc* (RMS/DC)[2]	5 V / 7.79 V	11 V / 16.7 V	25 V / 36.7 V	40 V / 56.7 V	93 V / 132 V
Current rating (signal)	1.25 A				
In-line resistance (per line ±10%)	1.0 Ω				
Bandwidth (-3 dB 50 Ω system)	45 MHz				
Transient specification	**ESP PCB/06E**	**ESP PCB/15E**	**ESP PCB/30E**	**ESP PCB/50E**	**ESP PCB/110E**
Let-through voltage (all conductors)[3] *Up*					
C2 test 4 kV 1.2/50 µs, 2 kA 8/20 µs to BS EN/EN/IEC 61643-21	36.0 V	39.0 V	60.0 V	86.0 V	180 V
C1 test 1 kV, 1.2/50 µs, 0.5 kA 8/20 µs to BS EN/EN/IEC 61643-21	26.2 V	28.0 V	49.0 V	73.5 V	170 V
B2 test 4 kV 10/700 µs to BS EN/EN/IEC 61643-21	16.0 V	25.5 V	43.5 V	65.0 V	160 V
5 kV, 10/700 µs[4]	17.0 V	26.2 V	44.3 V	65.8 V	165 V
Maximum surge current[5]					
D1 test 10/350 µs to BS EN/EN/IEC 61643-21: – Per signal wire	2.5 kA				
D1 test 10/350 µs to BS EN/EN/IEC 61643-21: – Per pair	5 kA				
8/20 µs to ITU-T K.45:2003, IEEE C62.41.2:2002: – Per signal wire	10 kA				
8/20 µs to ITU-T K.45:2003, IEEE C62.41.2:2002: – Per pair	20 kA				
Mechanical specification	**ESP PCB/E Series**				
Temperature range	-40 to +80 °C				
Connection type	0.64 mm (0.025”) square PCB pins, 1.2 mm diameter PCB holes recommended				
Case Material	FR Polymer UL-94 V-0				
Weight - Unit	0.035 kg				
Dimensions	See diagram below				

[1] Nominal voltage (RMS/DC or AC peak) measured at < 10 µA (ESP PCB/15E, ESP PCB/30E, ESP PCB/50E, ESP PCB/110E) and < 200 µA (ESP PCB/06E)

[2] Maximum working voltage (RMS/DC or AC peak) measured at < 5 mA leakage (ESP PCB/15E, ESP PCB/30E, ESP PCB/50E, ESP PCB/110E), < 10 mA (ESP PCB/06E)

[3] The maximum transient voltage let-through of the protector throughout the test (±10%), line to line & line to earth, both polarities. Response time < 10 ns

[4] Test to IEC 61000-4-5:2006, ITU-T (formerly CCITT) K.20, K.21 and K.45,Telcordia GR-1089-CORE, Issue 2:2002, ANSI TIA/EIA/IS-968-A:2002 (formerly FCC Part 68).

[5] The installation and connections external to the protector may limit the capability of the protector