Active short circuit capability of half-bridge power modules towards e-mobility applications

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Abstract

In this paper, a methodology to characterize active short circuit (ASC) in half-bridge power modules is demonstrated and utilized to determine the capability of the RoadPak module towards this failure mode in e-mobility applications.

First, a surge current test with increasing current, until the failure occurs, is performed on the modules and then replicated in a simulation environment to calculate which maximum junction temperature the chips inside the module can withstand. Then, an ASC event is simulated using a developed PLECS model to calculate the maximum temperature of the chips during the event, thus obtaining a pass-fail criterion for any specified currents.

1 Synopsis

The e-mobility market is on the rise, as society is concerned in finding a solution to avoid high consumption of fossil fuels. This interest towards a more sustainable mobility has pushed electric vehicles (EV) to play now an important role in the transport of individuals and/or goods. EV industry constantly in development must focus now in the safety of these vehicles. The safety in EVs involves not only the user's safety but also the drive system's safety. Improving the system's safety allows its components to survive possible failures, increasing their useful life and, indirectly, increasing the user's safety.

Most EVs use a three-phase permanent magnet synchronous motor (PMSM) [1] drive for propulsion. Such a system is mainly composed of a battery, a PMSM and a 3-phase inverter which comprises three half-bridge power modules. In order to ensure safe operation of the 3-phase inverter, the semiconductors used in the modules must be tested up to their thermal and mechanical limits. Knowing these limits, one can assess the potential of these devices towards the application and the capability to survive any failures which could occur during operation.

In this paper, the operation of a high current SiC MOSFET half-bridge module under high current conditions is demonstrated up to its thermal limit. The thermal limits of the SiC MOSFET chips under high current are discussed and a PLECS [2] model is developed in order to determine via simulation if the tested SiC MOSFET module would withstand an active short circuit current profile, such as the one expected during the operation of an EV inverter.

2 Active short circuit

Due to their high performance, PMSM motors are the most common chosen electrical drive system for an EV. This motor has very high-power density and efficiency, but the use of permanent magnets introduces the counter electromotive force (CEMF or back EMF), a voltage generated by the rotation of the motor. If the motor is rotating at very high speed, the high back EMF induced can be dangerous in the event of a fault (e.g. failure of the control).

The active short circuit [3] is a safety mode used in 3-phase PMSM inverter circuits, to protect the battery and the components of the vehicle in case of loss of control of the converter. It is typically used when the motor induced back EMF is higher than the battery DC voltage. This can occur when the motor operates in the field weakening region at speeds higher than the base speed and the control

of the motor is lost (e.g. due to an error). It can also be necessary if the battery has a problem or a fuse blows and the converter cannot transfer energy from/to the battery, then the converter must dissipate the energy stored in the motor to prevent it from being destroyed.

When the ASC is activated, the inverter is no longer modulated by the SVPWM algorithm and either the high side (Fig. 1) or the low side of the three half bridges is turned on with the rest of switches turned off. Thus, motor is short circuited and operates with a high current which depends on the characteristics of the motor and the actual current and speed [4]. This high current is briefly (in the range of ms) consumed by the modules and the motor until it is reduced and/or the rest of fail-safe measures are activated.

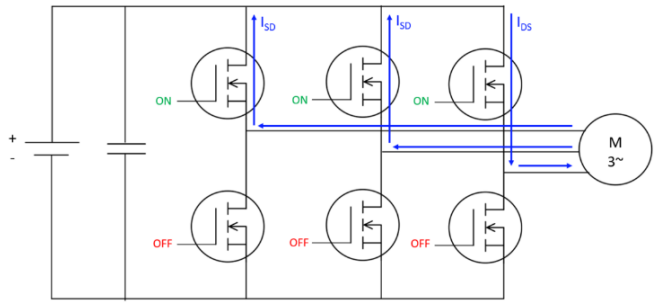

Fig. 1: 3-phase PMSM drive with ACS mode with only the high side (HS) of the inverter turned on.

During the time when the ASC mode is active, the motor is braking and thus it is operating as a generator. The energy of the motor is then essentially consumed exclusively on the semiconductors because they have the highest electrical resistance in the circuit, apart from the motor windings. Therefore, it is crucial that the capability of the modules to sustain such a current for the short period when the ASC mode is active is examined and validated to prevent the destruction of the modules due to overheating.

3 Surge current measurements on the RoadPak

The exact ASC conditions obtained on the power modules of the inverter of a PMSM drive during an ASC event are difficult to replicate in a laboratory because they depend on the motor and the operating conditions. For this reason, the approach used to test similar and representative conditions on the Hitachi ABB Power Grids RoadPak modules [5] (Fig. 2) has been to perform surge current measurements [6].

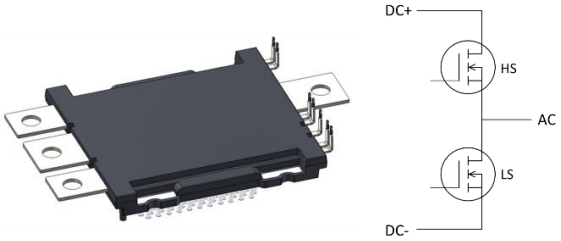

Fig. 2: RoadPak, high current SiC MOSFET half-bridge power module.

The surge current measurement consists in feeding one of the sides of the half-bridges modules with half sinusoidal current pulses of increasing magnitude until degradation is observed through: a shift of the on-state voltage (see example in Fig. 3) or dissipated energy comparing two (or more) consecutives pulses with the same amplitude and initial thermal conditions or an increase of the current leakage while performing a blocking measurement in between these consecutive pulses. Normally, the number of consecutive pulses with the same conditions is selected according to the expectation of the event occurring in the application. The current with magnitude lower than the degradation limits represents the capability of the module for the selected specific conditions.

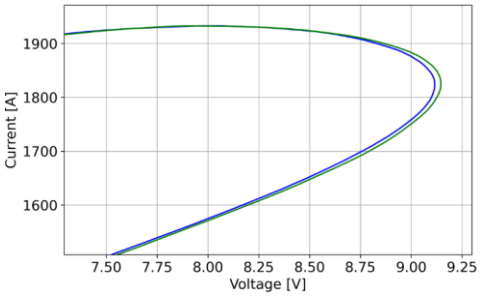

Fig. 3: Example of on-state shift, in green the second half sinusoidal current pulse shows an I-V curve with higher on-state voltage compared to the first pulse in blue with the same current conditions.

Two different designs of the RoadPak have been tested with the following boundary conditions: the baseplate of the module was kept at 175°C, the gate voltage was set to +15 V (chip recommended conditions), the measurement was performed both for drain-source (D-S) and for source-drain (S-D) and the half sinusoidal current pulse had a duration of 10 ms (equivalent to a 50 Hz AC frequency). Moreover, in between pulses a time of 1 min was

used to cool down and bring the module back to the original conditions and perform a blocking measurement to ensure current leakage was not increasing.

The results obtained on such a test for the RoadPak are presented in Table 1.

Module n°	1	1	2	3	4	4	5
Side	HS	LS	LS	HS	HS	LS	HS
Design	750V	750V	750V	750V	1.2kV	1.2kV	1.2kV
Current direction	D-S	D-S	D-S	S-D	D-S	D-S	S-D
Max. current pulse amplitude [A]	1939	2037	1825	>3000	1613	1609	>3000

Table 1: Results of the half sinusoidal current pulse test.

The results show that, for the SiC chips assembled in the RoadPak modules, the forward direction (D-S) has lower capability than the backward (S-D). Hence, the focus has been put on the D-S measurements as it would be the limiting point in case the ASC mode is activated in an EV drive. This is because in the S-D direction the body diode of the MOSFET is conducting in parallel with the channel, thus decreasing the on-state voltage and increasing the thermal capability of the device. Furthermore, the 750 V modules have higher current capability in comparison with the 1200 V modules due to the lower on-state resistance of the SiC paralleled chips assembled in the module.

By performing this test one can also assess how different technology designs affect the capability of the module towards high current unexpected events. The use of longer bond wires or with a material with higher electrical resistance would decrease the capability due to the heating generated on them, which at the same time is affecting the chips. The number of paralleled SiC MOSFET chips in each side of the module has also a big importance here, adding chips to a module means higher current capability but at the same time, if the module has the same size, the chips are closer between each other and then the heat spreading of a chip is affecting more the adjacent chips compared to a module with less chips.

4 Thermal simulation on surge current measurement results

In order to estimate the junction temperature on the RoadPak SiC MOSFETs during the surge current measurements, a thermal simulation which emulates the performed test has been developed using a Finite Element Method software for the 750V RoadPak design, more specifically for the module nº 1 HS included in Table 1.

In the simulation the on-state dissipated power (Fig. 4b) is applied on the junction of the SiC MOSFET chips in the stressed side of the module. This dissipated power is obtained by multiplying the on-state voltage measured and the half sinusoidal current profile applied during the surge current test (Fig. 4a).

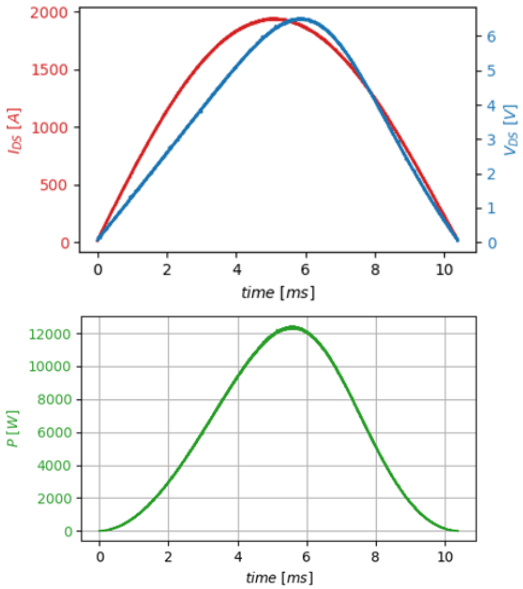

Fig. 4: a) Current profile I_{DS} (in red) and corresponding on-state voltage V_{DS} (in blue). b) Power dissipated profile (green).

The thermal simulation includes the bottom surface of the baseplate together with the pin fins (Fig. 5) set at 175°C, and then natural convection and radiation boundary conditions are considered for the module enclosure and terminal surfaces. As a simplification, the whole power dissipated during the test is divided by the number of chips on the tested module side and it is applied to the junction of these chips.

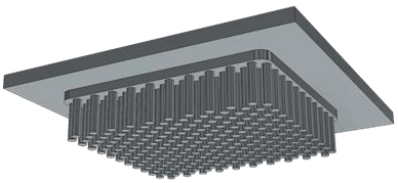

Fig. 5: Baseplate and pin fins of a RoadPak module.

The outcome of the simulation is the junction temperature profile (Fig. 6) expected for the half sinusoidal current pulse tested and simulated. Then, from this temperature profile it is possible to

obtain which is the absolute maximum junction temperature on the chips before any degradation occurs, in this case 325°C.

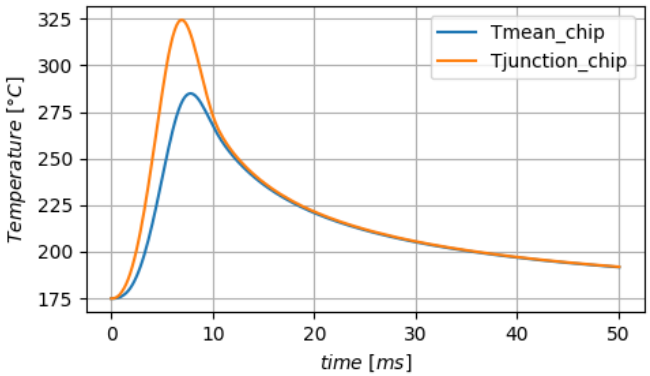

Fig. 6: Simulated temperature profiles obtained for the chip body (blue) and junction (orange).

The maximum junction temperature can be observed in Fig. 7, where a cross section of the module at around 7 ms, which is the moment with the highest junction temperature, shows that the small energy generated during the short pulse is kept in the chip for this short pulses and the rest of layers are almost not thermally affected.

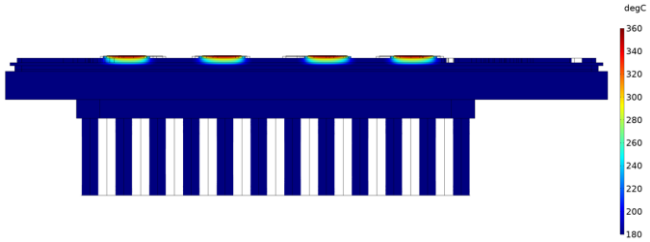

Fig. 7: Temperature contour from the thermal simulation of the surge current test at a cross-section of the RoadPak through the HS chips.

4.1 On-state voltage extrapolation on simulated temperatures

For the PLECS model developed in the following section it is required to use the temperature characterization of the drain-source and source-drain resistance, $R_{DS}(T_j)$ and $R_{SD}(T_j)$, of the RoadPak module.

The on-state resistance (R_{DS} and R_{SD}) of the RoadPak module has been measured at the range of 25°C to 175°C. Therefore, extrapolation is required for the simulated temperatures. To make sure this approach is valid for the model and similar current pulses, the temperature obtained in the thermal simulation has been used to calculate the on-state V_{DS} and verify obtained values using extrapolation at more than 300°C are equal to the measured values for these short pulses (Fig. 8).

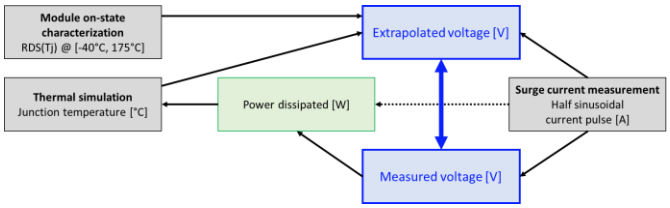

Fig. 8: Schematics of the approach followed to validate the extrapolation of the on-state voltage for higher temperatures than the characterized temperatures range.

The results show that extrapolating the on-state voltage down to 325°C using the fitted $R_{DS}(T_j)$ between 25°C and 175°C is a valid approach for similar current pulses. The voltage calculated using extrapolation on the $T_{junction\_chip}$ profile in Fig. 6 and the half sinusoidal current pulse of Fig. 5a) has almost the same value as the one measured during the test, only a difference of 3% can be observed in Fig. 9 at the peak voltage measured. The observed differences are most probably due to the slightly different cooling conditions between simulation and reality because the slight offset in the peak voltage is maintained until the chips have cooled down enough.

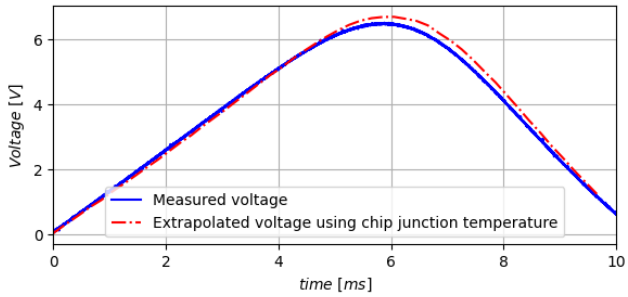

Fig. 9: Comparison between measured voltage on a surge current measurement (blue) and the calculated extrapolated voltage (red) by using the junction temperature profile obtained in FEM thermal simulation.

5 PLECS model

In order to determine the semiconductor's maximum junction temperature during an active short circuit, or a similar event with short current pulses, a PLECS model has been developed.

5.1 Methodology

The model included in Fig. 10 is mainly divided in two parts: the on-state characterization of the module and the thermal characterization of the module.

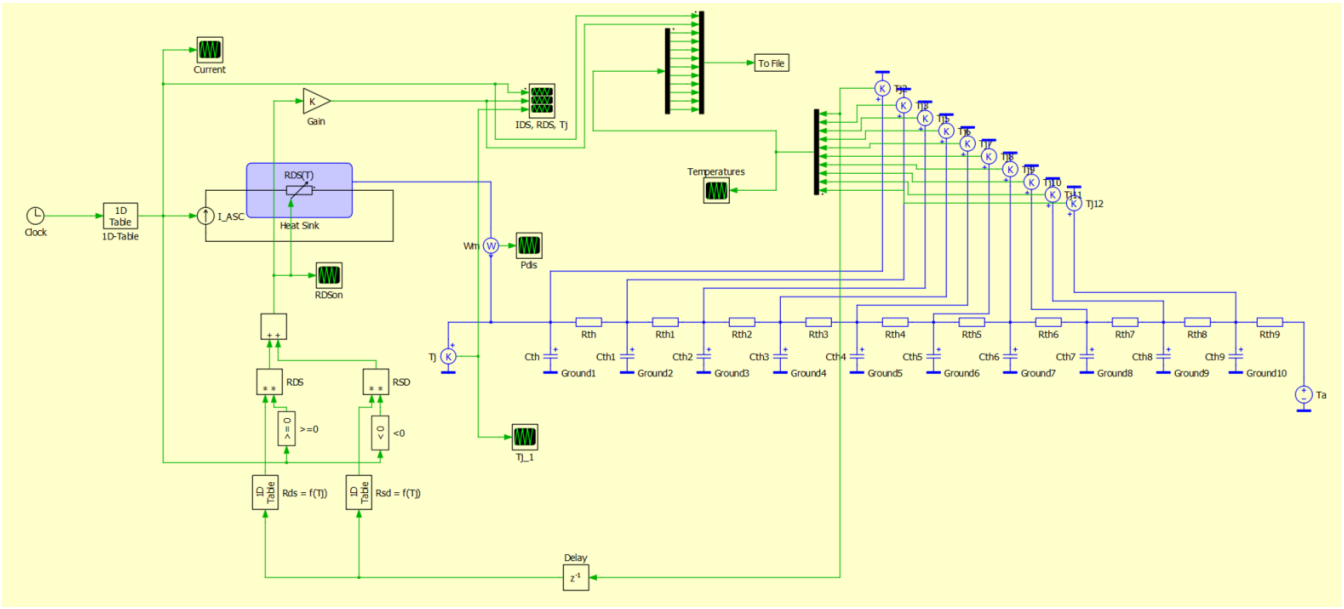

Fig. 10: PLECS model for active short circuit or surge current simulations.

5.1.1 On-state characterization

The module consists on the semiconductor represented as a variable resistor with respect to its temperature and the direction of the current (forward or reverse operation). A quadratic fitting on temperature in Eq. (1) and (2) has been used between -40°C and 175°C and then its extrapolation for higher temperatures has been validated in the section before.

$$R_{DS} = \mathrm{a}_{DS} \cdot T_j^2 + \mathrm{b}_{DS} \cdot T_j + \mathrm{c}_{DS} \qquad (1)$$

$$R_{SD} = \mathrm{a}_{SD} \cdot T_j^2 + \mathrm{b}_{SD} \cdot T_j + \mathrm{c}_{SD} \qquad (2)$$

A current source is used in the model to provide the current which allows to obtain the dissipated power during the high current event.

5.1.2 Thermal characterization

The transient thermal behavior of the module has been obtained by simulating a power step with constant amplitude applied on the junction of the semiconductors and studying the thermal behavior of the module and the cooler with certain cooling conditions.

On the simulation then, the transient average junction temperature can be expressed with Eq. (3), where the initial junction temperature, T_{vj0}, can also be the ambient temperature provided by the coolant.

$$T_{vj}(t) = T_{vj0} + Z_{th}(t) \cdot P \qquad (3)$$

Then the obtained thermal impedance can be represented with a Forster network of n R-C elements using Eq. (4), in the model a chain of ten elements has been selected to represent the different layers between the coolant and the semiconductors junction.

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \cdot \left(1 - e^{-t/\tau_i}\right) \qquad (4)$$

Where:

$$\tau_i = R_i \cdot C_i \qquad (5)$$

Then the obtained ten elements Foster network must be transformed to a Cauer network [7] where the capacitances are node-to-ground and where the heat-flow structure is represented via material layers. The Cauer network obtained is the one then used in the model.

The thermal behavior is better than the one simulated for the surge current measurements, here the module is cooled down with its own RoadPak cooler [8].

5.2 Simulation of an active short circuit using the developed PLECS model

The inputs of the model (Fig. 10) are the current profile expected and the initial conditions of junction temperature (T_j) and ambient temperature (T_a).

For simulating an active short circuit, one must provide to the model the current profile expected during such an event in application. This profile is

normally given by the PMSM drive manufacturer as it depends on the PMSM motor used and the main parameters defining the ASC are the current peak and the AC frequency.

In this case the current profile used is shown in Fig. 11. It has a peak current of almost 1800 A and an AC frequency of 50 Hz. After around 350 ms the current envelope has stabilized to a sinusoidal current with an I_{rms} value of approximately 550 A.

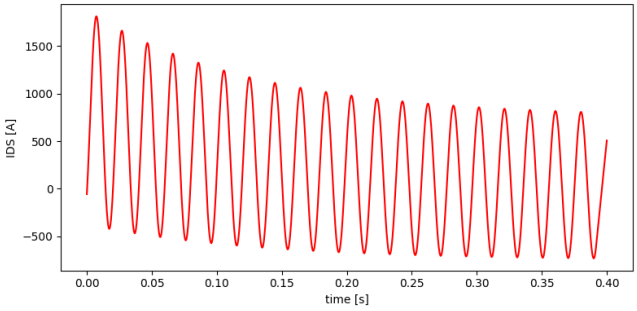

Fig. 11: Active short circuit current profile simulated using the PLECS model.

The output of the simulation is the temperature profile expected when running the ASC current profile in application, calculated at the semiconductor junction and all the module intermittent layers. Fig. 12 includes the junction temperature profile obtained on the RoadPak 750V design considering an initial junction temperature, T_{j0}, of 150°C and an ambient temperature, T_a, of 65°C.

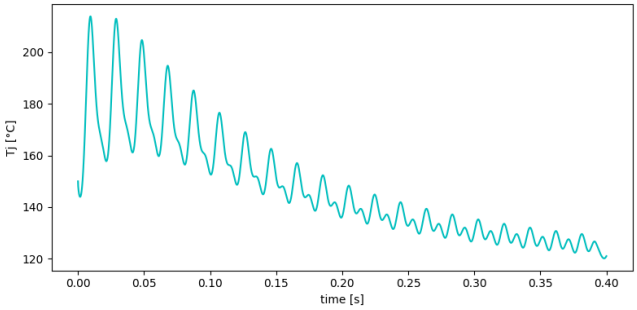

Fig. 12: Junction temperature profile obtained from the active short circuit simulation.

For the simulated current profile, the obtained maximum junction temperature (T_{j_max}) is 215°C, which is acceptable for the duration of the ASC event since T_{j_max} is lower, for a big margin, than the maximum allowed temperature of 325°C obtained in the thermal simulation of the surge current test. This can be used as an indication that the module will not fail during such an event in application.

6 Conclusions

A method for determining the capability of half-bridge power modules to withstand high current events, focused in active short circuit is proposed in this paper.

The methodology consists in finding the semiconductors junction thermal limits by doing high current tests on them (e.g. surge current test) and simulating the conditions of these tests in a FEM software to determine the maximum temperature the junction can withstand without observing any degradation or leakage on the power module.

Then a PLECS model has been developed to determine the semiconductors temperature in such events by simulating them and considering the thermal conditions expected in such event. Using the maximum temperature obtained from the FEM thermal simulation one can then consider if the semiconductors of the power module wouldn't suffer from the simulated events.

The surge current capability of two RoadPak designs is also included. The developed PLECS model is also used together with the thermal conditions of the RoadPak 750V in an e-mobility application to demonstrate this module would withstand an aggressive active short circuit current profile.

7 References

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