The Radial Layout Design Concept for the Bi-mode Insulated Gate Transistor

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***Abstract*—In this paper we present a new radial design concept for an optimized layout of anode shorts in the Bi-mode Insulating Gate Transistor (BiGT). The study shows that the arrangement of the n^+-stripes plays a key role for the on-state characteristics of the BiGT. With the aid of 3D device simulations the visualization of the plasma distribution during the on-state conduction was obtained in a 0.25 $\times$ 4 mm^2 large BiGT model area. The influence of the dimensioning and layout of the anode shorts was simulated and compared with measured on-state curves. A clear improvement of plasma distribution in the device when the stripes are arranged orthogonally (radially) to the pilot-IGBT boundary is observed in 3D simulations. Measurements confirm lower on-state losses as a result of better utilization of the device area.**

I. Introduction

Until recently, the use of reverse conductive (RC) IGBT devices has been limited to low voltage and/or soft switching applications with reduced diode requirements. With the introduction of the Bi-mode Insulated Gate Transistor (BiGT) [1], a new target to replace the high voltage IGBT - Free wheeling diode (FWD) pair in high power applications has been set. The BiGT device is expected to outperform the state of the art IGBT and diode in both soft and hard switching conditions, and fulfil rigorous robustness standards set on power devices today.

In a reverse conducting IGBT, alternating n^+-type doped areas are introduced into the collector contact, which act as a cathode contact in the internal diode conduction mode. The area ratio between the IGBT anode (p^+-areas) and the diode cathode (n^+-areas) determines which part of the collector area is available in IGBT and diode modes, respectively. During conduction of the body diode, p^+-areas are inactive and do not directly influence the diode performance. However, the n^+ areas act as anode shorts, strongly influencing the bipolar gain of the IGBT. During the design, trade-offs between the diode and IGBT modes must be carefully considered. One of the implications of anode shorting is the voltage snap-back, or negative resistance region in the device IGBT mode *I-V* characteristics. This effect could have a negative impact when devices are paralleled, especially at low temperature conditions. It has been shown that the initial snap-back can be controlled and eliminated by introducing a wide anode region, also called pilot-IGBT into the device [1], [2]. This resulted in a BiGT – a hybrid structure consisting of an RC-IGBT and a standard IGBT (Fig. 1). The sizing of the pilot-IGBT is an important design parameter determining the smooth on-set of the output characteristics with minimum snap-back. However, when the electron-hole plasma is built up in the pilot-IGBT area, only a small region of the BiGT is conductivity modulated. Further smooth and fast lateral expansion of the plasma towards the RC-IGBT region is crucial for strong conductivity modulation of the full device area and depends on the scaling, shape and arrangement of the anode shorts. For obtaining the largest possible diode to IGBT area ratio and widest anode areas simultaneously, stripe shaped anode shorts are utilized in the BiGT device. It has been demonstrated [2], [3] that stripe design might lead to secondary snap-backs in the *I-V* characteristics. In this work, we analyze in detail experimentally and by device simulation the influence of the shape and arrangement of the n^+-shorts on the trade-off between conduction losses of the BiGT in both diode and IGBT modes.

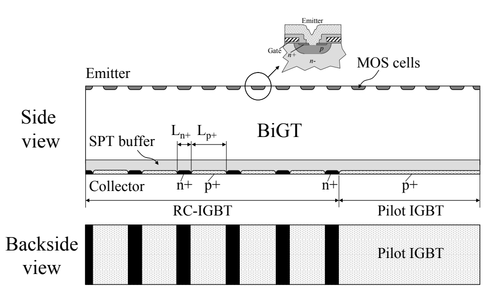

Fig. 1. Design features of the BiGT

II. Experiment and simulation setup

For the experiments we used 4500 V / 50 A Enhanced-Planar IGBT devices with anode shorts. Fig. 2 (a) shows the lithographic test-masks employed for the introduction of the n^+-shorts in the collector contact for the devices tested in this work. All the structures have identically sized pilot-IGBT regions, but different layout designs of the n^+-shorts. Structures S1, S2, S3 have stripe designs with different orientation of the stripes with respect to the pilot-IGBT area. The widths of the n^+ and p^+ regions (L_{n+} and L_{p+}, see Fig. 1) are 100 μm and 400 μm respectively, which results in an n area 25% of the total RC-IGBT collector contact area. Structures D1 and D2

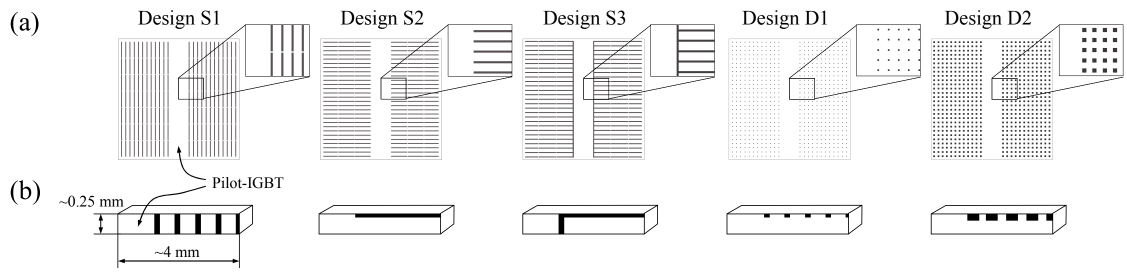

Fig. 2. Different anode shorts layouts of BiGTs. (a) lithographic test masks used to structure the anode: Stripes radial (S1), parallel (S2) and parallel-radial (S3); Dots matching n^+-stripe width L_{n+} (D1) and matching diode area (D2). (b) structures used in 3D device simulations to represent the above experimental layouts.

are designed with square dot shaped n^+-shorts. Structure D1 has the dot dimension equal to the n^+-stripe width in structures S1, S2, S3 (100 μm), while in the structure D2 the dots are sized to match the n area ratio to total collector area of 25% . Devices with different Soft Punch Through n buffers have been manufactured for comparison. The on-state characteristics of the BiGTs were measured in diode and IGBT mode. A gate voltage of +15 V was applied during both IGBT and diode measurements.

To explain the experimental findings, device simulations were performed for the anode patterns shown in Fig. 2 (a). Except for design S1, all other variants can only be modelled in a 3D-mode. As a basis, a 3.3 kV Enhanced-Planar IGBT structure was utilized for quasi-stationary simulations in the IGBT mode. Large device structures with detailed layout of the anode and n^+-shorts measuring up to 0.25 mm $\times$ 4 mm were simulated in order to provide a realistic representation of the BiGT concept including a sufficiently large IGBT-pilot region. With the aim to reduce the number of mesh points, the MOS cell structure was replaced by a continuous n-contact to represent the forward conduction of the BiGT. On the device collector side, the n^+ diffusions (anode shorts) were introduced. Structures showing the collector side layouts used in the simulations are presented in Fig. 2 (b). When mirrored, they closely resemble the experimentally verified structures.

III. Results and discussion

A. *Influence of the different n^+-stripe layouts*

Initially, stripe designs S1, S2 and S3 were compared. Fig. 3 shows the measured *I-V* characteristics of the three above designs. The difference between the designs can be close to 1 V at nominal (50 A) current, depending on the n buffer used. When the n^+-stripes are placed parallel to the boundary between the pilot-IGBT and RC-IGBT (design S1), the on-state voltage drop is the highest for the same current flowing in the device, whereas the orthogonally (radially) arranged stripes (design S2) yield the lowest on-state voltage drop values. Also, there are small but clearly visible secondary snap-backs at low currents in the parallel stripe (S1) design while in the case of orthogonal stripe design the *I-V* curve is completely smooth. Diode characteristics of both structures are overlapping and do not show any dependency on the stripe layout. The design with orthogonal stripes with an n^+-stripe running along the boundary of the pilot-IGBT area (design S3, Fig. 2) has features of both designs: high on-state voltage drop at low currents similar to the S1 design, and low losses similar to the S2 design at high currents.

To visualize the carrier plasma spread in the device, 3D device simulations were performed. The carrier density was extracted in the collector plane 30 μm above the contact. Fig. 4 shows a comparison of the simulated carrier density evolution for the S1, S2 and S3 designs. For all designs, at low current densities the electron-hole plasma is predominantly concentrated in the pilot-IGBT area. Further lateral expansion of the plasma strongly depends on the n^+-shorts layout. In the parallel stripes design (S1) case, the injection from the anode segments starts in a step-like manner as each anode segment becomes forward biased. When the stripes are placed orthogonally to the pilot-IGBT boundary, the injection from the anode stripes is initiated at a much lower current density. It starts at the position closest to the pilot-IGBT and smoothly extends towards the device periphery. It is important that for the same current, the device area filled with plasma is larger in the S2 design, giving lower on-state voltage drop and better current distribution compared to the parallel stripe (S1) design for the same n^+-shorts dimensions. Due to the low buffer doping applied in the simulations, the enhanced plasma spread

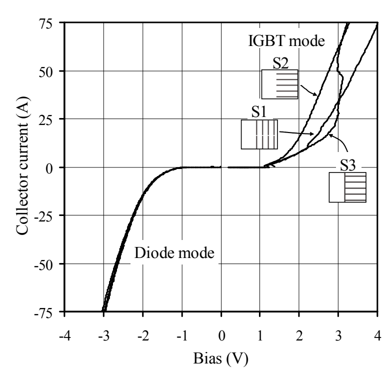

Fig. 3. Measured on-state *I-V* characteristics of BiGTs with different stripe orientation.

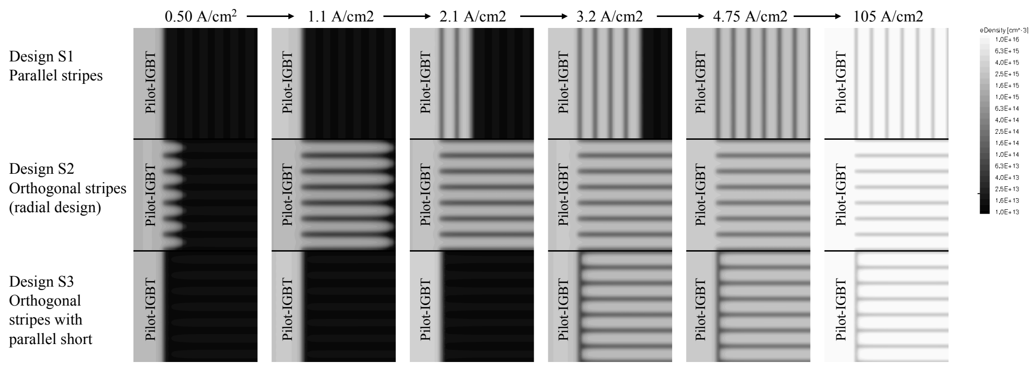

Fig. 4. Evolution of the simulated carrier density 30 μm above the anode contact during the current rise in the BiGTs with different backside n^{+}-stripe layouts. n^{+}-shorts ratio to full collector area is 25%, and pilot-IGBT size is maintained between designs.

effect is observed at significantly lower currents compared to the measurements.

In the case of design S3 the end of the anode stripe closest to the pilot-IGBT is shorted, which prevents forward biasing of the anode stripes and smooth expansion of the plasma seen in the orthogonal S2 design. The hole injection from the anode stripe starts at a higher current density in the middle of the stripe and almost instantly fills the whole device area with plasma, yielding at high current an identical *I-V* curve to the radial design S2.

We attribute the above phenomenon to the different direction of the lateral current in respect to the anode stripes. For all designs, the plasma is confined to the pilot-IGBT initially and the device current flow is directed vertically and laterally, towards the pilot-IGBT. In case when the n^{+}-stripes are placed parallel to the pilot-IGBT boundary, lateral current flows perpendicular to the anode segments and the voltage drop across the anode segment is small due to the limited non-shorted anode segment width L_{p+} available. Therefore, a high device current is required to forward bias the anode segments in the RC-IGBT region. Injection from each anode segment is visible in the *I-V* characteristics as a small secondary snap-back (see Fig. 3, design S1). This effect has been treated using 2D device simulations as well as analytical models [2]–[5] . Orthogonal (radial) placement of the n^{+}-stripes is a complex case and can no longer be treated in 2D. On the one hand, the anode stripe is now oriented along the lateral current flow and provides its full length for the forward biasing to be achieved. At the same time, the anode stripe is shorted along both sides. Evidently, this arrangement enables smooth transition from the pilot-IGBT towards the periphery of the device without negative resistance regions due to the early injection from the anode stripe at the point of connection to the pilot-IGBT (Fig. 4, compare 1.1 A/cm^{2} plasma distribution between the designs). If this position is shorted as in design S3 (Fig. 2), injection from the anode stripe occurs in the middle of the stripe, which in this case is the point of highest potential difference. However, the required current is much higher as compared to design S2, therefore, up to 3.2 A, the current has to concentrate in the pilot-IGBT area and then quickly spreads to the whole device area.

B. Comparison with a square dots pattern

It is interesting to see if a dot shaped n^{+}-shorts can bring further advantage to the best performing radial stripe design S2. Similar to the radial n^{+}-stripes design, dotted patterns also have long continuous p^{+}-doped anode regions along the lateral current direction. If the dots have the same dimension as the n^{+}-stripe (compare designs D1 and S2, Fig. 2) and the distance between the p^{+}-dots is equal to the width L_{p+} of the anode stripes in design S2, this inevitably reduces the diode contact area. To compensate for this, either the dot pitch or the dot size has to be adjusted, as done in design D2 (Fig. 2). Fig. 5 shows the comparison of the *I-V* characteristics in IGBT and diode mode for the stripe and dot designs. While the D1 design has slightly lower on-state voltage in the IGBT mode due to less shorting of the anode, the diode mode suffers from high conduction losses, as the diode contact area is reduced by 80%. Design D2 has the same diode mode conduction losses as for the stripe designs which is expected from the same diode contact area. However, the anode p^{+} spacing between the dots is smaller by 25%, which is the cause for slightly higher losses in IGBT mode. 3D simulations in Fig. 6 also

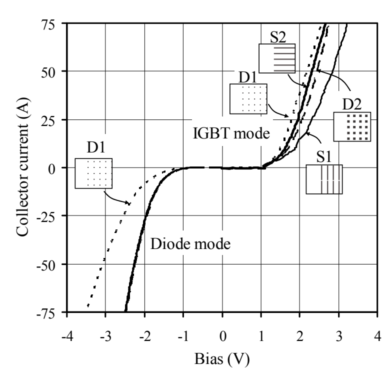

Fig. 5. Comparison of on-state *I-V* characteristics of BiGT devices with n^{+}-stripe and n^{+}-dot designs

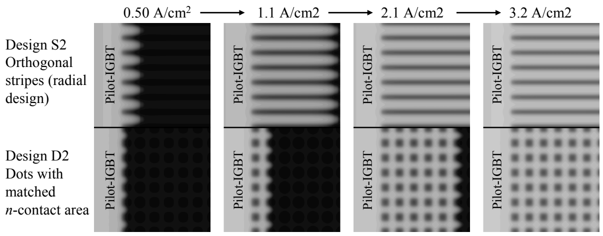

Fig. 6. Comparison of the simulated carrier density 30 μm above the collector contact during the current rise in the BiGTs with backside n^+-stripe and square n^+-dots designs.

confirm that less of the device area is filled with plasma in the D2 design, compared to S2. It is clear that radially arranged n^+-stripes achieve better trade-off between diode and IGBT on-state losses.

C. Influence of the n buffer

The resistivity of the *n* buffer determines the lateral voltage drop required for forward biasing the anode segments, as reported in [2], [3]. Therefore, a higher resistivity (or lower doped) buffer is preferred to initiate the injection from the anode segments at low currents. However, adjustment of the buffer affects other design parameters such as the leakage current. Fig. 7 shows the *I-V* characteristics of the parallel stripe (S1) and radial stripe (S2) designs, measured on samples with different buffer doping concentrations. The change in buffer design increases the on-state losses at the nominal current from 2.8 V to 4.5 V for the parallel n^+-stripe (S1) design. In addition, secondary snap-backs become very prominent with the increase of the buffer doping. Radial n^+-stripe design (S2) has much lower sensitivity to the buffer and changes the on-state voltage drop from 2.4 V to 3.3 V for the same buffer modifications. The weaker sensitivity to the *n* buffer doping opens additional flexibility in the design which is important for optimizing the device for high temperature operation.

D. Switching characteristics

Switching characteristics were measured for the samples with parallel stripe (S1) and radial stripe (S2) designs at

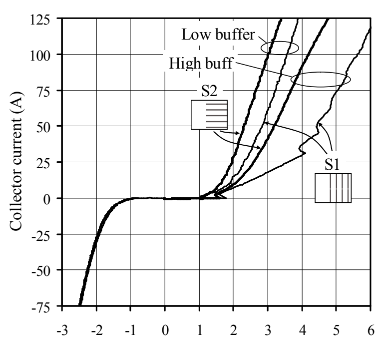

Fig. 7. Influence of *n* buffer doping on the on-state *I-V* characteristics of BiGT devices with different layout of the n^+-stripes

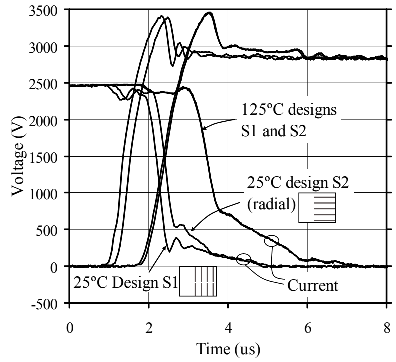

Fig. 8. Measured turn-off characteristics of BiGTs with different orientation of the stripes. Switching conditions 2800 V 50 A, $L_\sigma = 4400$ nH

nominal voltage and current (2800 V, 50 A), as shown in Fig. 8. Only a small difference in the current tail at room temperature is visible as a result of the different carrier density distribution. The higher and more evenly distributed plasma in the radial design provides additional carriers for the softer turn-off at low temperatures. At 125 °C, the waveforms become indistinguishable from each other.

IV. Conclusions

We have presented a comparison between the different layout designs of the anode n^+-shorts for the optimization of the BiGT. The investigation shows that the choice of shape and arrangement of the n^+-shorts determines the on-state conduction losses of the BiGT in IGBT mode. With the aid of 3D device simulations it has been demonstrated that the radial n^+-shorts stripes significantly improve the plasma spread in the device. Measurements confirm lower on-state losses as a result of better utilization of the device area. Square dot shaped n^+-shorts also offer good plasma spread in the device, but have a worse trade-off between diode and IGBT on-state losses. The radial n^+-stripe design of the anode shorts achieves the best diode and IGBT conduction losses trade-off and is the optimum design for the BiGT.

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References

[1] M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell, S. Klaka, *The Bi-mode Insulated Gate Transistor (BiGT) A potential technology for higher power applications*, Proc. ISPSD09, p 283, 2009.

[2] L. Storasta, A. Kopta, M. Rahimo, *A comparison of charge dynamics in the Reverse-Conducting RC IGBT and Bi-mode Insulated Gate Transistor BiGT*, Proc. ISPSD10, p.283, 2010.

[3] U. R. Vemulapati, N. Kaminski, L. Storasta, M. Rahimo, *Springende Kennlinien in rückwärtsleitenden IGBTs*, HL-Kolloquium Freiburg, 08-09. November 2010.

[4] A. Bourennane, J-L. Sanchez, F. Richardeau, E. Imbernon, M. Breil, *On the integration of a PIN diode and an IGBT for a specific application* Proc. ISPS06, Czech Rep., p 145, 2006.

[5] M. Gärtner, D. Vietzke, D. Reznik, M. Stoisiek, K.-G. Oppermann, W. Gerlach, *Bistability and hysteresis in the characteristics of segmented anode lateral IGBTs*, IEEE Trans. Electron. Dev., vol. 45, pp. 1575-1579, July 1998.