

V_{DRM}	=	4200 V
$I_{T(AV)M}$	=	500 A
$I_{T(RMS)}$	=	785 A
I_{TSM}	=	$7.1 \cdot 10^3$ A
V_{T0}	=	1.14 V
r_T	=	1.288 m Ω

Phase Control Thyristor

5STP 04D4200

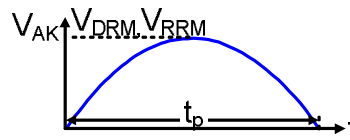
Doc. No. 5SYA1025-09 May. 20

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	5STP 04D4200	Unit
Max repetitive peak forward and reverse blocking voltage	V_{DRM} , V_{RRM}	$f = 50$ Hz, $t_p = 10$ ms, $T_{vj} = 5 \dots 125$ °C, Note 1	4200	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to $0.67 \cdot V_{DRM}$, $T_{vj} = 125$ °C	1000	V/ μ s



Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	V_{DRM} , $T_{vj} = 125$ °C			100	mA
Reverse leakage current	I_{RRM}	V_{RRM} , $T_{vj} = 125$ °C			100	mA

Note 1: Voltage de-rating factor of 0.11% per °C is applicable for T_{vj} below +5 °C.

Mechanical data

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		8	10	12	kN
Acceleration	a	Device unclamped			50	m/s ²
Acceleration	a	Device clamped			100	m/s ²

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				0.3	kg
Housing thickness	H	$F_M = 10$ kN, $T_a = 25$ °C	25.89		26.54	mm
Surface creepage distance	D_s		25			mm
Air strike distance	D_a		14			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

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On-state

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, $T_c = 70\text{ °C}$			500	A
RMS on-state current	$I_{T(RMS)}$				785	A
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 125\text{ °C}$, sine half wave,			$7.1 \cdot 10^3$	A
Limiting load integral	I^2t	$V_D = V_R = 0\text{ V}$, after surge			$252.1 \cdot 10^3$	A ² s
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 125\text{ °C}$, sine half wave,			$5.9 \cdot 10^3$	A
Limiting load integral	I^2t	$V_R = 0.6 \cdot V_{RRM}$, after surge			$174.1 \cdot 10^3$	A ² s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	$I_T = 500\text{ A}$, $T_{vj} = 125\text{ °C}$		1.63	1.78	V
Threshold voltage	$V_{(TO)}$	$I_T = 300\text{ A} - 1000\text{ A}$, $T_{vj} = 125\text{ °C}$			1.14	V
Slope resistance	r_T				1.288	mΩ
Holding current	I_H	$T_{vj} = 25\text{ °C}$			75	mA
		$T_{vj} = 125\text{ °C}$			60	mA
Latching current	I_L	$T_{vj} = 25\text{ °C}$			500	mA
		$T_{vj} = 125\text{ °C}$			200	mA

Switching

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_{vj} = 125\text{ °C}$, $I_T = 1500\text{ A}$, $V_D \leq 0.67 \cdot V_{DRM}$,			100	A/μs
		$I_{GM} = 2\text{ A}$, $t_r = 0.5\text{ μs}$	Cont. $f = 50\text{ Hz}$		1000	A/μs
Circuit-commutated turn-off time	t_q	$T_{vj} = 125\text{ °C}$, $I_T = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A/μs}$, $V_D \leq 0.67 \cdot V_{DRM}$, $dV_D/dt = 20\text{ V/μs}$			600	μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	$T_{vj} = 125\text{ °C}$, $I_T = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A/μs}$	450	1150	1400	μAs
Reverse recovery current	I_{RM}		25	37	40	A
Gate turn-on delay time	t_{gd}	$T_{vj} = 25\text{ °C}$, $V_D = 0.4 \cdot V_{RM}$, $I_{GM} = 2\text{ A}$, $t_r = 0.5\text{ μs}$			3	μs

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V _{FGM}				12	V
Peak forward gate current	I _{FGM}				10	A
Peak reverse gate voltage	V _{RGM}				10	V
Average gate power loss	P _{G(AV)}		see Fig. 7			W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V _{GT}	T _{vj} = 25 °C			2.6	V
Gate-trigger current	I _{GT}	T _{vj} = 25 °C			400	mA
Gate non-trigger voltage	V _{GD}	V _D = 0.4·V _{DRM} , T _{vjmax} = 125 °C			0.3	V
Gate non-trigger current	I _{GD}	V _D = 0.4·V _{DRM} , T _{vjmax} = 125 °C			10	mA

Thermal

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T _{vj}				125	°C
Storage temperature range	T _{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	R _{th(j-c)}	Double-side cooled F _m = 8... 12 kN			36	K/kW
	R _{th(j-c)A}	Anode-side cooled F _m = 8... 12 kN			70	K/kW
	R _{th(j-c)C}	Cathode-side cooled F _m = 8... 12 kN			74	K/kW
Thermal resistance case to heatsink	R _{th(c-h)}	Double-side cooled F _m = 8... 12 kN			7.5	K/kW
	R _{th(c-h)}	Single-side cooled F _m = 8... 12 kN			15	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R _i (K/kW)	20.440	10.524	4.138	0.897
τ _i (s)	0.4451	0.0485	0.0049	0.0013

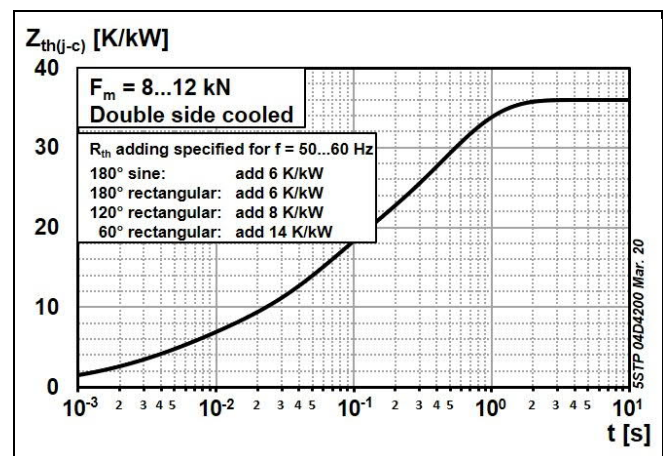


Fig. 1 Transient thermal impedance (junction-to-case) vs. time

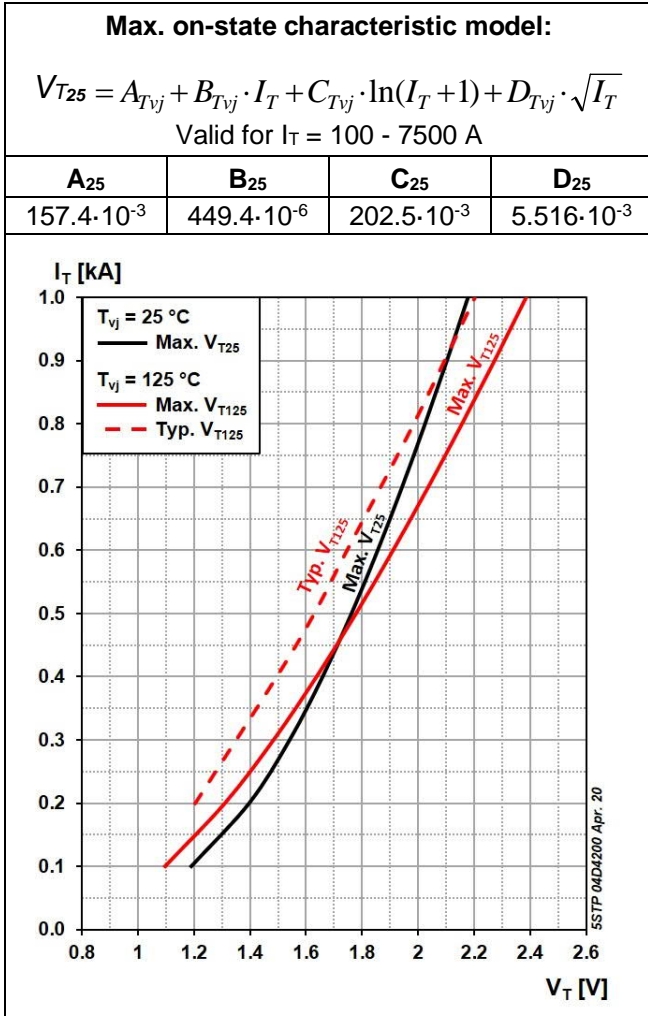


Fig. 2 On-state voltage characteristics

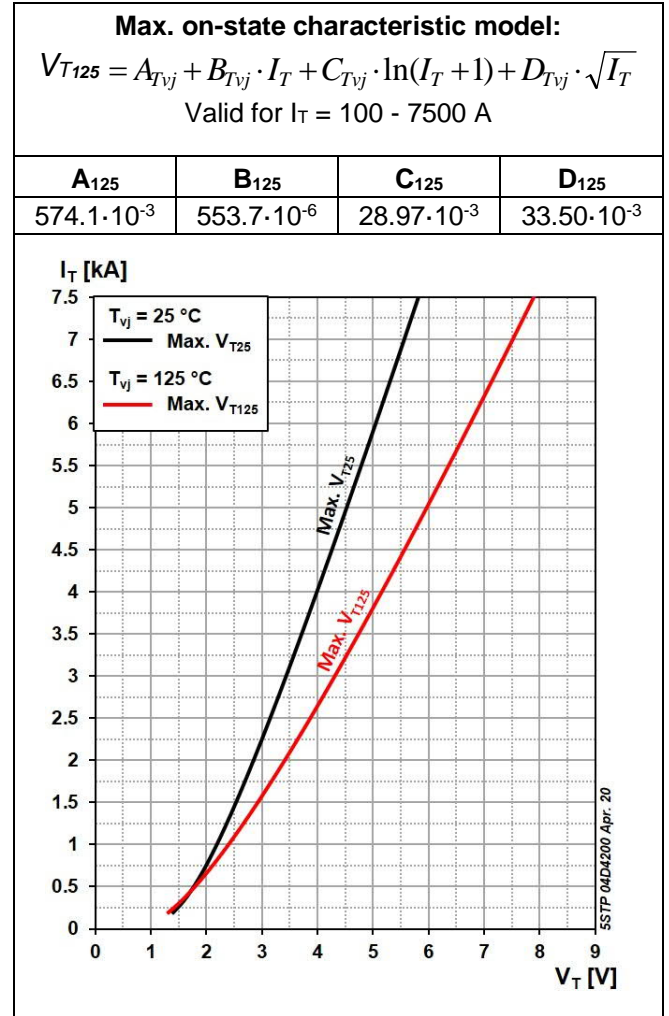


Fig. 3 On-state voltage characteristics

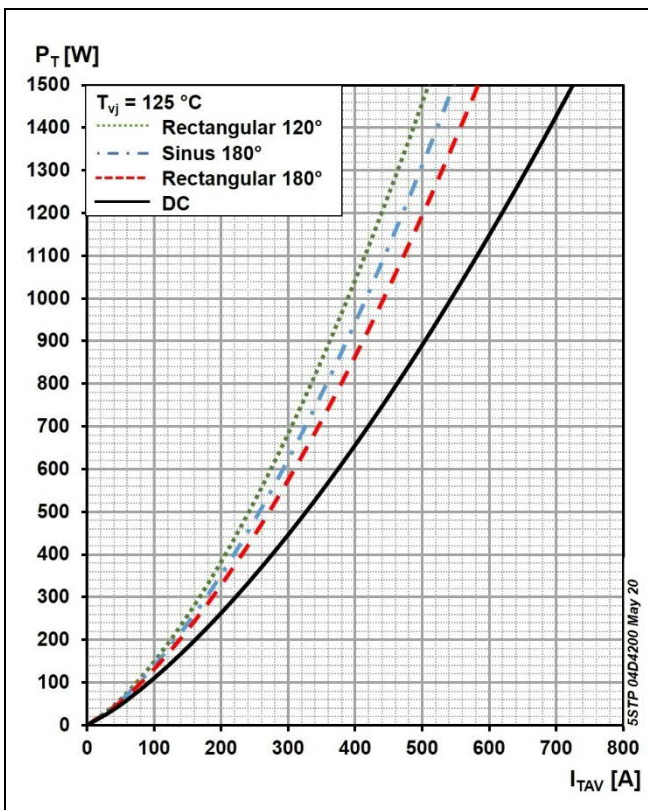


Fig. 4 On-state power dissipation vs. mean on-state current, turn-on losses excluded

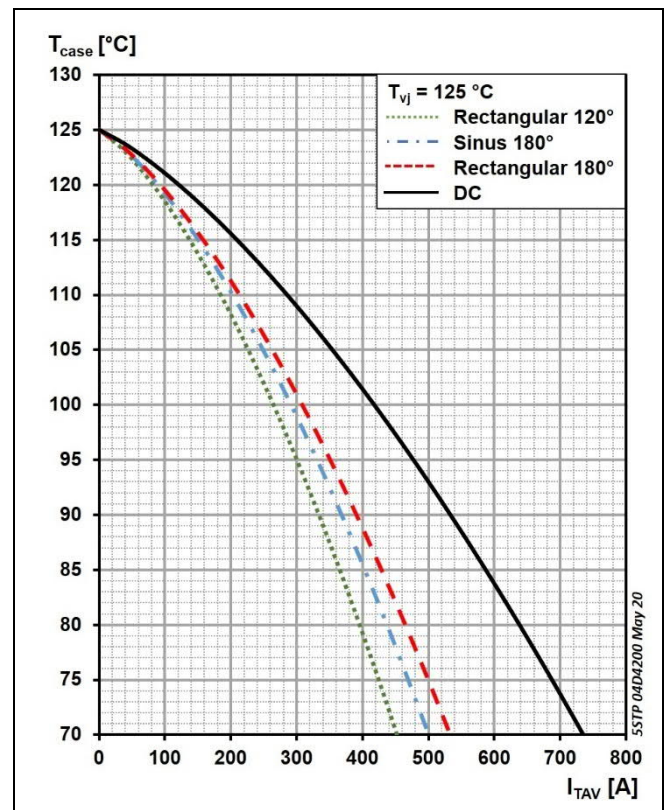


Fig. 5 Max. permissible case temperature vs. mean on-state current, switching losses ignored



Fig. 6 Recommended gate current waveform

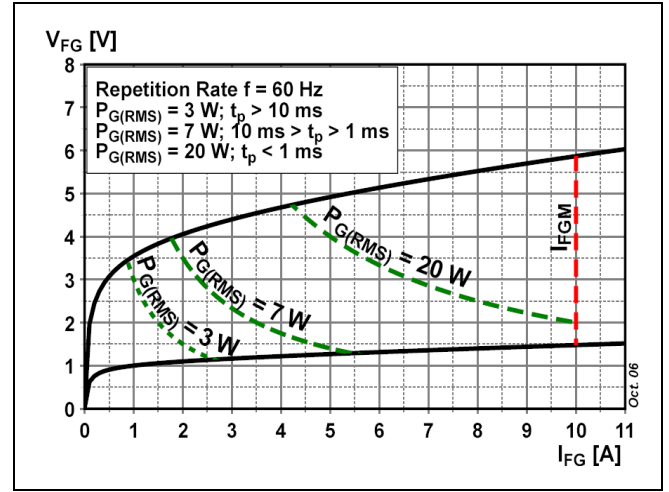


Fig. 7 Max. peak gate power loss

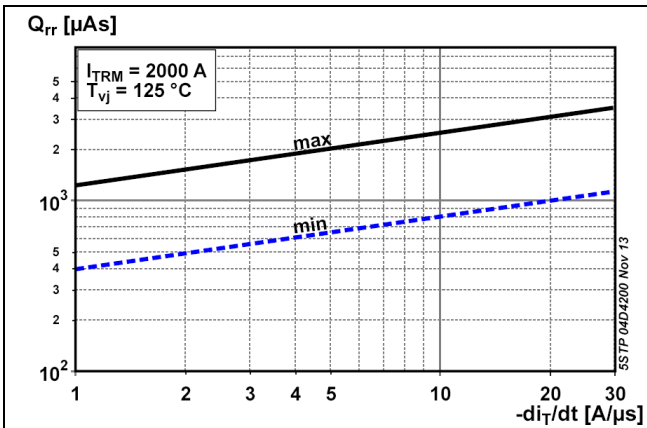


Fig. 8 Reverse recovery charge vs. decay rate of on-state current

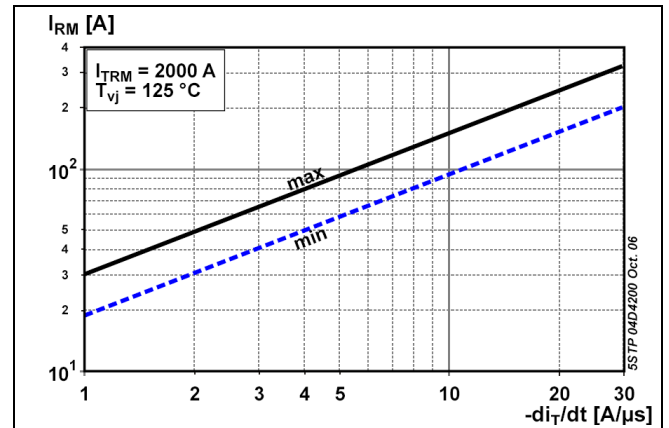


Fig. 9 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

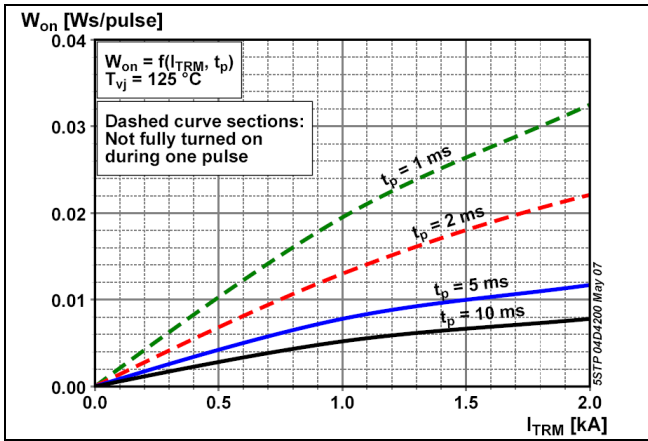


Fig. 10 Turn-on energy, half sinusoidal waves

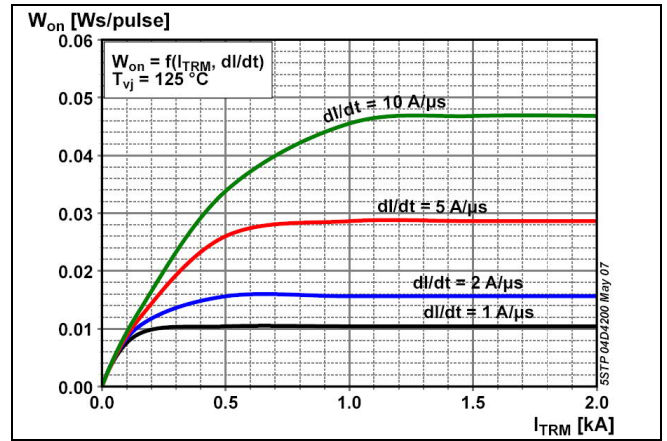


Fig. 11 Turn-on energy, rectangular waves

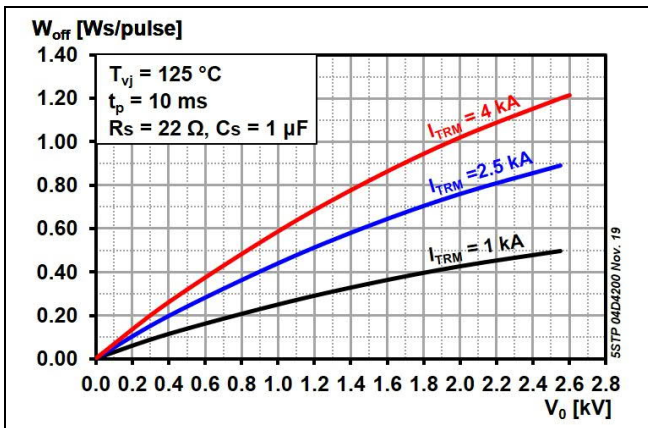


Fig. 12 Typical turn-off energy, half sinusoidal waves

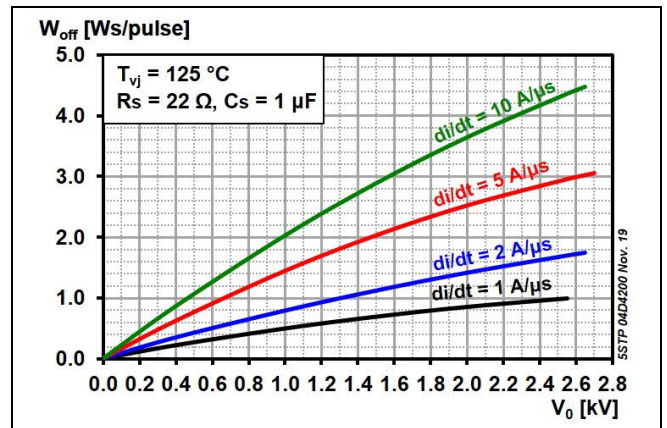


Fig. 13 Typical turn-off energy, rectangular waves

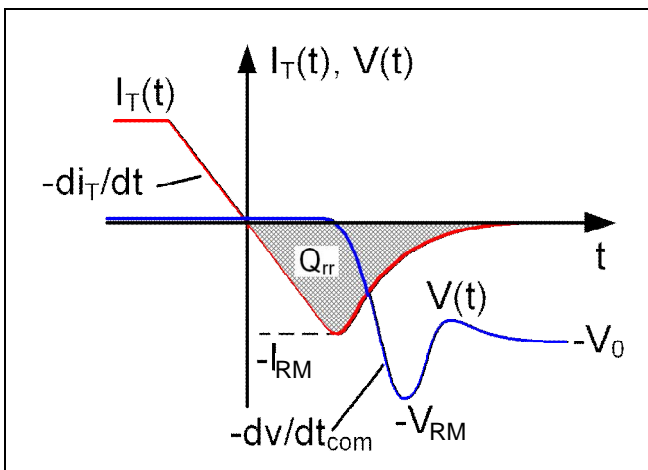


Fig. 14 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T} \int_0^T I_T \cdot V_T(I_T) dt$$

Fig. 15 Relationships for power loss

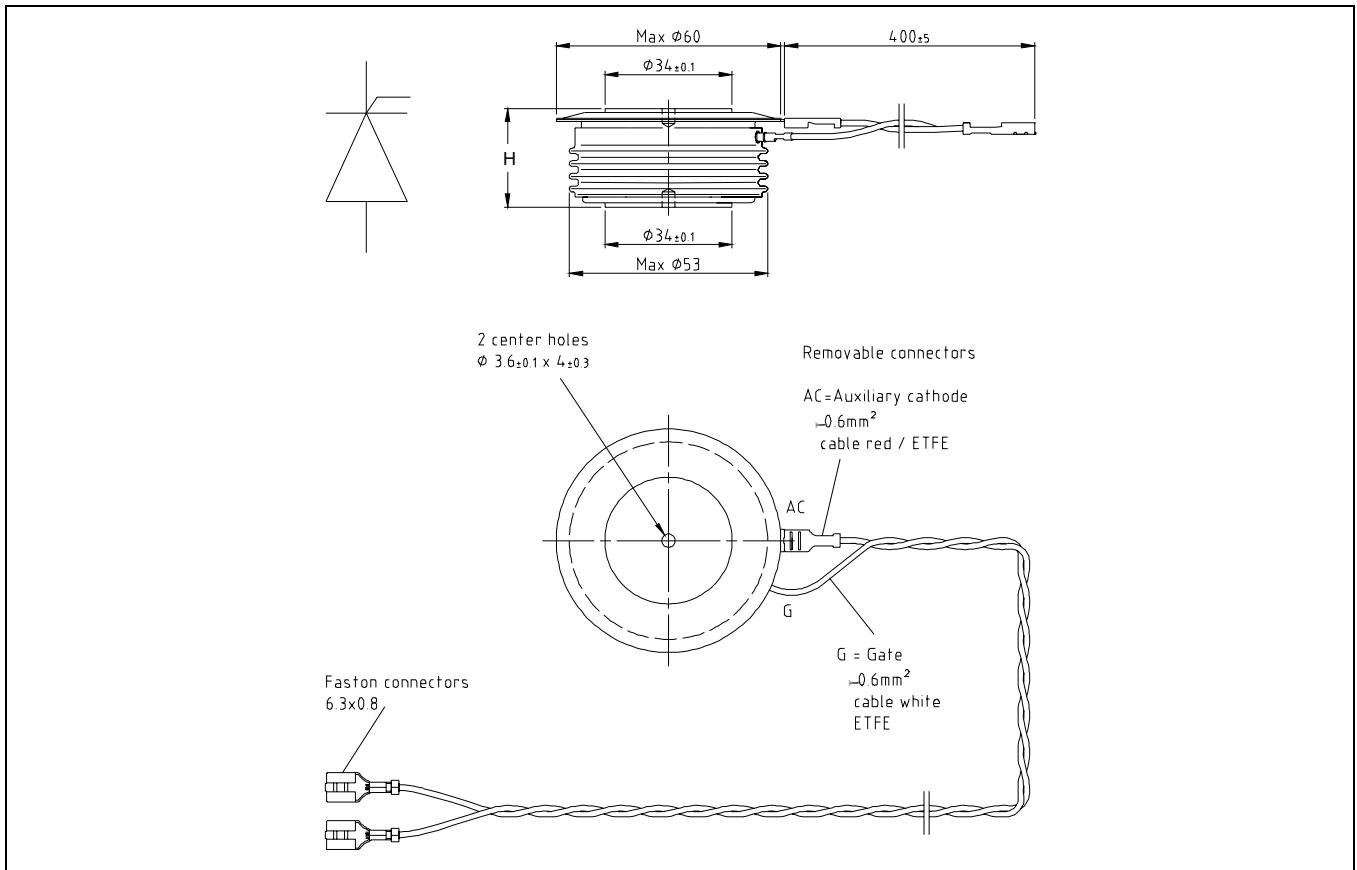


Fig. 16 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubbers for Phase Control Applications
5SYA 2049	Voltage definitions for phase control and bi-directionally controlled thyristors
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-drive recommendations for phase control and bi-directionally controlled thyristors
5SYA 2036	Recommendations regarding mechanical clamping of Press-Pack High Power Semiconductors
5SZK 9118	General Environmental Conditions for High Power Semiconductors

Please refer to <http://www.abb.com/semiconductors> for current version of documents.

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