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Optimization of Parameters influencing the Maximum Controllable Current in Gate Commutated Thyristors

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Abstract

The model of interconnected numerical device segments can give a prediction on the dynamic performance of large area full wafer devices such as the GCTs and can be used as an optimization tool for designing GCTs. In this paper we evaluate the relative importance of the shallow p-base thickness, its peak concentration, the depth of the p-base and the buffer peak concentration.

Keywords: Integrated Gate Commutated Thyristors, GCT, Optimization.

INTRODUCTION

The Integrated Gate Commutated Thyristors (IGCTs) feature the most competitive trade-offs in the very high power range of the Power Semiconductor Device spectrum. At high current densities, they offer robustness, excellent reliability, low conduction losses and large utilization of silicon area [1]. IGCTs also meet the device requirements of high-power converters for DC distribution systems which will be required to handle an increasing share of renewable power [2]. An increase in the power handling capability would mean a significant reduction in the cost of power conversion in large renewable power generation sites such as offshore wind-farms. For achieving this there are three requirements which need to be met concomitantly (i) reduction of losses (switching and on-state), (ii) increase of the current handling capability and (iii) high temperature operation. The reduction in the on-state power losses was recently addressed through the introduction of the Punch Through concept and the transparent anode [3] whereas the latest reported improvement in the current handling capability with high temperature operation was reported in [4]. This paper focuses on the relative importance of various optimization techniques and how they impact on the on-state (VT) and the maximum controllable current (MCC).

Fig. 1 depicts a typical Gate Commutated Thyristor (GCT) wafer with 91mm diameter. It consists of more than 2700 long and narrow cathode fingers surrounded by a gate metalization. These cathode fingers are distributed in concentric rings (10 in our case) and the gate metalization in the area between the fingers of ring 5 and ring 6 makes the annular gate conduct terminal of the device. They are conducted together by the pole pieces of the press pack housing. An IGCT is the result of the combination of the GCT with its Gate Unit (GU).

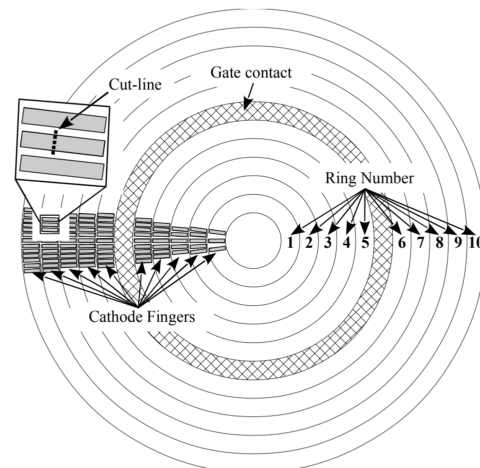


Fig. 1: A 91mm diameter wafer GCT wafer with more than 2700 cathode fingers operating in parallel.

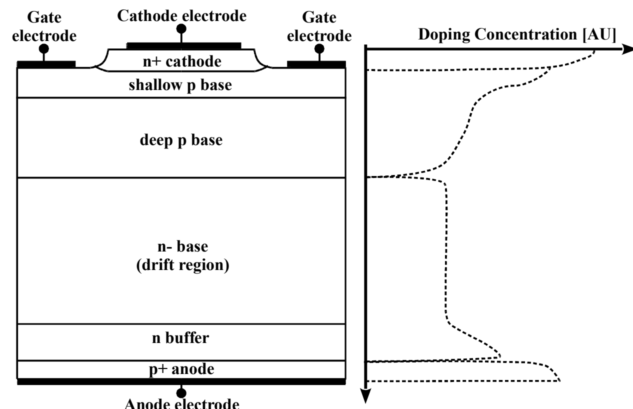
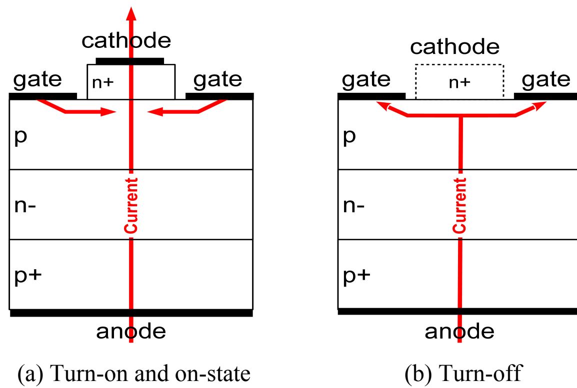


Fig. 2: The structure of one cell across the cut-line in Fig.1. with the doping characteristic shape on the right.

Principle of Operation

The principle of operation is diagrammatically shown in Fig. 3.

Turn-on. In order to turn on (latch) the device (Fig. 3a) a forward gate current pulse is provided by the GU similarly to the Thyristor and GTO. The injected holes in the p-base layer forward bias the cathode emitter junction. Electrons now injected from the cathode induce the injection of holes from the p+ anode emitter. The device quickly enters the on state regime which is characterized by the double injection of carriers (electrons from the cathode and holes from the anode) and heavy carrier modulation, a distinctive operation of thyristor devices.



(a) Turn-on and on-state (b) Turn-off

Fig. 3: The principle of operation

Turn-off. The turn-off procedure in GCTs (Fig. 3b) is very different to the GTO or the classical Thyristor. The turn-off procedure starts with the application of negative voltage on the gate with respect to the cathode. This voltage is very close to the reverse breakdown of the junction, usually about 20-25V. The whole anode current is then quickly (less than 2us) commutated into the gate from the cathode which in turn stops emitting almost instantaneously while a thin depletion region is formed along the cathode/p-base junction. The current commutation has to be completed before the device starts supporting any voltage that is when the space charge reaches the main blocking junction (p-base/n-base junction). The device is then converted into an open base transistor and the turn-off process continues without any regenerative action taking place. The transistor turn-off is much more uniform, no current crowding is occurred, the formation of hot-spots (previously common in GTOs) are eliminated and the snubbers are now obsolete. In GTOs the cathodes continue to emit throughout the turn-off process and the device has to be protected from parasitic re-triggering.

In order to achieve such a fast commutation (hard drive) a nearly unity gain GU is required. Thus the maximum stray gate inductance has to be maintained to lower than 5nH, an achievement of the integration of the GU with the semiconductor wafer device.

METHODOLOGY, RESULTS AND DISCUSSION

The turn-off process and the failure in large area full wafer devices such as the GCT is difficult to be reproduced in simulations. The reasons behind this are the nature of the turn-off, the dimensions and the geometry of the device. During conduction, thousands of amperes are distributed over the entire wafer device, with thousands of parallel operating thyristor cells conducting. At the onset of turn-off the whole current has to be commutated via the gate metalization that surrounds the cathode segments to the single gate annular conduct within less than 2μs.

Previous studies on GCTs have shown that the inductive loading in the wafer is not uniformly distributed. It has been found that sections of the device closer to the gate contact experience lower inductance during turn-off compared to those farther from it. The impedance loading along a radial line extending from the center of the wafer was reported in [8]. This imbalance strongly perturbates the turn-off procedure thus in order to reproduce the behavior of the GCT in dynamic conditions, the interaction between adjoining regions in the wafer has to be taken into account. Furthermore the parasitic inductance and resistance loading of the gate metalization has to be considered in correlation with the geometrical features of the wafer. Inevitably during turn-off there is a large current redistribution in the wafer, thus a good model of the GCT needs to feature all those requirements and distinctive characteristics of the device in order to make a good prediction of the MCC.

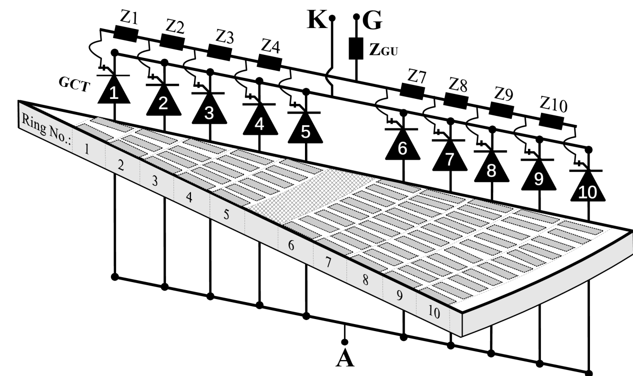


Fig. 4: The GCT model used for turn-off simulations. It consists of ten individual numerical structures of distributed area (GCT1, GCT2, … GCT10) interconnected with a network of SPICE resistances and inductances. Z1, Z2, ... Z10 represent the gate metalization impedance loading of the GCTs lying in different rings.

Methodology

Fig. 4 illustrates the model approach of the GCT as used for this study. Indeed it is a mixed mode representation with a combination of numerical devices and SPICE components. The GCTs indicated in this figure are in fact two dimensional numerical structures (Fig. 2) which represent each one of the ten rings of cathodes that can be found in a typical wafer GCT (Fig. 1). Every one of them has been given the approximate active area of the equivalent ring it represents. The electrical coupling of the silicon is simulated by a network of SPICE interconnections which also embeds the impedance loading distribution along the wafer (inductive and resistive).

The inductance values used in this model are those reported in [8] whereas the resistance distribution has been evaluated by direct calculation. These values are summarized in Table 1. The model was build with the Synopsys package. Similar models of interconnected perturbed 2D numerical devices have been proposed in [6] and [7].

GCT	Impedance (Z)		Active Area
	R [mΩ]	L [nH]	[%]
1	0.64	0.46	3.5
2	0.88	0.62	4.2
3	0.10	0.73	5.5
4	1.16	1.54	6.8
5	-	-	8.2
6	-	-	11.8
7	1.50	0.77	13
8	1.55	0.42	14
9	1.59	0.34	16
10	1.63	0.34	17
GU	1.30	2.15	-

Table 1: Model specific values of the impedance and the active area of every ring

The SPICE representation of the external circuit used for dynamic simulations with the mixed mode model of interconnected perturbed numerical GCT segments is shown in Fig. 5. This is a representation of the circuit of standard applications i.e. inverter circuits or choppers. It has a di/dt and over-voltage clamp but no dV/dt snubbers. This has been used to asses various cell designs in terms of their on-state and turn-off capability.

The optimization parameters are the thickness of the shallow p-base, its peak concentration, the thickness of the deep p-base and the buffer peak concentration. The determination of the maximum turn-off current requires many mixed mode simulations in consequence of the fact that one simulation can only predict whether the device was able to switch off or not. First the DC link voltage (V_D) is fixed to the normal working voltage of 2800V and the temperature (T_J) to 400K. The circuit components are kept constant and the device is set to turn off a certain current. Every successful turn-off is followed by another turn-off simulation of increased current until a failure to do so is recorded.

Successful turn-off. For this paper, a turn-off is considered to be successful when the anode current reduces to the blocking leakage value right after the tail phase.

Failure to turn-off. The GCT is considered to have failed to turn off when during the anode voltage rise period one or more cathode fingers start conducting more than 10% of the on-state anode current value.

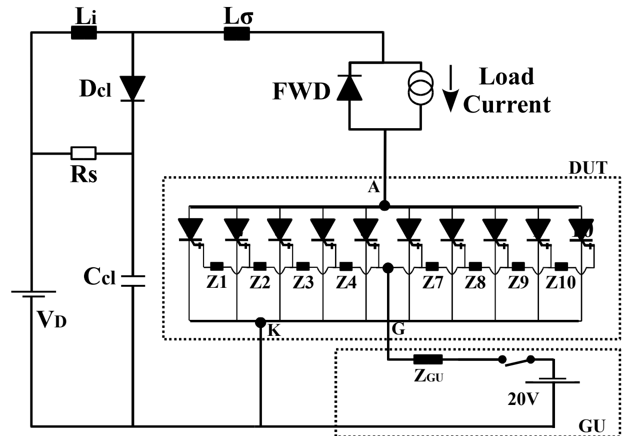


Fig. 5. Graphical representation of the complete circuit as used for the turn-off simulations. Li (di/dt limiting inductor) = 2μH, Ccl (clamp capacitor) = 10μF, Lσ (clamp parasitic inductor)=0.3μH

Results

The simulated forward conduction characteristics of a reference GCT (Ref.) design is shown in Fig. 6 whereas the turn-off waveforms are shown in Fig 7.

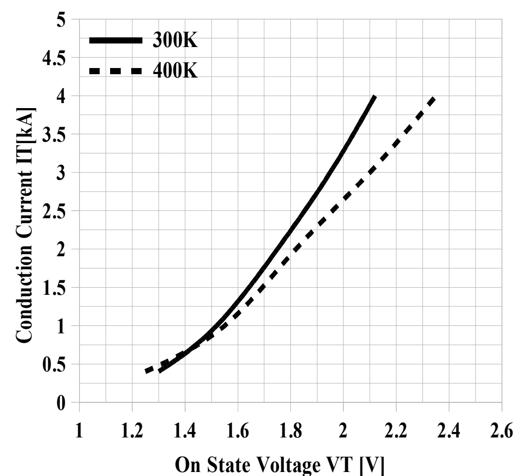
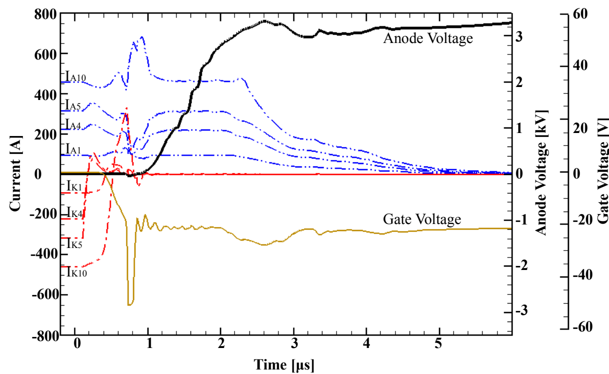
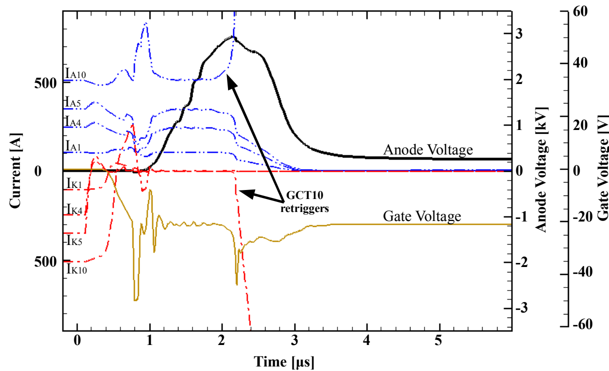


Fig. 6: Simulated on-state characteristics of the reference structure in Fig. 2.

In the on-state, the conduction current is shared among the 10 GCT segments of the model according to their active area. The negative gate voltage on the gate terminal initiates the turn-off process but as clearly demonstrated in Fig. 7a, the current commutation is much slower for the GCT segments that lie farther from the gate conduct (GCTs in ring 10 and ring 1). Nevertheless it is completed before any significant voltage is supported on the anode which is the first requirement for a successful turn-off, the Hard Drive requirement. At this point all the n+ emitters are isolated and the anode voltage ramp phase follows. The presence of high electric field with high conduction current induces carrier generation by dynamic avalanche. This reduces the rate of voltage rise, identified in the voltage anode waveform by the characteristic “knee” at the onset of change of the rate. Throughout this phase there is a current shift from the region of the wafer that is closer to the gate contact to the farthest silicon area, rings 1 and 10. This can be explained by the fact that these regions have had their regions depleted slower at the initial moments of the turn-off, thus they form a more preferable path for the current. When the anode voltage reaches the DC-link voltage (V_D), the current starts to redirect in the FWD, thus the conduction current starts to reduce. This is the beginning of the current fall phase.



(a) Successful turn-off waveform at I_{LOAD}=2700A, V_D=2800V

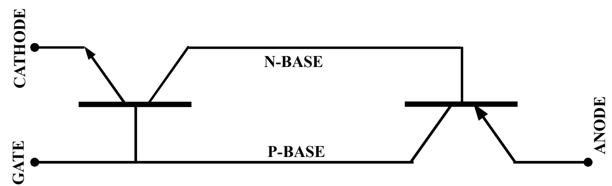


(b) Turn-off failure waveform at I_{LOAD}=3000A, V_D=2800V

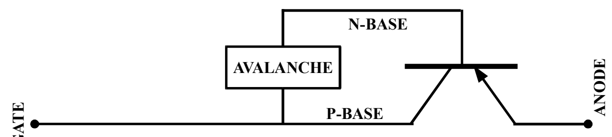
Fig. 7. Successful and turn-off failure waveforms for the Ref. design at T_J=400K.

When the conduction current is increased to a value outside the controllable range, the device fails to turn off. The waveform for the failure turn-off for the Ref. design is depicted in Fig. 7b.

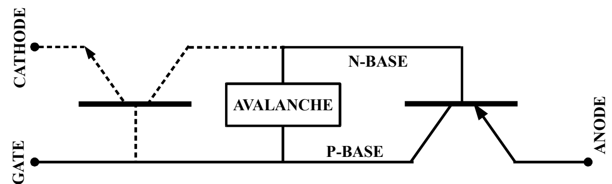
The carrier ionization in the depletion region serves as the base current of the p-n-p transistor that remains active until the end of the turn-off. This positive feedback current gain mechanism (Fig. 8b) is always more intense in the remotest regions of the wafer which leads to a localized increase in the current share. At the onset of turn-off failure, the current flowing beneath one or more cathode fingers (which also serves for the base current of the n-p-n transistor) becomes enough to trigger the thyristor regenerative action. The combined transistor-transistor and avalanche-transistor positive feedback mechanism (Fig. 8c) creates a local highly conductive path (depicted in Fig. 9) which leads to the failure.



(a) Transistor-transistor current gain – Active during on-state



(b) Avalanche-transistor current gain – Active during turn-off



(c) Combined transistor-transistor and avalanche-transistor current gain – Active at the onset of turn-off failure.

Fig. 8. The current gain positive feedback mechanisms in GCTs

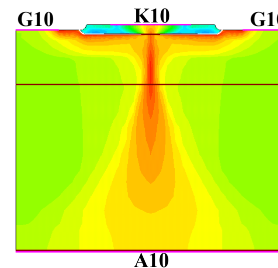


Fig. 9. At the onset of failure, the current density in the 10th ring (GCT10)

An optimized GCT doping design can survive the current gain mechanisms described above up to a higher current level, it leads to high ruggedness wafer devices with high current controllability. The collective results of the trade-off (optimization) curves for the turn-off capability in terms of the conduction voltage drop are shown in Fig. 10. All cell designs are compared against the reference design (marked as Ref. in Fig. 10).

Buffer peak concentration. The n-buffer peak concentration strongly affects the efficiency and the transparency of the anode. The simulations have shown that by increasing the peak concentration from $1x10^{16}cm^{-3}$ to $5x10^{16}cm^{-3}$ or $1x10^{17}cm^{-3}$ the hole current in the device reduces which improves the Maximum Controllable Current but strongly deteriorates the conduction. The improvement in the turn-off capability arises from the reduction of the p-n-p transistor action in the avalanche transistor current gain mechanism. As shown in Fig. 11b, the plasma concentration in the device is reduced dramatically in the proximity of the anode which results to an increased voltage drop during conduction. The simulations have shown that the peak buffer concentration should not exceed $5x10^{16}cm^{-3}$.

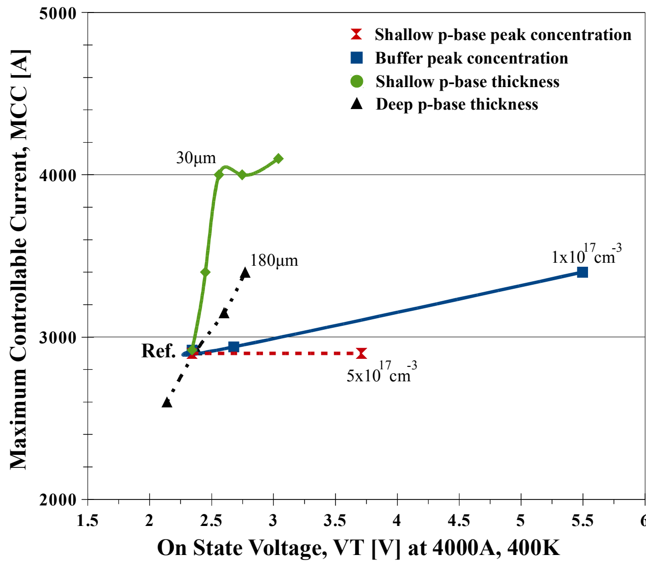
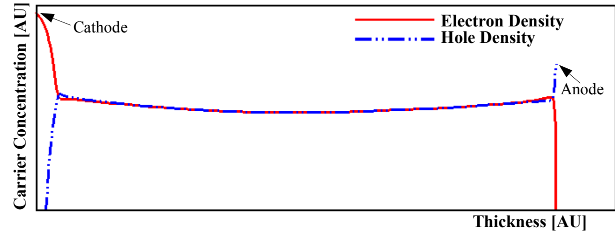
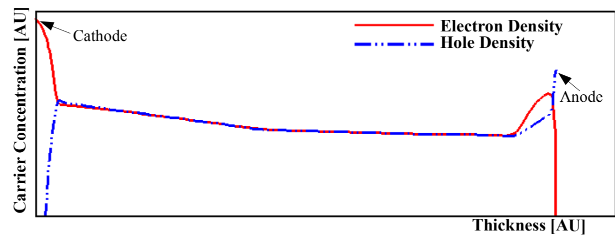


Fig. 10: Optimization curves – Last pass turn-off current as a function of the on state voltage drop at 4000A, 400K.
Ref.: On-state characteristics shown in Fig. 6, shallow p-base of 20µm thickness and $1x10^{17}cm^{-3}$ peak concentration, 140µm deep p-base thickness and $1x10^{16}cm^{-3}$ buffer peak concentration.

Shallow p-base thickness. This is the most effective optimization parameter. The shallow p-base is a narrow layer of Gaussian profile with $1x10^{17}cm^{-3}$ peak boron concentration. Its thickness strongly affects the collection of hole current during turn-off. This effectively reduces the susceptibility of the n-p-n transistor to the latch-up. It hence increases the current level at which the combined current gain mechanism strikes up. When it becomes too wide however, it starts inhibiting the injection of electrons from the n+ cathode and deteriorates the n-p-n transistor action in the transistor-transistor current gain mechanism. Hence the performance of the device deteriorates in the on-state without any further considerable increase in the MCC. The simulations have shown that the optimum thickness of this layer is about 30µm. At this thickness, the increase of the conduction voltage at 400K, 4000A is only 0.2V (8%) whereas the increase in the turn-off capability is about 1100V (38%).



(a) Ref.



(b) Buffer peak concentration $1x10^{17}cm^{-3}$

Fig. 11. Electron and hole distribution along a vertical line starting from the middle of the cathode of the numerical GCT representing ring 10 at 2700A, 400K.

Shallow p-base peak concentration. The peak concentration of boron in the p-base strongly affects the n-p-n transistor action of the transistor-transistor current gain. It gives an increased on-state voltage without any improvement in the MCC. As shown in Fig. 10, the MCC remains virtually unchanged when the shallow p-base peak boron concentration is increased from $1x10^{17}$cm-3 to $5x10^{17}cm^{-3}$.

Deep p-base thickness. The p-base depth gives a more preferable relationship between MCC and VT compared to the buffer and the shallow p-base concentration but inferior to that of the shallow p-base thickness. The augmentation in the MCC comes from the simultaneous deterioration of the avalanche generation and the reduced susceptibility of the n-p-n transistor to the latch-up. A bigger p-base region means smoother electric field distribution and reduced carrier ionization. Furthermore by bringing the main blocking junction farther from the cathode/p-base junction, the lateral hole current density underneath the cathode junction reduces. This in turn

weakens the exposure of the n-p-n equivalent transistor to the hole current; a higher current is required for the latch-up. The on-state performance degradation comes from the enlargement of the current path and hence the sheet resistance of the device as well as the deterioration of the n-p-n transistor action.

Discussion

The doping profile strongly affects the maximum current one device can safely switch off but the impact of different parameters on the final failure varies. The simulations have shown that the best trade-off comes from *minimizing the effect* of the transistor-avalanche couple on the transistor-transistor current gain mechanism. This approach can increase the maximum current required before a failure can be recorded while avoiding the direct influence of the conduction modulation in the on-state. The best approach towards achieving this is the enlargement of the shallow p-base thickness up to a maximum of 30μm. Beyond this value, the layer starts interfering with the transistor-transistor current gain mechanism which is responsible for the low conduction losses in the on-state.

For this study we have chosen to use a two dimensional approach to model the three-dimensional nature of the turn-off. A three-dimensional model for full wafer devices has only recently been introduced [9]. Such a model is expected to give more accurate prediction of the absolute value of the MCC compared to the two-dimensional counterpart. This is because a full wafer 3D model takes into consideration all the geometrical and physical features of the wafer and it can capture current and space charge traveling via silicon. A 3D wafer level model however is beyond the needs of this work. As a matter of fact the 2D model is considered suitable for this study in the interest of capturing the turn-off failure and the MCC/VT reliance on the described doping parameters. Of notable importance also is the modest memory and processing requirement of this model which is indispensable in MCC studies due to the large number of simulations required.

CONCLUSIONS

Increasing the maximum turn-off current it would mean an increased power handling capability from one single device. This can be achieved by optimizing the parameters that influence the turn-off process, i.e. those who increase the current capability of the device without compromising the on-state performance. Even though simulation packages are really good on predicting the behavior of semiconductor devices, capturing the turn-off capability and turn-off failure in such a large area full wafer device is impossible without a good model. The mixed mode model of interconnected 2D numerical GCTs of distributed active area can capture the turn-off failure. It can hence be used as an optimization tool for designing GCTs. Indeed it has been found that the parameter with the strongest effect on the turn-off capability is the thickness of the shallow p-base. It can have up to 38% improved current controllability without sacrificing more than 8% in the on-state .

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