HIGH PERFORMANCE DIFFERENTIAL PROTECTION, ANALOG VERSUS NUMERICAL

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ABSTRACT

For bus zone protection applications, it is extremely important to have good security since an unwanted operation might have severe consequences. The unwanted operation of the bus differential relay will have the similar effect as simultaneous faults on all power system elements connected to the bus. On the other hand, the relay has to be dependable as well. Failure to operate or even slow operation of the differential relay, in case of an actual internal fault, can have fatal consequences. Human injuries, power system blackout, transient instability or considerable damage to the surrounding substation equipment and the close-by generators are some of the possible outcomes. These two main requirements are contradictory to each other in nature. To design the differential relay to satisfy these two requirements at the same time is not an easy task. The analog relays have been successfully used for these types of applications for years. Can their numerical counterparts offer the same performance?

INTRODUCTION

The bus zone protection has experienced several decades of changes. It is fair to say that the first introduction of bus zone protection in Europe started in Britain as early as 1904. This was known as the circulating current Merz-Price system [7]. Later, in the beginning of the 1940s, the high impedance differential protection scheme was introduced [1]. One of the main features of the high impedance differential scheme is that it permits the faulty line current transformer (CT) to be fully saturated in the event of a severe external fault and still keep the stability. However, in order to fulfil this requirement, it demands that all current transformers connected to one protection zone have to have the same ratio and magnetizing characteristics.

As a result of the requirements from central Europe to cope with different CT ratios within one protection zone, the percentage restrained differential protection scheme, based on a special analog circuit, was developed in the late 1960s [2].

Although successful in practice, both of the above mentioned analog differential relays have some shortcomings such as the need for auxiliary CTs to match the different CT ratios, the lack of self-supervision, secondary CT switching for double or multiple busbar arrangements and relatively complicated scheme engineering.

The first generation of digital differential bus zone protection was developed in order to fulfil these additional requirements. However, these new relays could not match the performance of the analog relays regarding the speed of operation. The demands on the main current transformers were as well much higher than in the case of the analog percentage restrained differential relay. Therefore, the analog busbar differential protection schemes continued to be used worldwide.

DIFFERENTIAL RELAY DESIGNS

The basic concept for any bus differential relay is that the sum of all currents, which flow into the protection zone, must be equal to the sum of all currents, which flow out of the protection zone. If that is not the case, an internal fault has occurred. This is practically a direct use of Kirchoff's first law, which is taught in the "Basics of Electricity" during the first year of electrical engineering studies. Unfortunately, practice is often different and more difficult than the theory in the books.

Magnetic core current transformers

Bus differential relays do not measure directly the primary currents in the high voltage conductors, but the secondary currents of magnetic core current transformers, which are installed in all high-voltage bays. Because the current transformer is a non-linear measuring device, under high current conditions in the primary CT circuit the secondary CT current can be drastically different from the original primary current. This is caused by CT saturation, a phenomenon that is well known to protection engineers [6]. It is especially relevant for bus differential protection applications, because it has the tendency to cause unwanted operation of the differential relay.

Remanence in the magnetic core of a current transformer is an additional factor, which can influence the secondary CT current. It can improve or reduce the capability of the current transformer to properly transfer the primary current to the secondary side. However the CT remanence is a random parameter and it is not possible in practice to precisely determine it.

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Another, and maybe less known, transient phenomenon appears in the CT secondary circuit at the instant when a high primary current is interrupted. It is particularly dominant if the HV circuit breaker chops the primary current before its natural zero crossing. This phenomenon is manifested as an exponentially decaying dc current component in the CT secondary circuit. This secondary dc current has no corresponding primary current in the power system. The phenomenon can be simply explained as a discharge of the magnetic energy stored in the magnetic core of the current transformer during the high primary current condition. Depending on the type and design of the current transformer this discharging current can have a time constant in the order of a hundred milliseconds. Therefore, it has to be considered during the design stage of a differential relay in order to prevent the unwanted operation of the relay at the moment when a heavy external fault is cleared by the faulty line's circuit breaker.

Analog differential protection

The high impedance differential relay generally solves all practical problems caused by the CT non-linear characteristics by using the galvanic connection between the secondary circuits of all CTs connected to the protected zone. The scheme is designed in such a way that the current distribution through the differential branch during all transient conditions caused by non-linearity of the CTs will not cause the unwanted operation of the differential relay. This is achieved by connecting a high impedance (usually resistance) in series with the operating element of the differential relay. This impedance will then limit the level of false differential current through the differential branch. To obtain the optimum relay performance, the resistive burden in the individual CT secondary circuits must be kept low and should have a similar value in all bays. Therefore no other relays can be connected to the same CT core. At the same time, due to the lack of any other restraint quantity, it is strongly required that all current transformers within one differential zone have to have the same ratio and the same magnetizing characteristic. All these requirements impose additional expense to the power utility in order to purchase specially made CTs only for the bus differential protection.

However if all of the above conditions are met, this scheme is quite reliable and very sensitive. Its usual operating times for internal faults are below one power system cycle [1].

The percentage restrained differential protection scheme, based on a special analog circuit, depends as well on the galvanic connection between the secondary circuits of all CTs, connected to the protected zone, to remain stable for all transient conditions caused by the non-linearity of the main CTs. The galvanic connection is made via a special diode circuit arrangement, as shown in Figure 1. This diode circuit creates the rectified incoming current I_{T3} and the rectified outgoing current I_L. The difference between these two currents is the differential current I_{d1}. By this approach, a very simple but effective design of the relay is obtained. All relay decisions are based only on these three quantities, and the operation of the relay does not depend on the number of connected HV bays to the protection zone.

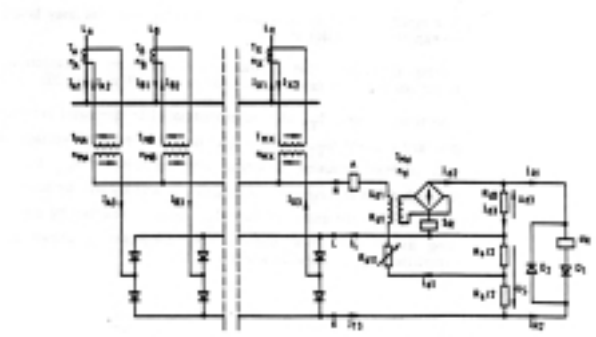

Figure 1: Principal schematic of the analog percentage restrained differential protection

Stability of this protection relay is guaranteed, regardless the primary fault current level and CT saturation if the total CT secondary circuit loop resistance, transferred across its auxiliary current transformer to the relay side, is less than or equal to the resistance R_{d11} in the differential relay branch (for operating slope of 0.5). Due to this special design feature, the relay allows much bigger resistance to be included in the secondary circuits of the individual main current transformers than in the original high impedance scheme. It can accommodate the different CT ratios by use of auxiliary current transformers. The CT requirements are very moderate and the relay can tolerate other relays on the same CT core. At the same time, by the use of high-speed reed relays, this bus differential protection scheme reliably detects internal faults within 1 to 3 milliseconds and issues the trip signal to the high voltage circuit breakers within 9 to 13 milliseconds from the occurrence of the internal fault.

Numerical differential protection

In new numerical protection relays, all CT and VT inputs are galvanically separated from each other. All analog input quantities are sampled with a constant sampling rate and these discreet values are then transferred to corresponding numerical values (i.e. AD conversion). After these conversions, only the numbers are used in the protection algorithms. Therefore it is impossible to directly re-use and copy the operating principles from the analog bus differential schemes, because there is not any galvanic connection between the CTs.

Therefore, if the secondary circuit resistance is not very important, what then are the important factors for the numerical relay design in order to guaranty the stability of the protection algorithm?

Actually it is the time available to the differential relay to make the measurements during CT saturation and to take the necessary corrective actions. This practically means that the relay has to be able to make the measurement and the decision during the short period of time, within each power system cycle, when the CTs are not saturated. As described in the references [2] and [3] this time, even under extremely heavy CT saturation, is for practical CTs around 2 ms. Therefore, it was decided to take this time as the design criterion for the minimum acceptable time before saturation of a practical magnetic core CT.

However, if the necessary preventive action has to be taken for every single HV bay connected to the protection zone, the relay algorithm would be quite complex. Therefore, it was decided to try to re-use the important quantities from the analog percentage restrained differential protection relay, like incoming, outgoing and differential currents, in the numerical design. These three quantities can be easily calculated numerically from the raw sample values from all analog CT inputs connected to the differential zone. At the same time, they have extremely valuable physical meaning, which clearly describes the condition of the protected zone during all operating conditions.

By using the properties of only these three quantities, a new differential algorithm has been formed which is completely stable for all external faults and very fast for the internal faults. All problems caused by the non-linearity of the CTs are solved in an innovative numerical way on the basic principles described above.

HEAVY CURRENT TESTING

When a new relay is designed, it is extremely important to properly test it in order to verify the performance and check its limits. The performance of the analog percentage restrained differential protection was checked in the heavy current laboratory about twenty-five years ago, with outstanding results. With the permission of the author, two oscillograms are reproduced from the reference [3].

For the external fault case (Figure 2) it can be seen that the relay was stable for a heavy external fault, with a burden of 20 Ohms in the secondary circuit of the CT with ratio 1000/5.

The internal fault case is shown in Figure 3. It can be seen that the relay differential element operated within 0.6 ms and that the relay sealed in after 3.5 ms from the inception of the internal fault.

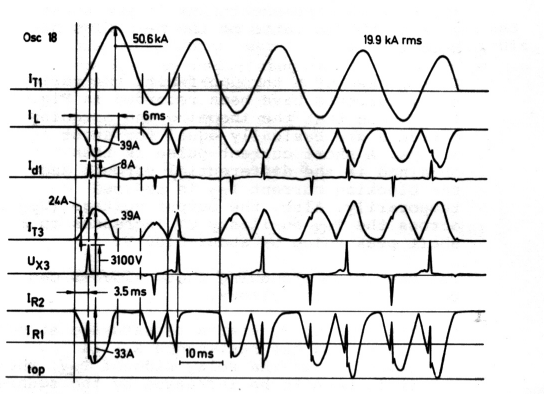

Figure 5 External fault (osc. 18) with permissible main CT secondary loop-resistance R_{X2} = 20 ohms. No operation has occurred.

Figure 2: External fault case during testing of the analog percentage restrained differential relay

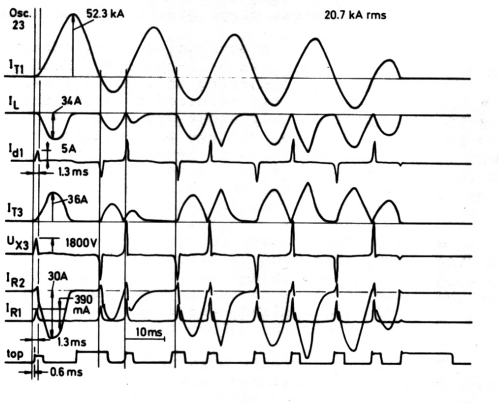

Figure 6 Internal fault (osc. 23). The S_R + d_R relays operate within 0.6 ms. The auxiliary seal-in relay operates 3.5 ms later.

Figure 3: Internal fault case during testing of the analog percentage restrained differential relay

When the design and the implementation of the new numerical differential relay were finished, the following heavy current testing facility was setup to test the relay:

- short circuit generator with the capability of producing currents of 26kA or 50kA RMS, and all other necessary heavy current equipment
- calibrated resistive shunt for measurement of the primary current
- digital recorder with the sampling interval of nine microseconds with ten input channels
- four identical dual ratio CTs with the data as specified in Table 1

Table 1: Data for dual ratio CTs used during testing

Ratio	Class	Rating [VA]	Sec. Resistance [Ohms]	Knee-point Voltage [V]
200/1	5P20	10	1.7	280
400/1	5P20	20	3.4	580

These four current transformers are designated as TA, TB, TC and TX. The three current transformers TA, TB and TC were used with the ratio 400/1 in all tests. However for current transformer TX the ratio 200/1 was used. It was as well possible to add additional resistance RX in the secondary circuit of the TX current transformer in order to obtain the very heavy CT saturation. In addition to that, a 200mA dc current source was available to pre-magnetize the TX current transformer in order to obtain the maximum possible remanence in the magnetic core for some tests.

The following quantities were recorded during all tests:

- Itot – total primary current of the short circuit generator
- IA – current on the secondary side of the TA current transformer
- IB – current on the secondary side of the TB current transformer
- IX – current on the secondary side of the TX current transformer
- Trip – status of the binary trip output contact from the numerical differential relay

However, it should be noted that all currents recorded on the secondary side of the current transformers (IA, IB and IX) are scaled, in all of the following figures, with the relevant CT ratio in order to be compared with the primary current Itot.

Stability Tests for numerical differential relay

During testing of external faults the test circuit was arranged as shown in Figure 4. During all these tests a primary current level of 26kA RMS was used.

As it can be seen from the Figure 4, the test circuit was arranged in such a way that it was possible to test the external faults with or without the pre load.

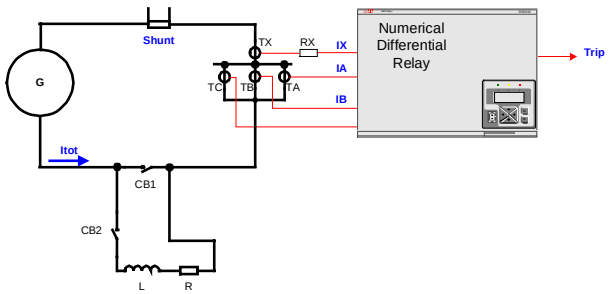

Figure 4: Simplified test circuit for external fault testing of the numerical differential relay

If the circuit breaker CB2 was closed before the main circuit breaker CB1, then the pre load of 200A was established. On closing of the main circuit breaker CB1 the external fault condition was applied to the numerical differential protection relay. It was as well possible to control the closing instant of the main circuit breaker in order to control the dc offset of the primary current.

The total incoming current to the differential zone was supplied to the numerical protection relay via three parallel-connected current transformers (TA, TB and TC). However, the total outgoing current from the differential zone was supplied to the numerical protection relay via only one weak current transformer TX. Therefore, during the external fault, the measured current IX on the secondary side of the current transformer TX had to balance the differential relay and prevent any unwanted operation.

For simplicity only two external fault test cases are presented in this paper. In test case No 20 (Figure 5), the current transformer TX was pre-magnetized with the dc current in order to get maximum possible remanence. Resistance RX had a value of 30 Ohms and the fault was applied without any pre load. The switching angle was chosen to get the maximum possible dc offset of the fault current. The first peak value of the primary current was 65kA. Current transformer TX saturated within 1.2 ms, but the numerical differential relay remained fully stable as can be seen from Figure 5.

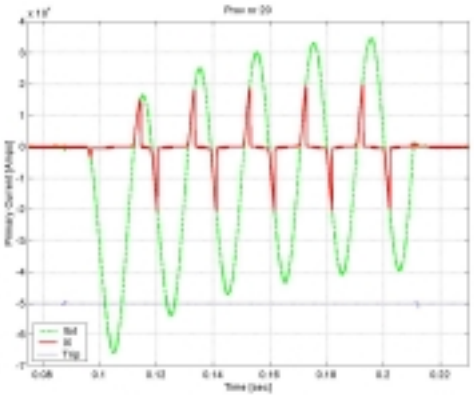

Figure 5: Test case No 20 - External Fault

In test case No 75 (Figure 6), the secondary resistance RX had a value of 48 Ohms and the fault was applied after a pre load of 200A. The switching angle was chosen to get the maximum possible dc offset of the fault current but without any pre-magnetization and hence no maximum remanence. The first peak value of the primary current was 65kA. Current transformer TX saturated within 1.8 ms, but the numerical relay remained fully stable as can be seen from Figure 6.

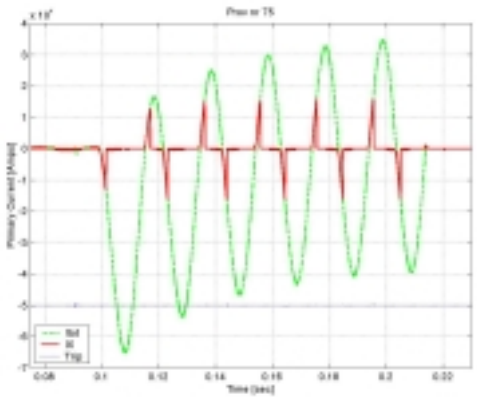

Figure 6: Test case No 75 - External Fault

In all other external fault test cases the numerical differential relay remained fully stable so long as the time to saturation of the weakest current transformer was above 1.2 ms. This meant as well that the relay is properly designed with respect to transients in the CT secondary circuits caused by clearing of high primary current. Such CT transients, captured during these tests in the secondary circuits of the TA and TB current transformers, are represented in Figure 7.

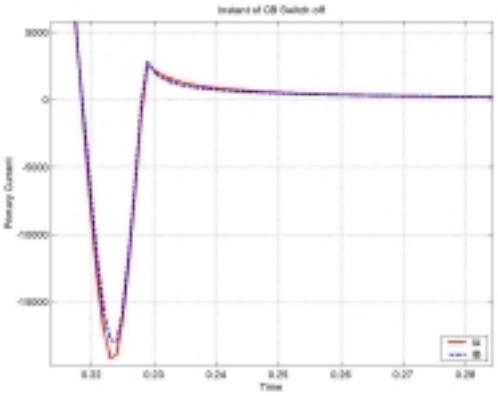

Figure 7: CT transients when external fault is cleared

Dependability tests for the numerical differential relay

During testing of the internal faults supplied with strong input CTs, the test circuit was arranged as shown in Figure 8. During these tests primary current levels of 26kA RMS and 50kA RMS were used.

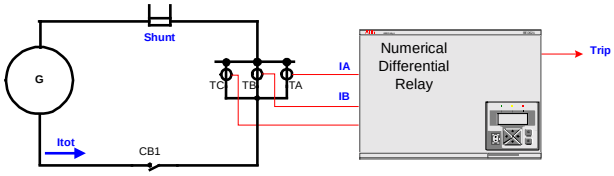

Figure 8: Test circuit for internal fault testing of the numerical differential relay with strong CTs

As it can be seen from Figure 8, the test circuit was arranged in such a way that it was only possible to test the internal faults without any pre load. After closing of the main circuit breaker CB1 the internal fault condition is applied to the numerical differential protection relay. It was as well possible to control the closing instant of the main circuit breaker in order to control the fault inception angle. The relay was tested for the complete possible span of fault inception angles (i.e. from 0 to 360 degrees) in steps of 10 degrees.

The total incoming current to the differential zone was supplied to the numerical protection relay via three parallel-connected current transformers (TA, TB and TC). The main purpose of these tests was to check the speed of operation of the relay for internal faults. For some of these test cases the primary current level was increased to 50kA RMS in order to check the capability of the relay to operate properly for extremely big secondary CT currents, which flow through the relay. For simplicity only two test cases with the 50kA fault level are presented in this paper.

In test case No 43 (Figure 9), the internal fault was applied without any pre load. The fault inception angle was chosen in such a way as to get completely symmetrical fault current without any dc offset. The first peak value of the total primary current was 70kA. The numerical differential relay correctly operated in 12ms, as can be seen from Figure 9.

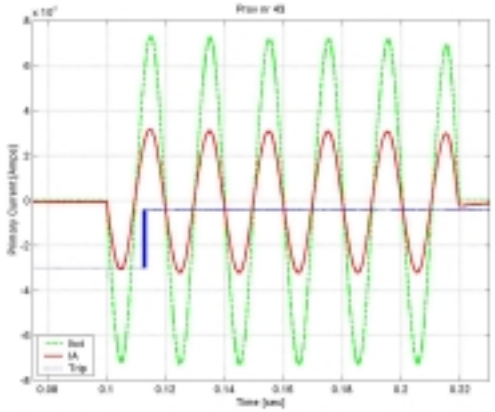

Figure 9: Test case No 43 - Internal Fault

In test case No 45 (Figure 10) the internal fault was applied as well without any pre load. The fault inception angle was chosen to get the maximum possible dc offset of the fault current. The first peak value of the total primary current was 125kA. Current transformer TA saturated within 4 ms, but the numerical differential relay correctly operated in only 12ms, as can be seen from Figure 10.

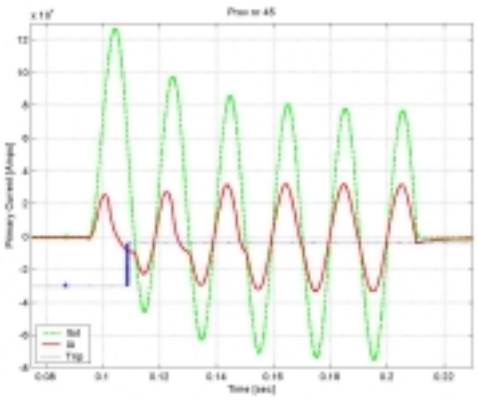

Figure 10: Test case No 45 - Internal Fault

It is as well extremely important to test the operation of the bus differential relay for internal faults with heavy incoming CT saturation. Therefore, the test circuit was re-arranged as shown in Figure 11, and the fault current was supplied to the relay via only one weak current transformer. During these tests a primary current level of 26kA RMS was used.

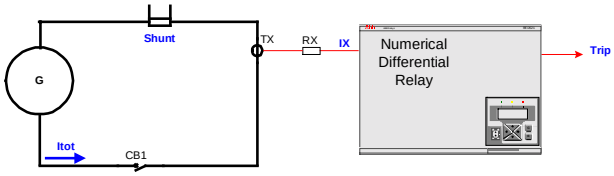

Figure 11: Test circuit for internal fault testing of the numerical differential relay with one weak input CT

For simplicity only one of these test cases is presented here. In test case No 66 (Figure 12), the current transformer TX was pre-magnetized with the dc current in order to get maximum possible remanence. Resistance RX had a value of 30 Ohms.

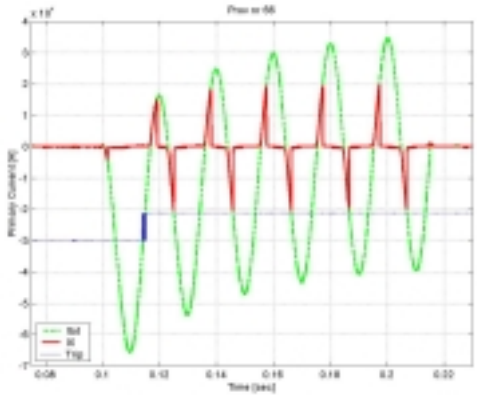

Figure 12: Test case No 66 - Internal Fault

The internal fault was then applied without any pre load. The fault inception angle was chosen to get the maximum possible dc offset of the fault current. The first peak value of the primary current was 65kA. Current transformer TX saturated within 1.2 ms, but the numerical differential relay correctly operated in only 14ms, as can be seen from Figure 12.

For all other internal fault test cases the numerical differential relay operated as expected with the trip time span from 12 to 16 ms.

CONCLUSION

It has been shown that it is now possible to design a numerical differential relay with similar performance as the best previous analog busbar differential relays.

In the heavy current laboratory, the new numerical bus differential relay was entirely tested. More than 70 very difficult test cases were made. The tests proved that the numerical differential relay remained totally stable for all external faults, even with a CT saturating in 1.2 milliseconds. On the other hand, the numerical relay issued a trip signal within 12 milliseconds for an internal fault. This means that the new numerical differential relay can practically match the performance of the previous analog generation of busbar differential relays. It has similar speed of operation and very low demands on the main current transformers. At the same time it offers all the other benefits of the numerical technology such as communication, self-supervision, no need for auxiliary CTs to match the different CT ratios, software CT switching for double or multiple busbar arrangements and relatively simple scheme engineering.

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