Future Trends in High Power MOS Controlled Power Semiconductors

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Future Trends in High Power MOS Controlled Power Semiconductors

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Abstract

Silicon based high power devices continue to play an enabling role in modern high power systems, especially in the fields of traction, industrial and grid applications. Today, approximately 30 years after its invention, a Bipolar-MOS "BiMOS" controlled switch referred to as the Insulated Gate Bipolar Transistor IGBT is the device of choice for the majority of power electronics converters with power ratings ranging from few kWs to beyond the 1GW mark. Following a brief introduction into power devices and applications in general, this paper will provide an overview of the development history and recent advancements of the IGBT. More importantly the future technology trends purely from the device design view point will be discussed including the predicted performance impact such technology platforms will have at the system level especially in the high power range.

Keywords: High Power, Bipolar, MOS Controlled, IGBT

INTRODUCTION

The power electronics revolution, which has over the past few decades swept across the power delivery and automation sectors, has opened up a wide range of possibilities in terms of controlling the way electrical energy is transported and used. At the heart of this revolution lies the power semiconductor device which has the main task of modulating the energy flow to suit the demands of the application. Power devices in general terms have enabled an ever increasing number of circuit topologies and related applications which in turn has enabled constant improvements in device performance. The progress of power devices has been largely dependent on technologies and processes developed initially for lower power applications and then scaled and optimized to enable the components to withstand higher voltages and currents to meet the requirements of higher power ratings. These advances in power semiconductors have led to tremendous improvements in power electronics applications in terms of power handling capability and control. With the recent energy related social, economic and environmental concerns coupled with the continuous progress in electrical power generation and control, the power device development trends are set to continue as a major enabler for matching the performance expectations of future systems.

The main power device development trends have always focused on increasing the power ratings while at the same time improving the over all device performance in terms of reduced losses, increased robustness, better controllability and reliable behavior under normal and fault conditions. In this paper, we shall begin with a basic overview of the silicon based power semiconductor technologies employed specifically in high power electronics conversion systems. This is followed with the main subject regarding today's most dominant high power semiconductor, namely the IGBT. The development history will be covered showing how the IGBT became the concept of choice for a wide range of applications and power levels. In addition, recent advancements and future technology trends based on the IGBT and on BiMOS concepts in general are discussed including an overview of the design and process requirements and their subsequent device performance improvements. It is important to note that similar advances and trends in line with the IGBT progress exist for the companion freewheeling fast recovery diode but this topic is not covered in this paper.

POWER DEVICES AND APPLICATIONS

Despite of the fact that a wide range of high power devices with attractive electrical characteristics exist, higher power and superior overall performance remain as the main targets for satisfying the demands of new high power system designs. Fig. 1: left illustrates the different available silicon based power device concepts and their typical operational power ratings and application frequencies while Fig. 1: right shows the different applications and their respective range of voltages and currents.

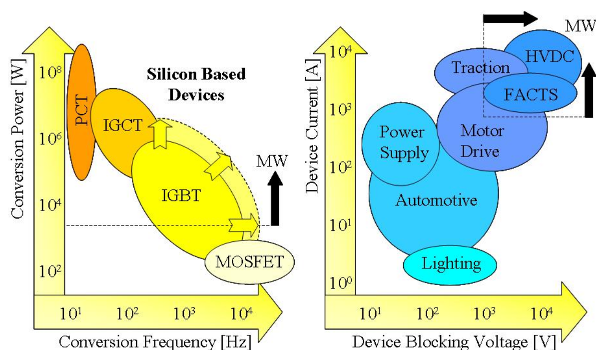

Fig. 1. Silicon based power devices and applications.

In the very high power range (also can be referred to as megawatt MW range), three types of switching high voltage devices are dominant; namely the Phase Controlled Thyristor (PCT) with no controlled turn-off function, the Integrated Gate Commutated Thyristor (IGCT) and the Insulated Gate Bipolar Transistor (IGBT) with the later two having controlled turn-off capability. One must also remember the power diode covering the whole power range when employed for rectification, snubber or freewheeling purposes [1]. In order to provide a brief historical insight, Fig. 2 shows the evolution of different power semiconductors in their respective packages while being classified here under Bipolar or MOS based technologies. It is important to point out here that the emergence of BiMOS controlled devices such as the IGBT was a result of combining the design and performance advantages of bipolar device concepts such as the power Bipolar Junction Transistor BJT and the low power Unipolar MOSFET. Therefore, the IGBT can cover a wider power range in many applications with improved MOS voltage driven controllability and lower losses due to the Bipolar carrier modulation.

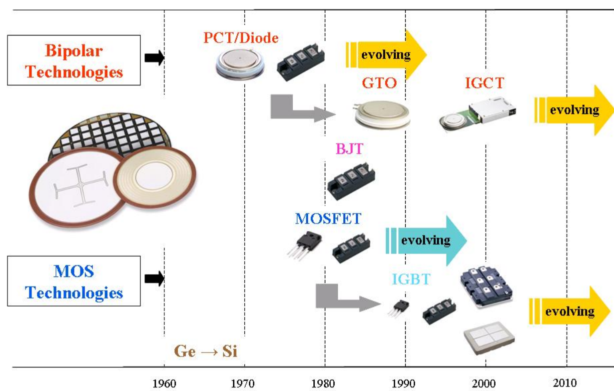

Fig. 2. Silicon based power device concepts and evolution. The extending arrows indicate a continuing development trend on a technology platform level.

Today, the above mentioned high power silicon based devices can be designed with good overall performance up to several thousand volts and amperes as single wafer components in the case of PCTs, IGCTs and diodes [2] [3] [4]or by paralleling devices in a specific package as is the case for IGBT/Diode chips [5]. For grid systems operating typically at much higher voltages in the hundreds of kilovolts range, devices are normally connected in series to support the total dc-line voltage. However, in the majority of modern power electronics applications, the VSI-topology (Voltage Source Inverter) when compared to CSI-topologies (Current Source Inverter) has achieved a dominant position in the field of frequency conversion. This is largely due to the better availability of low loss asymmetric power semiconductors (IGBT, IGCT) compared to symmetrical devices (PCT, RB-IGCT), simplified design and good controllability. In addition, to achieve the required control levels in such applications, turn-off devices are almost mandatory and the choice available today is between the IGBT and the IGCT. For comparison, Fig. 3 shows the IGBT and IGCT basic structures and related plasma distributions. The IGCT (as for the PCT) is a current controlled Bipolar device operating during conduction in thyristor mode which is mainly characterized by its favorable excess carrier distribution near the cathode for low on-state losses. On the other hand the IGBT is a voltage controlled Bipolar MOS device for achieving robust switching and relatively low on-state losses although still clearly higher than for the IGCT due to the lower MOS cathode plasma levels. However, IGBTs exhibit both a high input impedance allowing comparatively small gate drivers and unique and well controlled short circuit withstand capability as an added feature for fault control when compared to IGCTs.

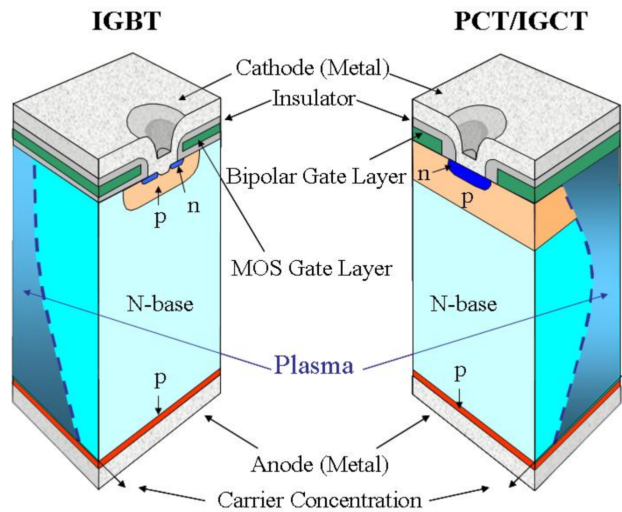

Fig. 3. IGBT and IGCT structures and carrier distributions.

THE IGBT AND TECHNOLOGY DRIVERS

More than three decades ago, the IGBT being a seemingly simple variant of the silicon power MOSFET was set on to change the power electronic landscape. The device presented interesting characteristics combining both MOS and Bipolar structures with very desirable performance and driving features for power system designers. The basic functional IGBT designs were researched during the 1980s and while the first commercially available IGBTs did not exceed blocking voltages above 600V, and currents of a few amperes, development efforts continued aimed solely at increasing the power handling capability. These targets were achieved and currently, high voltage IGBTs and diodes rated up to 6.5kV are successfully manufactured for 3.6kV DC link applications. In addition, high current IGBT modules with heavily paralleled chips are employed in many applications with current ratings up to 3600A.

The target for providing higher powers was and is approached on two principle levels, first by providing *higher absolute power levels* by means of paralleling multiple devices or by functional structure integration for a given package footprint. The second approach targeted *increased power densities* for a given device active area by means of losses reductions, higher operating maximum junction temperatures, improved thermal properties and increased Safe-Operating-Area SOA margins. Extensive process and design development efforts are required to enable such steps to take place. These technology drivers are illustrated in Fig. 4 and in the following paragraphs we will define each of these trends on general terms.

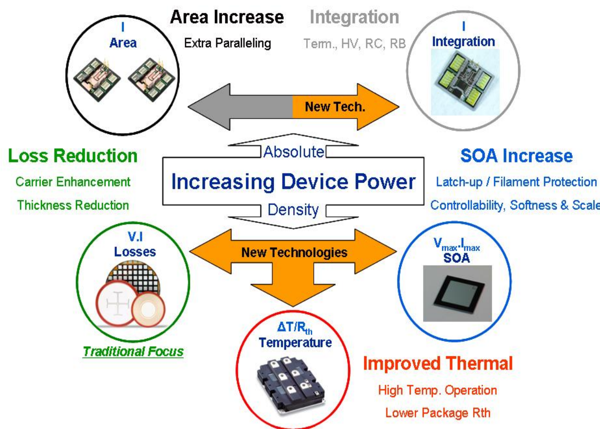

Fig. 4. Technology drivers for increased power ratings of IGBTs.

First we cover below the trend towards increasing the absolute power by means of area increase or through the development of integration solutions:

- Area Increase: Increasing power levels by means of paralleling chip in a single package or paralleling modules for a given inverter design is a standard approach for achieving the required power levels defined by the applications. Although at first glance, such an approach can appear to be less demanding in terms of technology development, it is a fact that higher power levels by such means were only reliably possible with improved device, package and system designs [6]. Critical parameters related to chip current sharing, SOA, package layout and system parasitics were always in the focus to enable the IGBT to make this step at a practical level with well defined de-rating rules having also been established [7].

- Integration Solutions: A number of development trends fall into this technology demanding category for enabling higher power capabilities. It mainly includes improved of full structure integration into a single device of currently separated structures having similar or different functionalities. Typical examples for IGBTs include:

- Higher voltage ratings of IGBTs to replace or reduce series connection for lower losses and lower cost when viable [8].
- Improved narrower junction termination designs for maximizing the active area of a given device total area.
- Reverse Blocking concepts (e.g. RB-IGBT) to replace an IGBT/Diode series configuration for providing lower losses and hence higher power in CSI applications.
- Reverse Conducting concepts (e.g. RC-IGBT) to integrate the IGBT and freewheeling diode into a single structure for higher power per package footprint [9].

The second group of trends focuses on increasing the power density through the reduction of losses, increasing the SOA margins and/or improving the thermal performance of the device and package.

- Losses Reductions: Over the years, improved technology curves of successful IGBT generations through static and dynamic loss reductions have always been the traditional focus for achieving higher power densities. This development trend targets have been achieved by means of plasma enhancement through improved planar and trench MOS cell designs [10] and/or device thickness reductions with buffer / anode optimization [11]. This trend is set to continue due to the fact that further loss reduction are still possible with plasma enhancement as discussed in a later section.

- SOA Capability: Higher power densities are always accompanied with the need for higher SOA margins and improved controllability for reliable operation. Typical device failure modes were always investigated and designs are improved to enable the device to withstand higher power switching transients, enable avalanche mode capability, reduce overshoot voltages with soft performance and the elimination of destructive filamentations due to design and process induced non-uniformities. A typical case for the IGBT is to improve the parasitic thyristor latch-up capability in the MOS cell during device turn-off under extreme operational conditions [12].

- Thermal Performance: Increasing the maximum operating junction temperature of IGBT modules is a recent trend to achieve higher power densities [13]. Device optimization for realizing this target has been focused on reducing the reverse bias leakage current at higher temperatures for stable thermal performance. Although not in the realms of this paper's main subject, it is worthy to point out that this trend is strongly accompanied with high temperature package developments in terms of improved filling materials and

joining technologies with lower thermal resistances while also maintaining high reliability power cycling capabilities for the targeted elevated temperatures.

As a general rule, for attempting to make the next power density capability leap, it is important first to single out main power limiting factor being it losses, SOA, or thermal for a given device technology. Once this is defined, the limiting capability must then be solved in order to achieve the higher power density target. In other words, if the SOA capability is limiting the power handling capability of a given device technology as was the case at some evolution stage with high voltage IGBTs, then further reductions in losses could provide better efficiency but it will not enable the device to operate and higher current densities and hence higher power levels.

IGBT EVOLUTION AND FUTURE TRENDS

Based on the above technology trends, Fig. 5 shows the evolution of IGBTs since their first commercial products appeared around the early nineties. The structural development of the basic IGBT design can be divided into bulk (including drift, buffer and anode) and MOS cell optimization where both target mainly lower losses. In parallel, developments were carried out for improving the SOA and High Temperature HT operation capabilities.

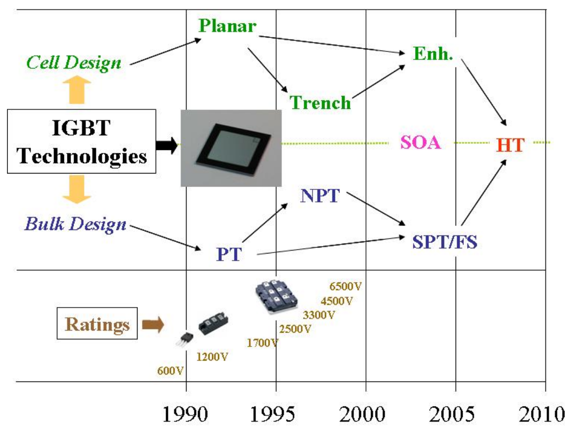

Fig. 5. Evolution of IGBT technology.

However, it is worth noting that during the 1990s extensive development efforts were underway to replace the IGBT with lower loss MOS controlled thyristor based structures [14]. Such concepts never materialized into mainstream products due to their complex designs and associated processes and the lack of SOA capability during turn-off and short circuit modes of operation. In parallel, the IGBT continued to develop from both the cell and bulk design platforms and the resulting wide range of IGBT products continued to provide applications with optimum components which have enabled with each improved generation a clear leap in power levels.

LOSSES REDUCTIONS

The most important trend in IGBT development targeted lower losses due to thinner n-base regions with optimized buffer/anode profiles combined with plasma enhancement layers and/or trench cell designs as discussed below:

a. The Bulk Design: The first IGBTs were available in the low to medium power range with voltages ranging from 600V up to 1200V. Such devices utilized the so-called Punch-Through structure PT-IGBT employing epitaxial starting material and heavy lifetime reduction necessary due to the strong and thick P+ anode substrate. The PT-IGBT suffered from major drawbacks such as a strong negative temperature coefficient during on-state and snappy turn-off switching behavior due to the low lifetime in the base region making them not suitable for heavy paralleling applications and restricting their use only in discrete packages and low current modules. A solution for this problem followed with the introduction of the Non-Punch-Through NPT-IGBT [15] that was manufactured on a thin-silicon substrate with a weak anode and therefore, no lifetime engineering was necessary. The NPT-IGBT was one of the first IGBTs to be employed successfully in high current modules with ratings up to 1700V and 2400A. Although, due to the thicker base region, the device suffered from higher on-state and turn-off losses, a strong positive temperature coefficient, soft turn-off behavior and excellent short circuit ruggedness were the main reasons preferring the NPT-IGBT in such heavy paralleling configurations.

In the past decade, designers resorted into an optimized version of the PT-IGBT to match the NPT performance by introducing a new generation employing the so-called Soft-Punch-Through “SPT” [16] or Field-Stop design “FS” [11]. The device had thinner n-base regions but with an optimized low-doped deep n-buffer and weak anode as shown in Fig. 6 when compared to the NPT IGBT.

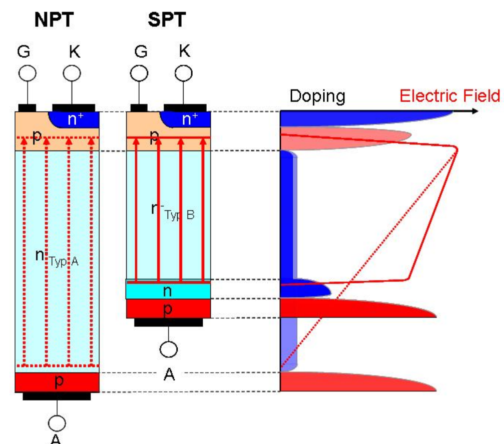

Fig. 6. The NPT and SPT IGBT structures, doping profiles and field distribution during reverse blocking.

The SPT buffer is optimized to stop the field penetration during the blocking state while still allowing conductivity modulation to occur during conduction. Therefore, the new SPT-IGBT combined the advantages of the low-loss PT-IGBT (thickness reduction reduces the static and dynamic losses simultaneously) and the positive temperature coefficient and soft turn-off behavior of the NPT-IGBT. For low voltage devices rated below 1700V, process challenges had to be met in terms of thin wafer processing <150um especially for establishing the required buffer and anode profiles after device thinning [17]. Furthermore, the SPT concept also allowed for the introduction of higher voltage rated devices up to 6500V.

Despite all the benefits introduced with the SPT-IGBT, major design constrains surfaced since the reduction in device thickness has always been accompanied with an increase in the resistivity to achieve the required blocking capability of the device and provide a low failure rate (FIT) due to cosmic rays [18]. This trend will have the following effect on device performance and becomes more critical when the device is operating with a higher stray inductance in high current modules due to

1. Reduced punch-through voltage resulting in snappy and uncontrollable turn-off behaviour.
2. Large peak overshoot voltage "stress" due to the faster di/dt commutation rates.

The choice of the silicon thickness and resistivity must be carefully reached to avoid or minimise the effects mentioned above. The higher the voltage rating of the device the more critical this optimisation approach becomes due to the higher resistivity values and large circuit stray inductance accompanied with a high DC link voltage. In general, current state of the art IGBTs are very close to their silicon limits, and any further optimisation for lower losses will jeopardise the usefulness of these devices in many applications. The device thickness for SPT-IGBTs versus vs. an equivalent NPT design over a whole range of voltage ratings is shown in Fig. 7.

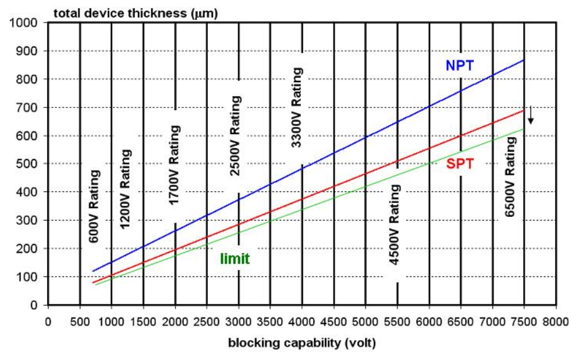

Fig. 7. Reverse blocking capability vs. device thickness for NPT and SPT IGBT structures.

The other important part of the bulk design is the choice of the buffer and anode doping profiles. Increasing the SPT buffer depth or employing a stronger anode to increase the plasma in the device for softer behaviour has been one approach for further softness optimisation at the expense of increased turn-off losses. However, experience has shown that there exists a strong trade-off relationship with other parameters as summarised in Fig. 8. The SPT-IGBT behaviour under static, dynamic and short circuit conditions was found to be strongly dependent on the PNP transistor gain values under different operating conditions [19] [20].

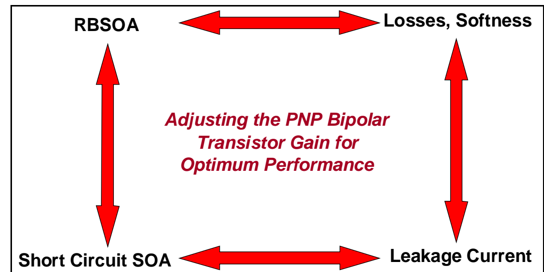

Fig. 8: The art of SPT-IGBT design.

In line with the bulk design trend, recent investigations have shown that the super junction concept employed currently in MOSFETs could also bring forth lower losses for IGBTs. The main feature is with regard to the lower turn-off losses [21] achieved due to the less plasma modulation and fast charge extraction in the n and p type bulk charge compensation regions. Nevertheless, when compared with the MOSFET, finer dimensions and higher dopings for those regions are needed for the IGBT for optimum performance. Hence, one can foresee the advantage of such a concept in lower voltage rated and very fast IGBTs (<1200V) while taking into account the complex processes and tight tolerances required.

b. Cell Design: The first IGBTs inherited planar DMOS cell designs from the power MOSFET with relatively large scale dimensions and weak plasma enhancement near the cathode region. Further moderate improvements were made for the optimization of the planar cell with finer dimensions but at the cost of lower SOA capability. Nevertheless, in the mid nineties, IGBT designers were also heavily involved in the development of trench gate emitter designs to replace the standard planar cell in order to further reduce the on-state losses of the device through strong carrier enhancement [22]. However, this step also prompted major changes in the device performance due to a large input capacitance of the trench cell and certain undesirable characteristics such as the high short circuit current levels due to the increased cell packing density. Since then, trench gate devices were optimized to overcome some of these drawbacks with optimized layout design [5] [23] and employing n-type enhancement layers

[24]. In parallel to trench developments, an Enhanced Planar IGBT concept shown in Fig. 9 was also realized to provide loss reduction figures rivaling those of the state-of-the-art trench IGBTs over the whole voltage range [25] [26]. Fig. 10 shows the IGBT technology evolution in terms of the impact on the on-state losses.

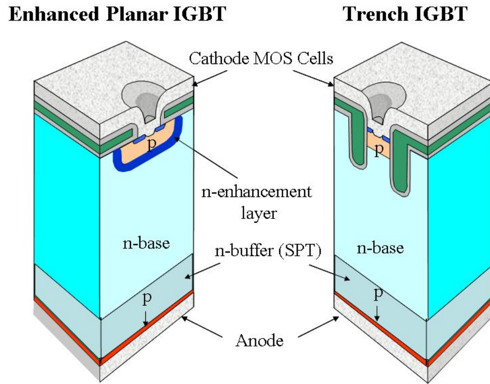

Fig. 9. IGBT modern structures.

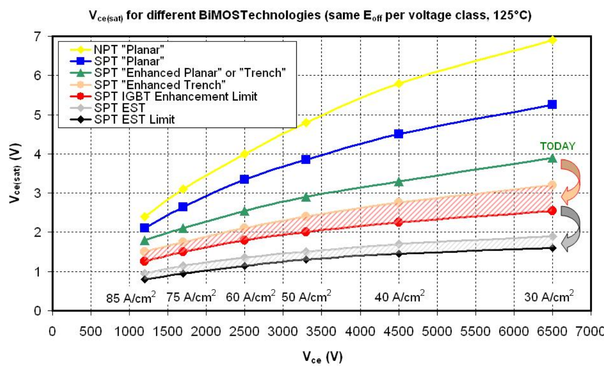

Fig. 10 BiMOS technologies on-state losses $V_{ce(sat)}$.

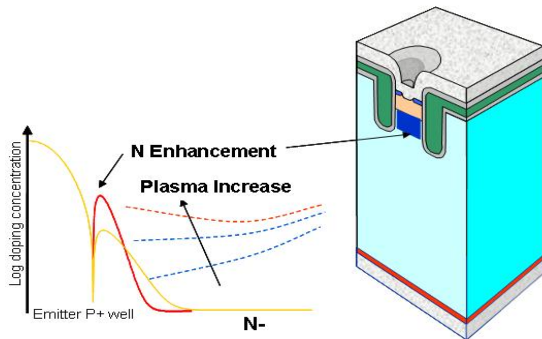

Fig. 11. Improved plasma for enhanced trench IGBT cell designs.

With very little optimization possibilities remaining by reducing the silicon thickness, any further loss reductions are predicted from simulation results by developing an improved trench cell design. The ultimate goal of reaching close to a plasma enhancement limit as shown in Fig. 10 could be approached with the optimization of an enhancement trench structure having higher levels of enhancement and minimum effective gate input capacitance associated with state-of-the-art trench designs as shown in Fig. 11. This can be achieved with optimised trench cell and layout designs while increasing the N-enhancement layers from today's 1e16/cm^3 to nearly 5e16/cm^3 for higher plasma levels [27].

SAFE OPERATING AREA

Trends for the development of IGBTs and diodes have always aimed to obtain a sufficiently large safe operating area (SOA) as required by many power electronic systems operating under hard-switching conditions. With improved cell and bulk designs, modern HV-IGBTs are able to demonstrate very robust performance even under extreme conditions [12]. Prior to that, in order to overcome the insufficient ruggedness, device manufacturers and system designers resigned themselves to a number of operational limits such as de-rating and the use of voltage clamps, snubbers and high gate resistances, to achieve the necessary switching capability. Modern IGBT design platforms with extremely high SOA capability were developed mainly for increasing substantially the cell latch-up immunity for a wide SOA performance. This new technology enables the devices to withstand the critical, formerly unsustainable, phase of dynamic avalanche resulting in a remarkable increase of ruggedness. Devices were also able to reach and withstand a new operational mode referred to as the Switching-Self-Clamping-Mode (SSCM) as the overshoot voltage reaches levels close to that of the static breakdown voltage. For example, the Enhanced-Planar SPT IGBT turn-off SOA power level can reach up to 1.5MW/cm^2 as shown in Fig. 12 for a 3300V device. The extremely harsh test was carried out on a single chip with a current rating of around 62.5A having endured up 500A and 3000V in conduction current and applied DC link voltage respectively. Such SOA margins play an enabling role for developing other trends such as high temperature operation and integration.

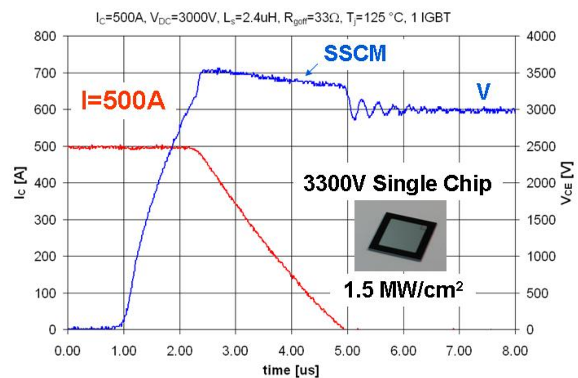

Fig. 12. 3300V/62.5A EP-IGBT turn-off SOA.

HIGH OPERATING TEMPERATURES

The recent important trend for increasing the maximum operating junction temperature of power devices has shifted the design focus towards improved blocking characteristics especially in terms of reduced leakage currents for stable high temperature performance. The important design parameters for achieving this target can be listed as follows

1- Improved termination and passivation with lower leakage current
2- Reduction of diode lifetime control impact on leakage currents (important for diode)
3- Reduction of the IGBT Bipolar gain impact on leakage currents

In principle, it has been shown that purely from the electrical performance viewpoint, there are no clear device related limits for enabling higher temperature operation up to 200°C in terms of the dynamic and static performance [28]. Fig. 13 shows the switching SOA turn-off waveforms of a 1200V SPT IGBT device at 200°C. Nevertheless, reliable performance at device and package level will remain in the focus in the coming years as this trend continues to evolve. Today, 600V up to 1700V devices are commercially available with maximum junction temperature ratings up to 175°C while 3300V IGBTs have reached 150°C and there are developments to extend his trend towards higher voltages.

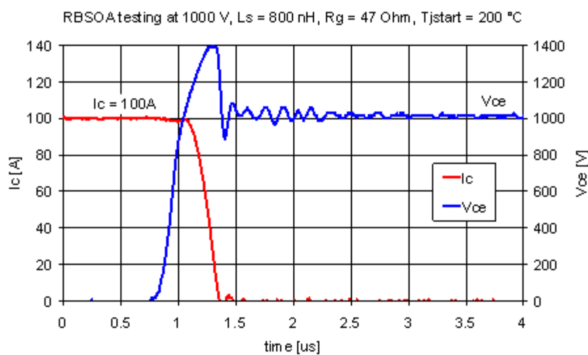

Fig. 13. 1200V/25A SPT IGBT turn-off SOA at 200°C.

INTEGRATION, THE RC-IGBT

In modern applications employing IGBT modules, the diode presents a major restriction with regard to its losses performance and surge current capability. Both limits are clearly a result of the historical limited diode area available in a given package footprint design which has a typical IGBT to diode area ratio of around 2:1. This limit in the diode current capability was fundamentally established after the introduction of modern low-loss IGBT designs. The simple solution of increasing the diode area is not a preferred one and in any case remains restricted by the package standard footprint designs. Therefore, the clear demand in increased power densities of IGBT and diode components has led to the focus on an IGBT and diode integration solution, or what has been normally referred to as the Reverse Conducting RC-IGBT [29] [30].

The practical realization of a single-chip technology will provide an ideal solution for compact systems with higher power levels, which is proving to be beyond the capability of the standard two-chip approach. However, the realization of such a concept has always been hindered by design and process issues resulting in a number of performance drawbacks such as on-state snap-back, IGBT vs. diode losses trade-off, turn-off softness, and SOA. Development efforts in the direction of solving these aspects have resulted in an advanced RC-IGBT concept referred to as the Bi-mode Insulated Gate Transistor (BIGT) which is a hybrid device integrating an RC-IGBT and an IGBT in a single chip as shown in Fig.14 [31]. The SPT buffer design and enhanced planar technology discussed previously have been the main enablers to bring forth the possibility of this integration step. In addition, a number of new technologies were introduced into the BIGT in order to realize the integration of the previously two chip functionalities such as the Local P-well Lifetime (LPL) step to reduce the diode recovery losses and the specialized backside layout design and process including a pilot IGBT defined as a region having no n-type shorted regions. The pilot area is centralized in the middle to obtain better thermal distributions and reduced current non-uniformities and is also designed to provide the outermost reach within the chip while ensuring a large RC-IGBT region [32]. The results obtained show that the BIGT exhibits low losses in both modes of operation with no typical snap-back behavior in the transistor on-state mode when compared to a standard RC-IGBT, while also maintaining high levels of SOA performance. The BIGT offers in addition a number of device performance advantages such as soft switching behavior under extreme conditions and better diode surge current capability.

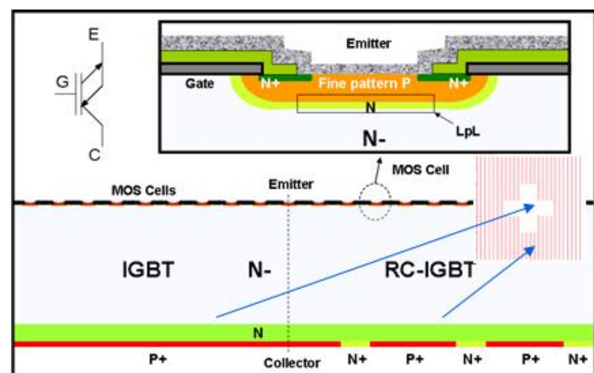

Fig. 14. Cross section of the BIGT.

The initial BIGT demonstrators were developed for devices rated at 3300V. High current BIGT (140 x 130)mm modules containing 24 chips each were fabricated and tested under conditions similar to those applied to state-of-the-art IGBT modules. The nominal transistor and diode mode switching characteristics of the BIGT modules are shown in Fig. 15 along with the associated switching losses indicated at 125°C. These waveforms show the clear capability of the BIGT to perform both the conduction and freewheeling tasks in a single chip.

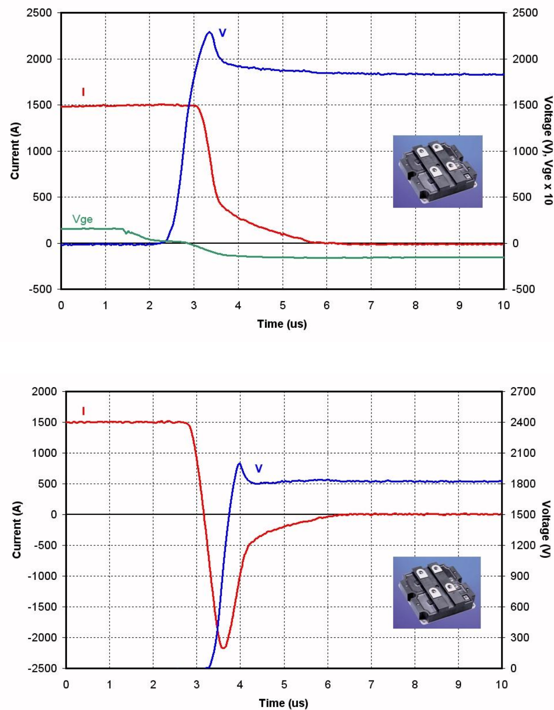

Fig. 15. 3.3kV BIGT module nominal turn-off (top) and reverse recovery (bottom). Losses: E_{off} =2.8J, E_{on} =2.2J and E_{rec} =2.3J.

Furthermore, due to the fact that transistor and diode share the same silicon area, there are no more inactive periods for the silicon and thus less temperature ripples. This will also lead to better thermal utilization of the module and eventually improved reliability performance due to a better thermal cycling capability. This feature will also enable a more reliable chip operation at higher junction temperatures [33] [34].

REVISITING MOS BIPOLAR DEVICE CONCEPTS

As shown previously in Fig. 10, despite improvements in carrier enhancement, the IGBT structure will still suffer from inherently higher on-state losses when compared to thyristor based devices such as the IGCT. The carrier enhancement level in IGBTs is mainly influenced by the MOS channel resistance, the hole accumulation effect between cells (or PIN effect) and the hole drainage effect in the cell. The electron spreading from the channel is an integrated part of the above three effects. These aspects of the IGBT design have been optimized with certain trade-offs in terms of blocking capability, controllability and SOA to achieve low losses as discussed previously in the cell design section. Nevertheless, the evolution maintained an IGBT structure in principle which remained intact since the basic properties to obtain good overall performance are kept.

The quest for an improved MOS controlled device with a thyristor like plasma distribution and IGBT like overall performance was intensified in the 1990s as pointed out previously. MOS Controlled Thyristors (MCT) [35] and Emitter Switches Thyristors (EST) [14] including many versions were investigated by means simulations and fabricated devices. The MCT was purely a turn-on and turn-off thyristor device which proved unpractical due to the limited current turn-off capability in thyristor mode when compared to IGBTs and IGCTs which turn off in Transistor mode. Only low voltage 600V and low current <20A MCTs in discrete packages were exploited commercially for a limited time and volume in niche applications. The EST on the other hand was proposed to attempt to solve the SOA problems by employing the cascade concept of integrating a low voltage MOSFET in series with a thyristor structure. The other main feature of this device is the controlled MOS turn-on capability. Different versions of the planar and trench ESTs (standard, duals, cascaded [36]) were proposed but still they showed few inherent drawbacks which contributed along with other factors to the eventual demise of this concept. So of these issues are listed below:

1) The continuous improvements in IGBT designs and the introduction of IGCTs
2) Low turn-off SOA capability, but this was a also an issue for IGBTs
3) Limited Short Circuit capability
4) Optimized EST versions resulted in higher on-state losses

Despite the historical background and the above reasoning, the basic idea and possible derivatives of the EST remain attractive at this stage of BiMOS developments. With the recent advancements in IGBT design and overall performance, revisiting the EST concept is important to surpass what IGBTs can achieve in the future especially when taking into account that there will be less emphasis to maintain the full short circuit capability since fault conditions can be dealt by other means such as the case in IGCTs. Predicted on-state values for such a technology are also shown in Fig. 10.

CONCLUSIONS

In an ever increasing power electronics applications market, the fundamental contribution power semiconductor devices have on the system level performance will ensure the continuous drive for improving both the device functionality and operational parameters. The paper presented a review of the recent advancements achieved in the field of Bipolar MOS controlled silicon devices with the main component under the spotlight being the IGBT. Future developments will maintain similar past trends for the growing system demands in terms of increased power levels, improved efficiency, greater control and reliability. It is important to note that the future of silicon based power devices in general will be to a certain extent influenced by the introduction of wide band-gap based power devices. Nevertheless, silicon based components will continue to be an enabler and market leader for the foreseeable future especially for the high power range applications.

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