

Route switching criteria for REL 551/561

1 Introduction

REL 551/561 only tolerates 0,2 - 0,5 ms asymmetric communication channel delay in the two directions. A constant delay difference can be adjusted by setting of the asymmetric delay on the built in HMI or by the CAP 540/PST tool. The acceptable time delay difference depends on the set sensitivity of the differential protection.

During route switching, a wider communication channel asymmetry can be accepted. However, *route switching can only be handled correctly after complete start-up of the terminals, i.e. when the master and slave clocks are properly synchronized.*

The supervision of the route switching is made by observing the deviation between the reference clocks in the slave and the master terminal.

2 Reference clock deviation < 150 μ s

A route switching, which cause a virtual difference between the reference clock in the master and the slave < 150 μ s due to asymmetry in the communication channel delay is not causing any communication failure alarm or blocking of the trip function. It is considered to be within the accuracy requirements and will be compensated for by the normal synchronization mechanism.

If the route switching takes long time, the master and slave terminal will start to synchronize, after a delay of 4 seconds, with the new channel asymmetry incorporated. The normal clock synchronization will adjust the slave within +1 μ s in addition to the compensation for the normal deviation between the clocks. The time synchronization messages are sent every 40 ms. With 150 μ s clock deviation between the master and slave terminals. It will take total 10 (4+6) seconds to reach a new synchronization with + 1 μ s accuracy.

3 Reference clock deviation >150 μ s

A route switching that cause a virtual difference between the reference clock in the master and the slave >150 μ s due the asymmetry in the communication channel delay is supervised during 50 master-slave clock synchronization messages. The time synchronization messages are sent every 40 ms, which gives a total time of 2 seconds. During this time the differential protection is still in operation, but the synchronization of the reference clock in the slave is blocked, why the original accuracy between the reference clocks will be maintained.

If the reference clock deviation >150 μ s is still valid after 2 seconds, internal Comfail will be issued and the current differential trip blocked. Then a new synchronization with a clock adjustment of 20 μ s initially for each clock synchronization message will take place. The clock adjustment step will gradually decrease, when the clock difference is reduced.

If the two channels are restored to the same time delay in both directions within 2 seconds, no difference between the reference clock in the master and the slave will be detected, and no blocking of the trip function will occur.

Route switching within 2 seconds has no influence on the clock synchronization for the current differential protection. Thus, the trip function is available directly, when the communication is restored.

4 Route switching / interruptions > 2 seconds, example

If the route switching takes longer time, for example 4 seconds, the clocks will be synchronized with the asymmetric delay included. The influence of the asymmetry will then be: $2 \text{ seconds} / 40 \text{ ms} \times 10^{-6} \text{ s}$ (average of 20^{-6} s and 1^{-6} s) = 0,5 ms, which can cause unwanted trip, depending on the sensitivity of the differential function.

Communication failure in the range of 10 to 30 seconds can cause the relay to lose the synchronization. Communication failure > 30 seconds will always need a new synchronization of the relays. If the synchronization has been lost, it takes 5 to 10 seconds of healthy communication to get the relays synchronized again and work with normal tripping times.

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