ABB Power T&D Company Inc.
Relay Division
Coral Springs, FL 33065

Instruction Leaflet
40-201.7

Effective: March 1994

NEW INFORMATION

G.703 Interface Adapter

1. INTRODUCTION

The G.703 Interface Adapter interfaces CCITT G.703 compliant Data Communication System to 64 kbs Fiber Optic or RS 422 port operating at 64 k baud.

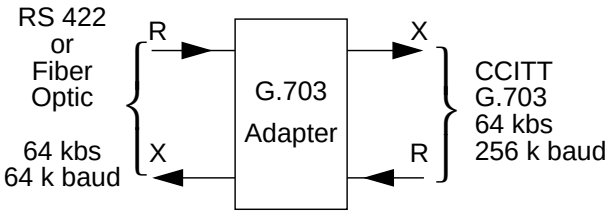


Figure 1. G.703 Block Diagram

2. FEATURES

The G.703 interface complies with CCITT G.703 co-directional, 64 kbps specifications. There is a five terminal, screw terminal block with two terminals for the transmit line, two for the receive line and one for earth ground.

The fiber optic and RS 422 ports operate at 64 kbps. Data rate clock signals are not needed or provided by the adapter.

NOTE: Only the transmit and receive data signals are available. Therefore a self clocking code like NRZI must be used.

The fiber optic port has a separate transmitter and detector connectors (separate transmit and receive fibers are required). Wavelength is 850 nm and ST type connectors are used. The transmitter is HFBR-14XX series and the receiver is HFBR-24XX series.

The RS 422 interface has transmit and receive differential pairs that comply with RS 422 electrical specifications. The connector and pins (chassis and signal grounds, transmit and receive pairs) comply with RS 530 specifications.

3. SPECIFICATIONS

3.1. Power Requirements

Input Voltage: 48 Vdc nominal (42 to 60 V range)
or
125 Vdc nominal (100 to 200 V range)

Power Consumption: 5W

3.2. Temperature Range

Operating: 0°C to 65°C

Storage: -20°C to 80°C

3.3. Physical Data

Height: 5.30” (134.6 mm)
Width: 3.43” (87.1 mm)
Depth: 4.25” (108 mm)
Weight: 2.0 lbs (0.9 kg)

3.4. Communication Ports

3.4.1. G.703 Port

CCITT G.703 co-directional 64 kbs compliant, transformer coupled.

3.4.2. Fiber Optic, 64 kbs Port

Transmit and receive lines 850 nm, ST connector, multi-mode cable, 10 dB optical power budget.

3.4.3. RS 422, 64 kbs Port

Transmit and receive lines are RS 422 (electrical) and RS 530 (mechanical, connector and pin numbers) compliant.

The female (receptacle) DB25 connector is used in adherence to Data Communication Equipment (DCE) definition.

4. INDICATORS

The four LEDs indicate:

- Transmitted signal activity (transitions)
- Received signal activity (transitions)
- Presence of G.703 received signal carrier and sync.
- power

5. INSTALLATION

5.1. Power

Connect 48 Vdc or 125 Vdc nominal to “DC Power Input” terminals.

5.2. G.703 Port

Connect transmit and receive ports to “G.703 TX OUT” and “G.703 RX IN” terminals respectively. Use of shielded twisted pairs is strongly recommended. Connect earth ground to terminal Chassis GND”.

5.3. 64 kbs Port

5.3.1. RS 422 / RS 530 Option

The G.703 Interface Adapter is equipped with DB25 female (Receptacle) connector. Therefore the interconnecting cable must use DB25 male connector.

Connect transmit pair (data from Interface Adapter) to pins 3 and 16. (Pin 3 positive and pin 14 negative).

Connect receive pair to pins 2 (positive) and 14 (negative).

Connect pin 7 (signal common) to corresponding signal common pin at the other end of the cable.

5.3.2. Fiber Optic Option

Connect transmit data cable to “XMT” fiber optic transmitter.

Connect receive data cable to “RCV” fiber optic receiver.

NOTE: ST connectors and multi-mode fiber optic cables are required.

6. DETAILED DESCRIPTION

6.1. G.703 Fundamentals

The following describes 64 kbit/s G.703 co-directional interface in which the information and its associated timing signal are transmitted in the same direction.

Code conversion rules

Step 1 — A 64-kbit/s bit period is divided into four unit intervals.

Step 2 — A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 — A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 — The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 — The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an Octet.

These conversion rules are illustrated in Figure 2.

6.2. Circuit Description

Both G.703 line pairs (refer to Internal Schematic Dwg. 1617C21) are coupled to U1 via transformers T1 and T2.

U1 converts the received analog signal at secondary of T1, to digital form and monitors received signal level. U1 also has level interface devices and output transistors that drive the transmit line pair via the primary of T2.

Co-directional Digital Data Processor U2 decodes the received G.703, 256 k baud signal and extracts the 64 kbps received data. It also converts 64 kbps data into a 256 k baud G.03 transit signal and monitors the received signal for correct sync.

U2 does not output and input 64 kbps data directly. It communicates in bursts of 8 bits at a time, at a 2.048 MHz clock rate, 8,000 times per second. This is because this particular IC is designed for equipment that processes T-1, CEPT or ISDN signals.

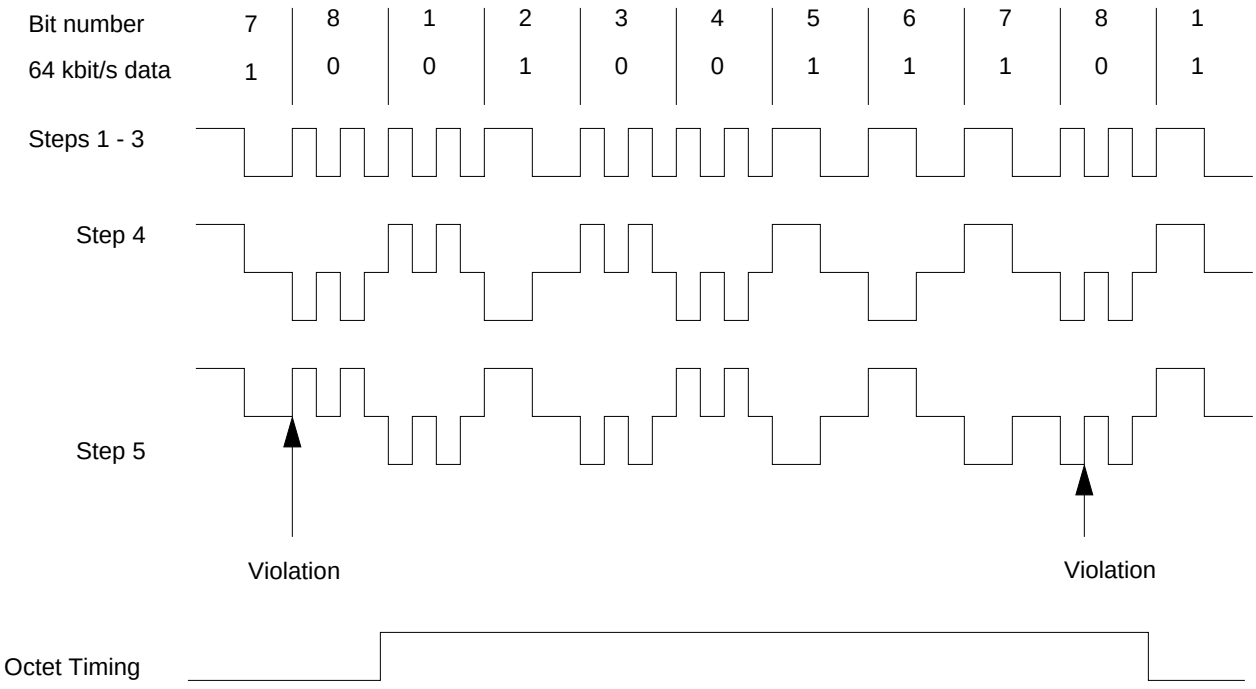


Figure 2. Code Conversions

EPLD U3 contains shift registers, counters, clock dividers and other logic that interfaces binary, synchronous, 64 kbps data to the bursts of data used by U2. The EPLD also detects transmit and receive data transitions and will pulse the data activity LED's.

The EPLD divides clock from crystal oscillator U5, or 2.048 MHz and 256 kHz for U2. It also switches from fiber optic port to the RS 530 port as determined by position of Jumper J1. The EPLD monitors carrier detector and sync signals from U1 and U2 and if these are all good, it will light the received signal OK LED.

When the fiber port is enabled, then transmitter LE1 and receiver LE2 are active. Q1 is an emitter follower which when conducting (EPLD drives its base low), will turn off the LED transmitter by absorbing all the R5 current. when Q1 is turned off by the EPLD driving its base high, then all current goes to LED transmitter LE1.

When the RS 422 port is enabled, than the signal path between U4 and the EPLD is active. U4 converts standard CMOS / TTL logic level to the differential RS 422 levels used for the data transmit and receive paths.

The only internal voltage is +5 Vdc (Power Supply Module schematic #1617C22). This is supplied by an internal Vicor power supply PS1. A different Vicor supply and input filter capacitor is required for 48 V, or 125 Vdc input voltage. DC input is applied to P5.1 and P5.22. this is fused by F1 and F2 before being applied to bridge rectifier BR1 and then to the Vicor dc input. BR1 always directs the right polarity to the power supply regardless of supply voltage polarity.

7. ORDERING INFORMATION

7.1. Catalog Number

Typical Catalog Number

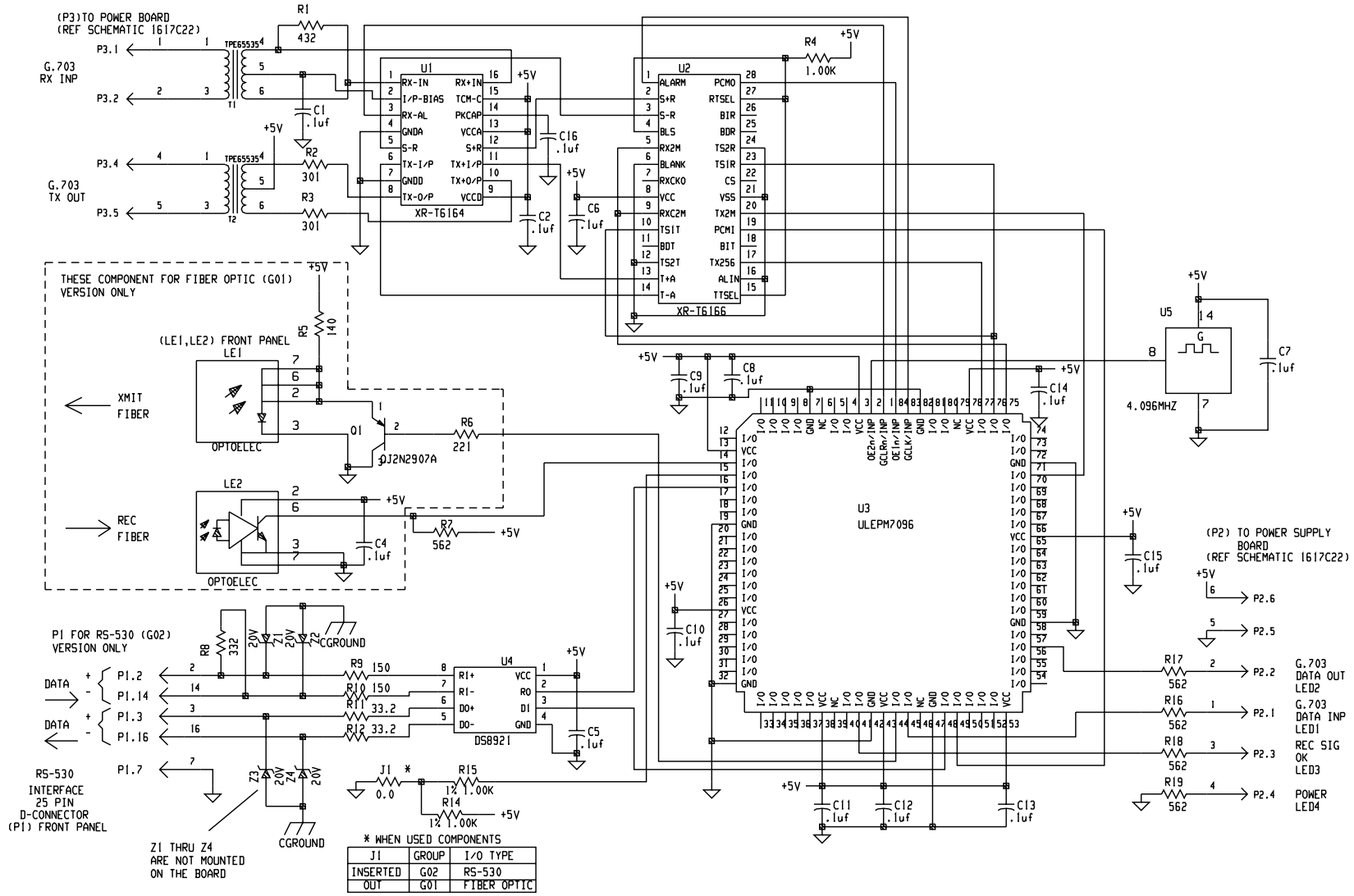
G.703 **1** **R**

Input Voltage

1 - 48 Vdc
2 - 125 Vdc

Interface Type

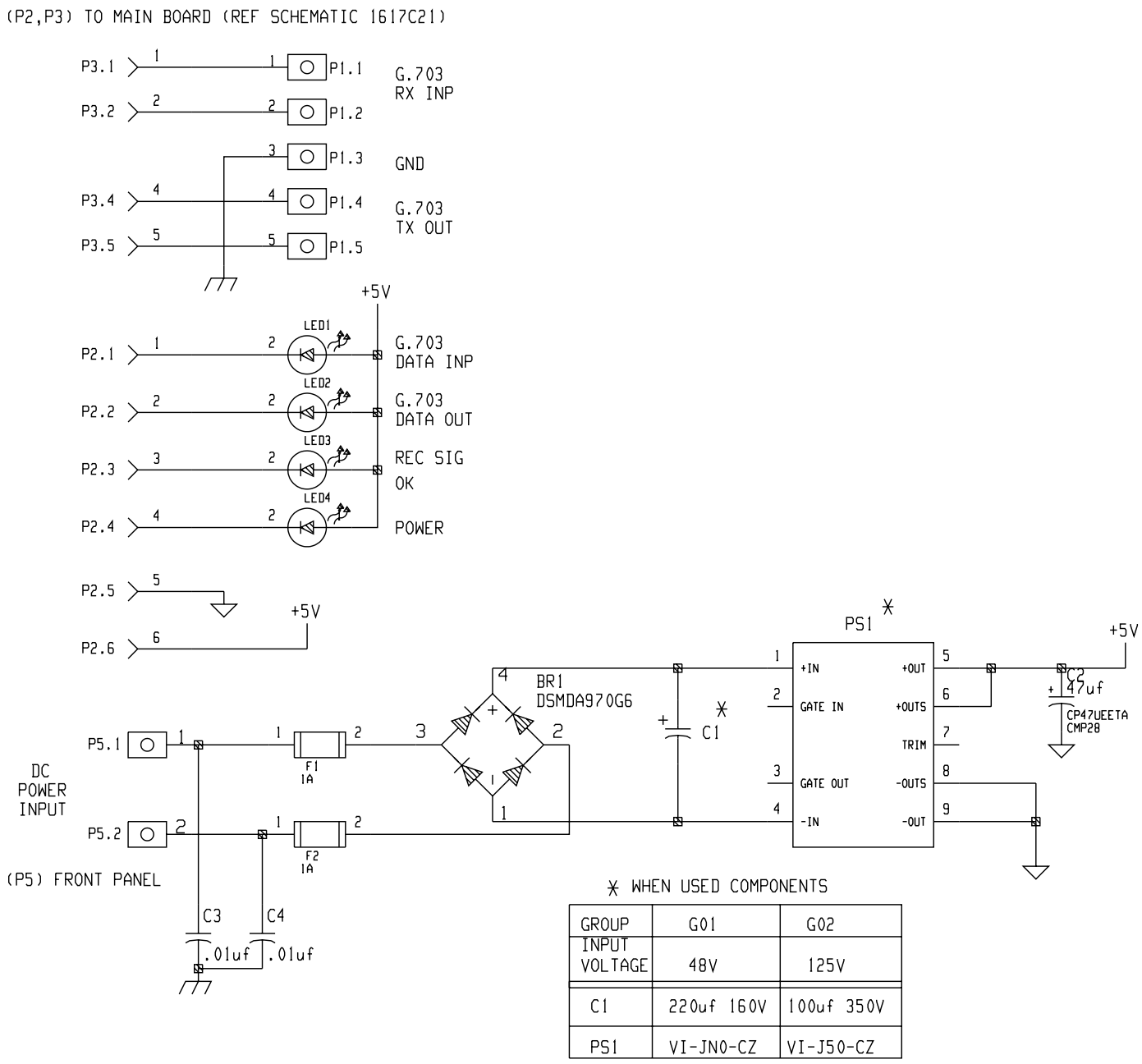
R - RS 422/RS 530
H - Fiber Optic
850 nm
ST Connector



J1	GROUP	I/O TYPE
INSERTED	G02	RS-530
OUT	G01	FIBER OPTIC

Sub 1
1617C21

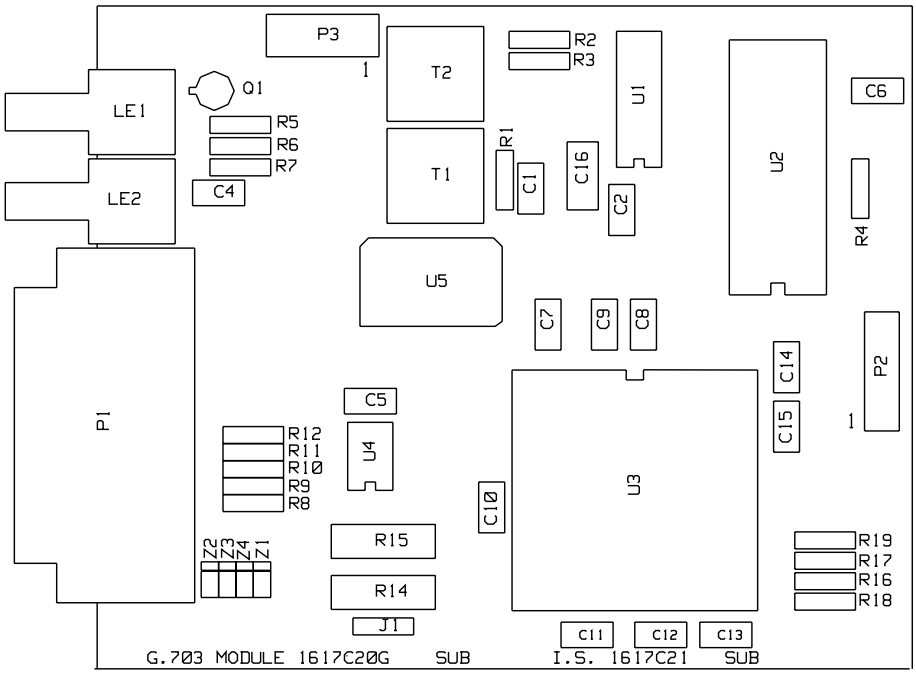
Figure 3. Internal Schematic (Main Module)



GROUP	G01	G02
INPUT VOLTAGE	48V	125V
C1	220uf 160V	100uf 350V
PS1	VI-JN0-CZ	VI-J50-CZ

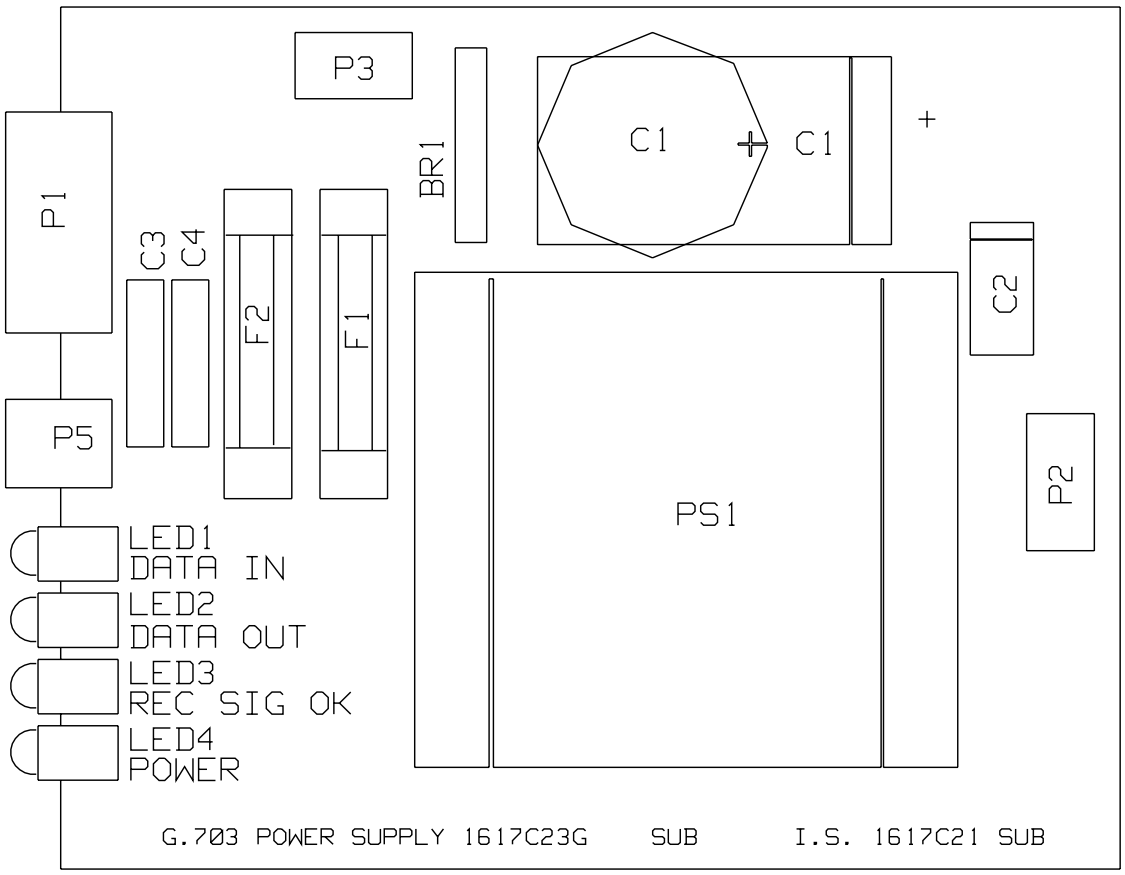
Sub 1
1617C22

Figure 4. Internal Schematic (Power Supply)



Sub 1
1617C20

Figure 5. Assembly Drawing (Main Module)



Sub 1
1617C23

Figure 6. Assembly Drawing (Power Supply)

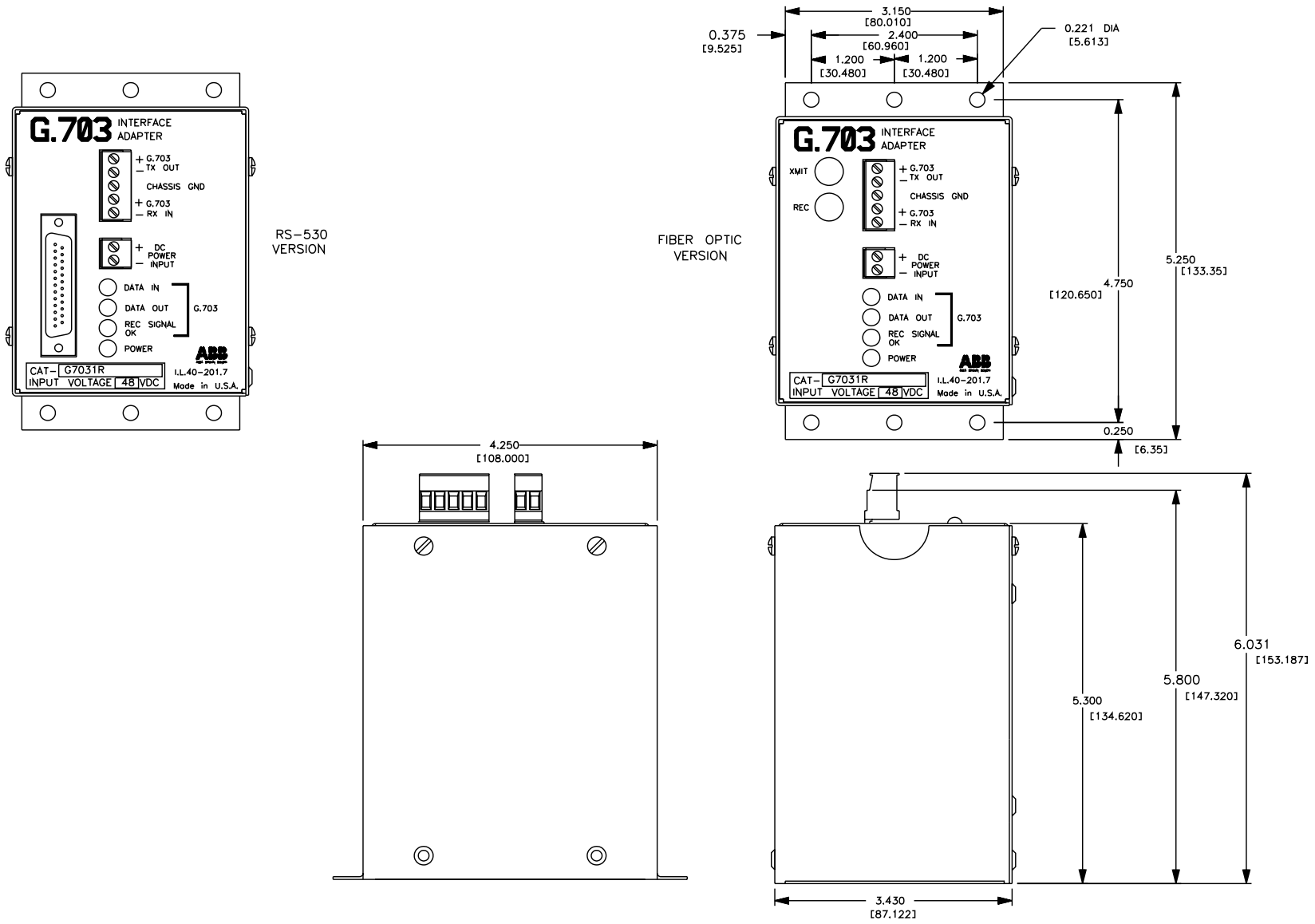


Figure 7. Outline Drawing

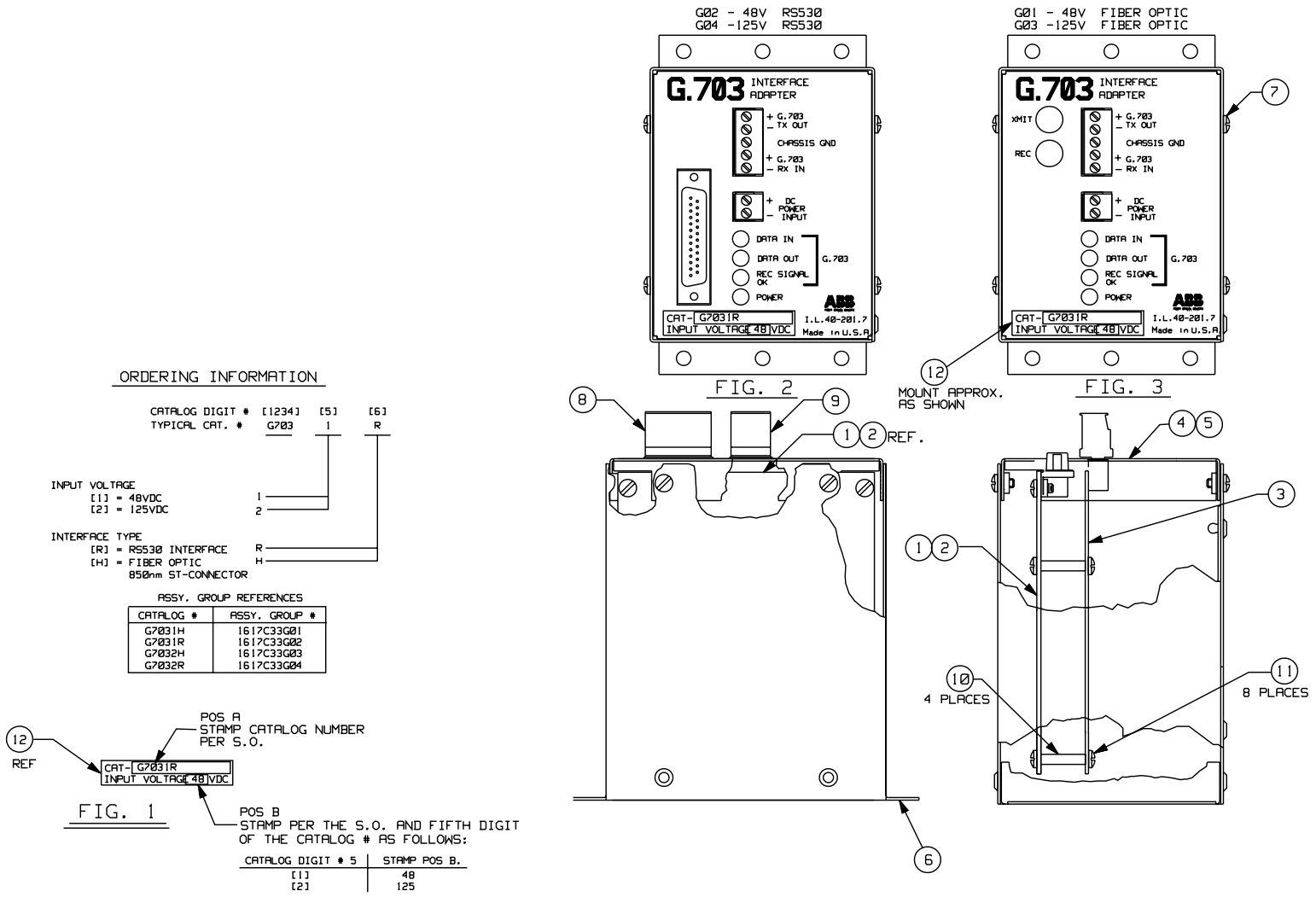


Figure 8. General Assembly

Sub 1
1617C33