Reliable high-temperature electronics

High-temperature electronics based on silicon-on-insulator (SOI) technology allows electronic circuits and systems to be operated continuously at temperatures in excess of 225 °C and yet still exhibit a long lifetime. This technology is being used for the so-called 'downhole' electronics in an 'intelligent well' system developed by ABB for offshore oil and gas production. Besides meeting industry needs for higher reliability and functionality, it enables complex oil and gas reservoirs to be developed more efficiently and economically. Other areas of application are in the automotive and aerospace industries

The term 'high-temperature electronics' refers to electronic circuits and systems designed to work at temperatures beyond 125 °C, which is the maximum operating temperature for most commercially available electronics. Although not based on scientific fact, this definition demonstrates a technological limit that the industry has shaped over the last few decades.

Using SOI[1] integrated circuits, it is possible today to design and manufacture electronic systems capable of a long lifetime in continuous operation at elevated temperatures of, eg, 225 °C. Such systems can even be operated at 300 °C, although at the expense of a shorter lifetime. The range of reliable 'standard' components available, however, is very limited and choosing suitable devices for specific applications represents a major challenge to system and hardware designers alike.

[1] Silicon-on-insulator

ABB Offshore Systems, in close cooperation with ABB Corporate Research as well as other ABB units, is about to begin manufacturing a highly reliable 'intelligent well' system for the extremely harsh environment in which downhole oil and gas equipment has to work. The system is based on SOI technology and will enable oil companies to develop complex oil and gas reservoirs in an efficient and cost-optimized way.

Applications and current ABB activities

At ABB Corporate Research in Norway there are two electronics application areas with harsh environments that call for special precautions. The first involves digital coding ASICs for space applications [1], a project undertaken for the European Space Agency (ESA), and the second an electronic system for high-temperature downhole oil and gas applications. Although the environment in each case is very different, the consequences for the electronics in general and for the integrated circuits in particular have a lot in common.

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1 shows the 'intelligent well' system. Flowlines carrying the product run from the wellhead on the sea bed to a host facility, in this case a floating production system. The wellhead is connected to the producing zones of the reservoir, where the fluid collects in the tubing string before being transported to the host facility. Since the reservoir can have a number of producing zones, it may be necessary to control the fluid inflow at various downhole junctions. This is done by controlling either sliding sleeve devices or downhole chokes using an electronic control and data acquisition system located within the hole. In order to optimize production, data are needed from various downhole sensors, the main tasks of which are to measure the pressure, temperature, water-cut in the produced fluid, and total flow. This kind of downhole active control and monitoring of several zones and branches is relatively new and involves much more 'downhole electronic intelligence' than in the past. Very few installations are actually in place and these are very simple in terms of the number of controllable downhole devices they have.

Experience with downhole electronics is generally limited to the equipment used for drilling, which only needs to be operated for a few weeks at a time. Production experience is restricted to one pressure and one temperature sensor (often redundant), and these are renowned for having a lifetime of only a few months at best on account of the very harsh environment in which they work. Much higher

reliability and higher functionality will be needed for the next-generation systems if the oil companies are to succeed in developing complex fields. The prospective rewards, however, are huge.

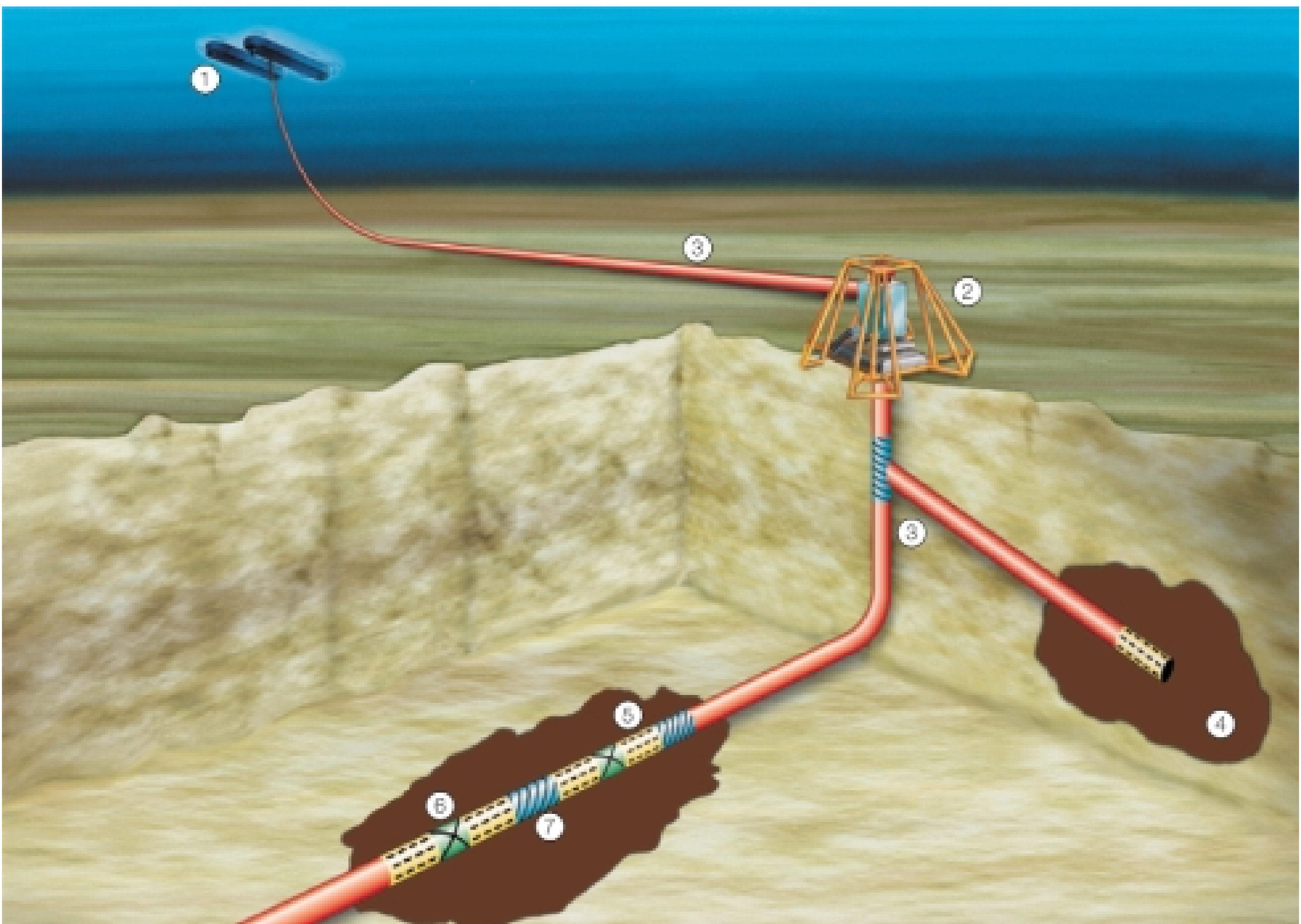
A typical downhole electronic system is illustrated in **2**.

Application characteristics and considerations that will affect the intelligent well electronics needed in the future can be summarized as follows:

- Environmental temperature above 200 °C for the whole of the equipment's lifetime.
- Distance between the wellhead and the electronics modules furthest away may be in excess of 10 km.
- Very harsh environment, including aggressive chemicals and very high pressures.
- Very limited space for the electronics modules as well as for cables and cable penetrations.
- Installation is subject to very severe mechanical and environmental conditions.
- Lifetime and system availability requirements are 10 to 20 years for worst-case environmental specification (eg 225 °C).
- Retrieval of downhole (failed) devices is extremely costly, being neglected entirely in most current installations.
- Electronic systems under development must support downhole devices (sensors and actuators) being developed and consequently at a stage where specifications are likely to change with time.
- Experience with electronic downhole systems has indicated low reliability and lifetime; very rudimentary investigations of the causes of actual failures have been made (due among other things to the high retrieval costs). The intelligent well system is much more complicated than previous systems and 'conceptual' solutions vary from vendor to vendor and from customer to customer. Customers and end-users

'Intelligent well' system for efficient and cost-optimized development of complex offshore oil and gas reservoirs **1**

1 *Floater*
2 *Wellhead*
3 *Oil/gas production tubing*
4 *Oil reservoir*
5 *Inflow section*
6 *Sensors*
7 *Downhole chokes*



(ie, the oil companies) are currently trying to ‘standardize’ solutions.

- The electronic system function does not seem to be very much more demanding than a ‘normal’ land-based system, but the lack of reliable standard electronic components still makes it hard to arrive at a good and reliable system concept.

As already mentioned, several ABB units and research centers are involved in the development of the ‘ABB Intelligent Well’ system **2**. ABB Offshore Systems is responsible for the overall system and is the ‘product owner’. Responsibility for developing the downhole electronic system, SOI ASICs design and system testing lies with ABB Corporate Research in Norway. Researchers in Germany are responsible for evaluating methods for ‘die attach’ and wire bonding, for selecting materials and discrete electronic components suitable for the downhole system design, and for the system aging tests.

During the electronic system design the focus was mainly on the following areas:

- Flexibility, to enable the system to cope with both simple and complex downhole configurations, ie the number of downhole controllable devices and the distance between them can be virtually unlimited.
- System partitioning, with the goal of making sure that the SOI ASICs in the system solution are the same for all configurations except the interface ‘close to’ the actual controllable devices, eg the (often analogue) sensor element interface or an actuator interface, which in most cases has to be customized.
- Incorporation of as much logic as possible in the SOI ASICs, for maximum reliability and a minimum number of ASICs according to the principle of ‘the simpler the better’. The few discrete components that are necessary are dimensioned for the large parameter span that can be expected over a long lifetime at high temperatures.
- Redundancy, to ensure that maximum operability is maintained in the event of component errors. No intricate high-temperature ‘switching’ devices for bypassing errors are used. Neither are intricate cooling devices of questionable lifetime needed.
- Downhole administration; these tasks are located at the ‘cold seabed controller’, where higher complexity can be tolerated without compromising system availability (this device can be retrieved).
- Degree of redundancy; this can be selected in each well installation without having to make any changes to the electronic design.

A point worth mentioning, and which is especially true for high-temperature designs, is that a successful design starts at the system level. The use of SOI ASIC technology is a vital factor in achieving ‘sufficient’ reliability.

Global market for high-temperature electronics

The commercial market for high-temperature electronics (HTE) has been insignificant in the past and R&D efforts directed at HTE by the electronics industry correspondingly limited, in spite of numerous scientific applications. Over the last decade or so the number of industrial applications that have pushed the limits to the extreme has increased and the basic material technology has matured. As a result, the semiconductor industry is now starting to speed up development and prepare for production.

HTE applications abound in industry, ranging from the automotive sector to petroleum well-logging, avionics and aerospace technology.

The total market potential for HTE is currently estimated at about US$ 10 billion, and is expected to increase to US$ 17 billion by the year 2005 [6]. The ‘actual market’ forecast for the year 2005, is US$ 1 billion, or 6 % of the total potential HTE market. Even this low penetration calls for large investments by the electronics industry.

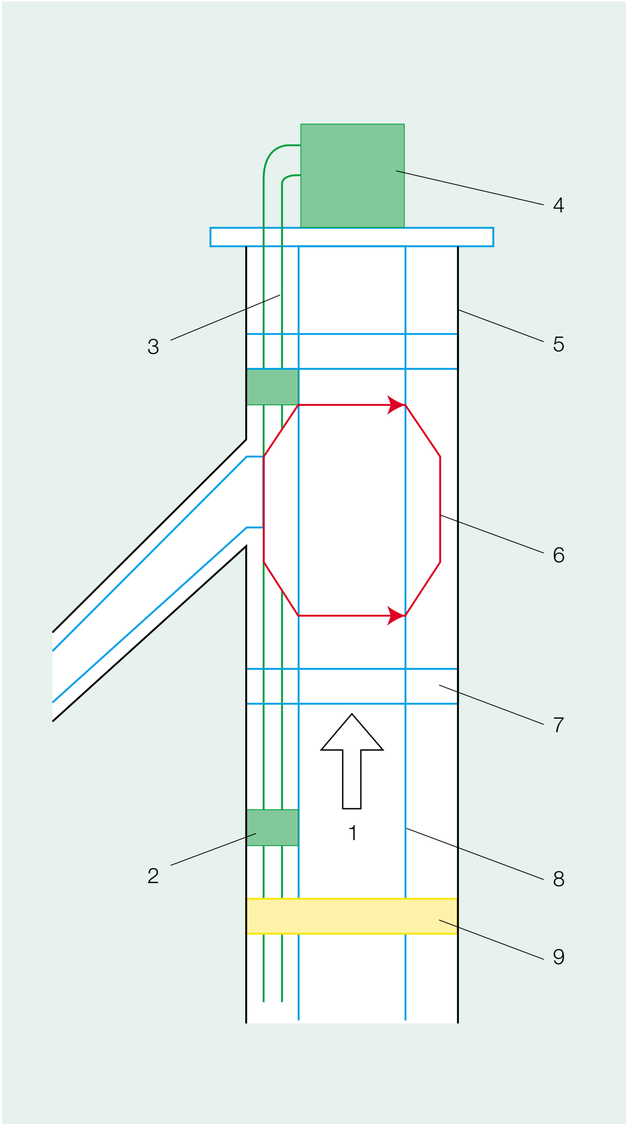
The largest application area for HTE is in engine, exhaust and brake control in the automotive industry (200 to 250 °C), which is expected to make up 65 % of the market by 2005. Well-logging (250 °C) and aerospace (max 800 °C) are the next two largest application areas, each of which is expected to comprise about 14 % of the market. These figures show that the HTE business still has to be driven by the impact of the application and not the profitability of the component business as such.

HTE technology development receives help, however, from another market not requiring high-temperature technology directly. The much bigger telecommunications and computing markets are in need of technology for very high-density and very high-speed components. Since the SOI serves all of these markets, heavy investments are being made in this technology to push it forward.

SOI technology, although currently the most mature high-temperature process, is not suited for high-current applications at all. Thus, another technology is needed for the latter.

‘Standard’ electronic components and semiconductors for the 200 °C range

All electronic modules consist of different components, such as semiconductors, passive components, substrates, wires, connections and packages. The semicon-

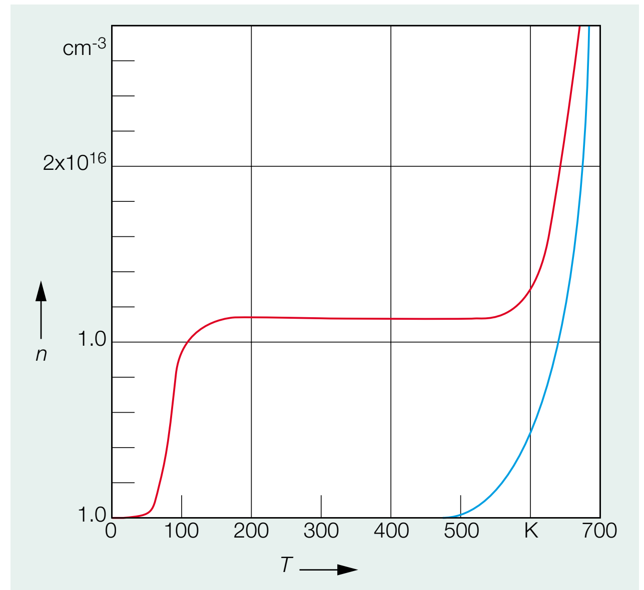


Typical electronic system for use in harsh downhole environments **2**

1 *Flow*
2 *Electronic module*
3 *Communication and power cables*
4 *Seabed control*
5 *Casing*
6 *Sliding sleeve choke*
7 *Packer*
8 *Production tubing*
9 *Flowmeter*

Electron concentration, n, as a function of the temperature, T, in n-type silicon **3**

Red *Electron density*
Blue *Intrinsic carrier concentration*



ductors can be divided into two groups: specially designed high-temperature devices, which will be discussed later, and the ‘low-temperature’ devices, which are usually screened and tested before being used in high-temperature environments. Experience has shown that the results with the latter are unsatisfactory, mainly because their lifetime and characteristics are unpredictable in the long term [7]. These components include devices designed to military specifications and high-power transistors/diodes that can operate with a junction temperature as high as 180 °C.

‘Passive components’ is a generic term for resistors, capacitors, magnetic materials, etc. In the case of resistors and capacitors it is the stability of the materials used and their inter-diffusion which are the main problems. Deposited resistors, such as Ni-Cr, Cermet (Cr-SiO) and thick-film resistors (eg, Ruthenium silver) have been shown to be most reliable and have the lowest temperature coefficients (200 ppm/K). NPO and glass dielectric capacitors are reliable up to 300 °C, but available capacitance values are limited to less than 0.33 μF with restricted voltage ratings. The main issues in the case of high-temperature capacitors are the dissipation factor, capacitance change and lifetime.

The characteristics of the magnetic materials can be described by the Curie temperature of the core and the hysteresis curve. Often, materials with a high Curie temperature exhibit low permeability and this makes a high-temperature inductor larger than its low-temperature equivalent. Although some types of organic printed circuit board have been shown to resist temperatures as high as 250 °C, experience with HTE shows that ceramic-type substrates are much more reliable.

Table 1
Semiconductor overview

	Bulk Si	SOI/ SIMOX	GaAs	SiC	III-V	Diamond
Bandgap (eV)	1.1	1.1	1.3	2.9	3.5 – 6.4	5.5
’Usable’ temperature (°C)	150	250	300	>600	>600	>1000
Maturity	Very high	Medium	High	Low	Very low	Very low

The latter technology has been used for thick- and thin-film circuits for many years. Ceramic substrates exhibit superior heat conduction and high-frequency characteristics compared with the organic types; in addition, the resistors and capacitors can be used directly on the substrate.

The range of semiconductor devices for high-temperature applications is very limited, although the SOI SIMOX[2)] semiconductor technology is maturing. While silicon is the most technologically mature semiconductor material presently available, it is not reckoned to be the ‘best’ one in the long run.

As will be explained, the higher the bandgap value of a semiconductor, the better it can be expected to perform at elevated temperatures. A summary of the semiconductors in use is given in *Table 1*.

The information given in this table serves only as a rough guide and does not claim to be ‘scientific’ in any way. The important message it carries is that the most promising candidates for the 200 °C regime applications will be found in the next few years among the SOI and SiC technologies. Single devices from the less mature materials have been studied scientifically, but they are years away from industrial application. Gallium arsenide (GaAs) is available but most applications are in the high-frequency and optical domains. Very little attention is paid to it for high-temperature applications, even though its prospects seem to be slightly better than those of silicon.

Basic temperature effects in (Si) semiconductors

The basic physics and properties of semiconductors are well understood and have been explained in a vast number of textbooks. Today’s extremely high silicon device production volumes are driving development and refinement of the devices at such a fast rate that the cost per function is dropping steadily. However, the market for high-temperature or radiation-tolerant devices makes up only a small fraction of the total market, so that there are relatively few vendors and costs are affected unfavourably. SOI technology, having been around in different forms for decades, has reached a stage of maturity today that makes conventional design and production completely feasible.

There are four basic physical properties that tend to dictate the performance of semiconductor devices at high temperature:

- Intrinsic carrier concentration
- Leakage current
- Carrier mobility
- Threshold voltage

Intrinsic carrier concentration

The intrinsic carrier concentration, n_i, is the number of ‘free’ electronic charges in a pure, undoped semiconductor with an equal number of free electrons and holes. It varies with the semiconductor lattice vibrational energy and hence with temperature, as well as with the gap energy, E_g, required to ‘break the bond’ or move an electron from the valence band, in which it does not contribute to conduction, to the conduction band, where it is ‘free’ to move in an electric field. In a state of equilibrium:

$$n_i = (p\,n)^{1/2} = \text{constant}\ T^{3/2}\, e^{(-E_g/2kT)} \qquad (1)$$

where n and p are the electron and hole density, respectively, k is Bolzmann’s constant and T the absolute temperature. The importance of eqn (1) becomes clear when a look is taken at the basic pn-junctions that all integrated circuits depend on. The pn-junctions are obtained when one part of the semiconductor is doped with an acceptor impurity, typically boron, and another part with a donor, typically phosphorus. At the interface between the n- and p-regions there will be a pn-junction, and a space charge region will form. MOS[3)] transistors likewise depend on the formation of a space charge region under the gate area.

From eqn (1) it is seen that n_i increases exponentially with the temperature. When n_i equals the donor density in the n-region the semiconductor becomes totally intrinsic and the space charge regions vanish.

[2)] Separation by implanted oxygen
[3)] Metal-oxide silicon

At this high temperature, about 400 °C in silicon and increasing somewhat with increasing doping levels, no transistors will operate [2]. This is illustrated in **3**.

The flattening out of n in **3** is due to the fully ionized donor concentration. The exponential dependence of T in the intrinsic concentration, n_i, is visible and dominates the total electron concentration so that semiconductor becomes intrinsic, as shown by the steep part of the curve on the right-hand side of **3**.

Thin-film SOI MOS transistors capable of operating at more than 350 °C are being manufactured today.

Eqn (1) also shows the exponential dependence of E_g, which explains why semiconductors with higher bandgap values than silicon are attractive for high-temperature operation. Si has a bandgap of 1.1 eV at room temperature, GaAs 1.34 eV with an intrinsic limit of about 650 °C, SiC 2.9 eV and a limit of about 1000 °C, and GaN 3.45 eV with an even higher intrinsic temperature.

Leakage current

The leakage current is another fundamental property that places limits on the operation and design of high-temperature integrated circuits. The reverse biased n+p-junction has a leakage current, I_r, [3] which is given by

$$I_r = q\,A_j\,n_i\,W_j\,/\,\tau_e + qA_j\,(D_n/\tau_n)^{1/2}\,n_i^2/N_a \quad (2)$$

where q is the electronic charge, A_j the junction area, n_i the intrinsic carrier concentration, W_j the junction width, τ_e the effective carrier lifetime for the carriers thermally generated in the space charge region, D_n the electron diffusion coefficient, τ_n the electron lifetime in the neutral p-type material, and N_a the acceptor doping concentration. The first term is the leakage carrier contribution made by carriers thermally generated in the space charge region and swept out of this region by the strong electric field existing in it. The second term is the diffusion component stemming from the carriers within a diffusion length from the space charge region, and which diffuse to the space charge region, where they are swept out.

From eqn (2) it is seen that the generation current varies with n_i and the diffusion current with n_i^2 . From eqn (1) it is known that n_i varies exponentially with temperature. In fact, it has been experimentally verified that the generation current dominates below 100 to 150 °C and the diffusion current above that. It is also observed that semiconductors with larger bandgaps exhibit lower leakage currents than those with smaller ones.

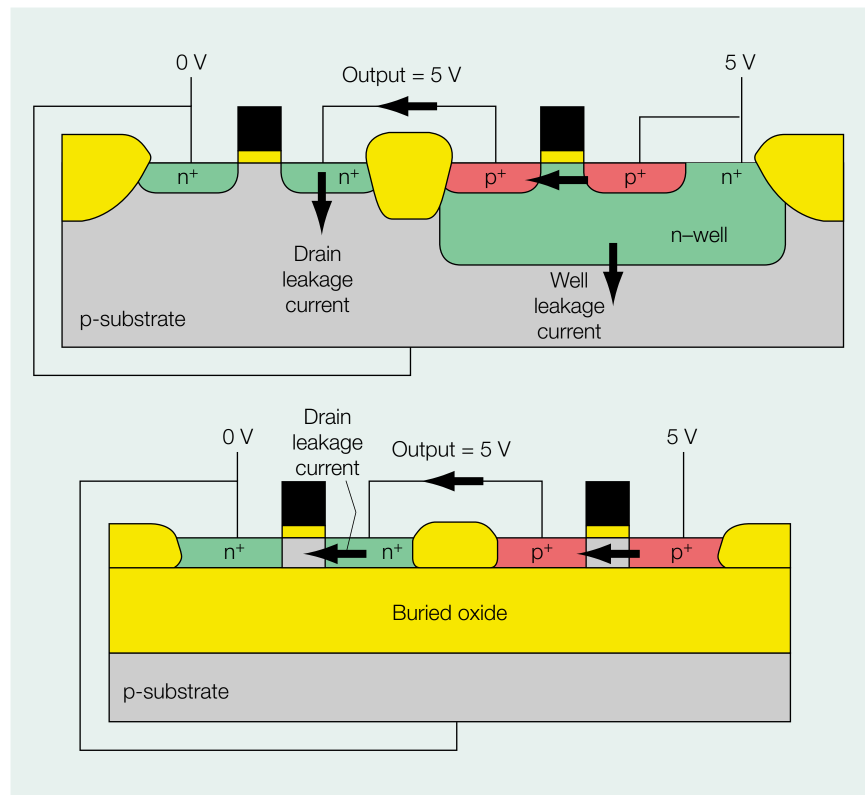
Also observed is the fact that the leakage current is proportional to the junction area, A_j, while looking at **4** it is seen that the large junction areas, the drain and especially the well that dominate the leakage current in bulk CMOS are completely absent in the SOI structure, being replaced by the interface to the buried oxide insulation.

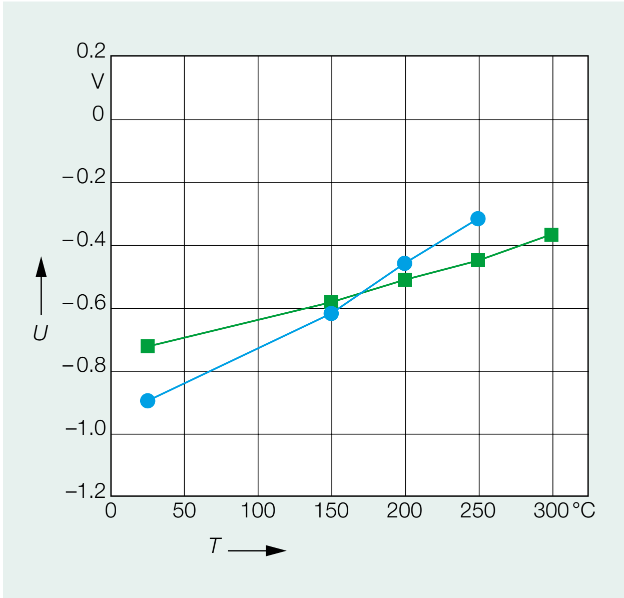
Ordinary bulk CMOS integrated circuits show a loss of functionality above about 240 °C due to the high leakage current, while SOI functionality has been demonstrated up to 350 °C. The leakage current of SOI is about two to three orders of magnitude less than that of bulk CMOS at high temperatures (200 to 300 °C).

Carrier mobility

Carrier mobility in the channel of an MOS structure, both in SOI and bulk CMOS, is highly influenced by the surface effects in the channel formed under the gate of the transistor, ie by the interface between the silicon and silicon dioxide. The surface scattering effect associated with this inter-

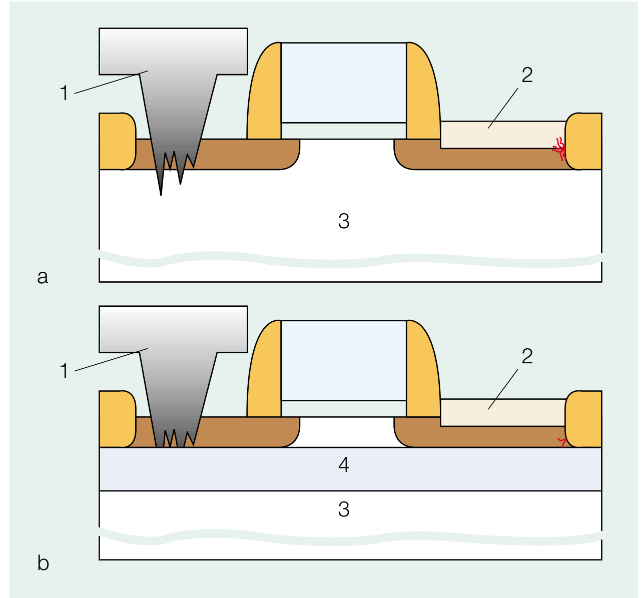
An inverter in bulk CMOS (top) and in SOI technology (bottom) **4**





Threshold voltage U as a function of temperature T for bulk CMOS and SOI **5**

Bulk CMOS
SOI



Metallization in SOI (a) and silicon bulk (b) **6**

1 *Metal*
2 *Silicide*
3 *Silicon substrate*
4 *Insulator*

face reduces mobility significantly from its bulk value, which is theoretically dominated by lattice scattering having a $T^{-3/2}$ dependence. The reduction is a function of the process of gate oxide formation. Because of this, the experimental dependence of mobility, μ, as a function of temperature is often given [4] as:

$$\mu(T) = \mu(T_0)\,(T/T_0)^{-m} \qquad (3)$$

where T_0 is the room temperature and m a value between 1.5 and 2, implying that the mobility is reduced by a factor of 2 to 4 at high temperatures.

Another factor on which the channel mobility depends is the surface potential under the gate of the MOS transistor, often resulting in a somewhat higher mobility for thin-film SOI MOS transistors than for bulk equivalents [5].

Threshold voltage

The threshold voltage, V_{th}, of the bulk MOS transistor decreases with increasing temperature. If it becomes too low a significant current will flow between the source and drain even if no voltage is applied to the gate, making the transistor useless. The threshold voltage for an n-channel bulk transistor is given by [5]:

$$V_{th} = V_{FB} + 2\varphi_F + \gamma\,(2\varphi_F + V_{SB})^{1/2} \qquad (4)$$

where $\gamma = C_{ox}^{-1}\,(2\varepsilon_{si}\,q\,N_a)^{1/2}$

and where V_{FB} is the flatband voltage, φ_F the Fermi potential, V_{SB} the source to bulk potential, C_{ox} the gate oxide capacity, ε_{si} the dielectric constant of silicon, and N_a the acceptor concentration. γ is called the body effect factor, which indicates the dependence of the body potential on the threshold voltage. The term involving γ in eqn (4) is due to the maximum depletion width under the channel.

The Fermi potential, again for an n-channel transistor, is given by:

$$\varphi_F = (kT/q)\,ln(N_a/n_i) \qquad (5)$$

From eqns 1, 4 and 5, it can be deduced that the threshold voltage decreases approximately linearly with increasing temperature, and once again it is seen that the intrinsic carrier concentration dictates the temperature dependence. The threshold voltage temperature coefficient for bulk devices is about 3 to 5 mV/deg.

For thin-film SOI MOS transistors, however, the film thickness may be so small that it is fully depleted and the maximum depletion width becomes almost independent of the temperature. Hence, the threshold voltage temperature coefficient is only about 1 mV/deg, as illustrated in **5**.

Based on the fundamental semiconductor properties and their dependence on temperature, it is now possible to summarize some relevant secondary effects

that are also very important for successful utilization of the high-temperature technology available.

Lifetime killers in high-temperature semiconductor devices

Electromigration

Electromigration – the process by which metal ions are moved at high current densities – is one of the major failure mechanisms in high-temperature applications. It results in the metal tracks on integrated circuits exhibiting increased resistance, eventually causing an open circuit, and is exponentially dependent on the temperature. Silicon vendors are therefore making a great effort to select suitable materials and establish layout rules that overcome this problem.

Metal-to-silicon electrical contacts

All kinds of metal-to-silicon electrical contacts are prone to error at high temperature. Once again, SOI is better than bulk in this respect, as illustrated in 6 [5].

Careful consideration also has to be given to techniques for wire bonding between the silicon chip and the substrate to which the chip is attached.

Hot carrier effects

The hot carrier effects that occur in the high electric field areas of semiconductor devices are more pronounced at high temperature. These effects stem from carriers (normally the electrons) being accelerated to such a high energy that they destroy the silicon silicon-dioxide interface or even the silicon-dioxide material itself, thereby creating irrecoverable parameter changes, eg permanent lowering of the breakdown voltage or the threshold voltage. One ASIC vendor has reported hot carrier effects in the reverse current, which as a result changed by about 5 % over a 10-year period. The effects are not as important as the two former ones as long as the necessary precautions are taken during processing.

Dielectric degradation

Dielectric degradation is also known to accelerate with temperature, but careful testing shows that dielectric leakage current will not interfere with circuit operation at 10 V and temperatures below 300 °C.

Conclusions and further work

Based on the work done to date, it is recommended that SOI technology be considered for all electronic systems that are expected to operate reliably at elevated temperatures. Although SOI cannot be used for high-power applications, alternative technologies, such as SiC and GaN, can be considered. There is a definite need for SOI technology in the downhole application which has been described, and work on high-temperature power supplies and power distribution schemes is under way.

ABB Corporate Research in Norway is well equipped to carry out the digital and analogue design of SOI ASICs. ABB's first SOI ASIC has already been manufactured and is being used in ABB products. Design and manufacture of the second digital SOI ASIC is on track, as is the build-up of SOI analogue ASIC design competence. It is planned to use this technology in downhole equipment as soon as it becomes available.

References

[1] K. Asskildt: Development of radiation tolerant integrated circuits for satellites. ABB Review 3/92, 19–26.

[2] A. S. Grove: Physics and technology of semiconductor devices. J. Wiley & Sons, 1967.

[3] S. Sze: Physics of semiconductor devices. J. Wiley & Sons, 1981.

[4] D.C. Sheridan et al.: Evaluation of Si3N4/SiO2 stack and commercially available MOS capacitors for high temperature electronics. Trans. on Third International High Temperature Electronics Conference (HITEC), Albuquerque, New Mexico, June 1996.

[5] J. P. Colinge: Silicon-on-Insulator Technology. Kluwer Academic Publishers, 1991.

[6] The world market for high temperature electronics. HITEN report, AEA Technology, 1997.

[7] F. P. McCluskey, R. Grzybowski and T. Podlesak: High Temperature Electronics. CRC Press, 1997.

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