Instruction Leaflet

I.L. 41-775.1A

Type SLB
Breaker Pole Failure Relay
10 Amp Continuous Rating

Effective: April 1987
Supersedes I.L. 41-775.1 Dated June 1978
0 Denotes Change From Superseded issue

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. Printed circuit modules should not be removed or inserted while the relay is energized unless specific instructions elsewhere in this instruction leaflet state that such action is permissible. Failure to observe this precaution can result in an undesired tripping output and cause component damage.

APPLICATION

The SLB pole failure relay protects against breaker pole failure, i.e. "pole disagreement". Pole failure is here defined as having one or more breaker poles open while one or more poles are closed during non fault conditions. This relay is recommended for "single-breaker" applications. Where "ring-bus" or "breaker-and-a-half" configurations are used the SLB-1 relay is recommended (See IL. 41-775.2.)

Types of Breaker Pole Disagreement

1) Pole disagreement during the attempted clearing of a fault. This "breaker failure" condition is detected by conventional breaker failure relay and is cleared by tripping adjacent breakers in normal manner.

2) Pole failure during a breaker closure. This involves the failure of one or more poles to close during a breaker close operation, not involving a fault. This is detected by the SLB current comparison logic which trips the protected breaker after time delay, T2.

3) Pole failure during a breaker opening operation. This involves the failure of one or two poles to interrupt current during a breaker trip operation, not involving a fault. This is detected by the SLB current comparison logic, which calls for another attempt at tripping the protected breaker after delay T2. This attempt will probably not successfully interrupt the stuck pole(s). Therefore, the current comparison logic will continue to operate and ultimately time-out T3 which either operates 86BF to clear the adjacent breakers or alarms the operator.

The SLB outputs are connected as shown in the external schematic diagram 5.

As explained in the Operation section of this leaflet, the current comparison logic of the SLB has an output whenever one or more phase(s) carries current above the III level (6.5 mA) while one or more phase(s) carries current below the IL level (20 mA). Though these IL and III settings are factory calibrations and not intended to be changed by the user, other levels can be set in the field if necessary. The IL calibration range is 18 to 60 mA and the I H range is 40 to 500mA.

Optional Relay Application - Alarm Only

In some instances it may be desirable to alarm-only for the pole failure condition. This is illustrateci in Fig. 5B, the external schematic for the SLB with one timer. A suggested setting for T2 is approximately one second.

All possible contingencies which may arise during installation, operation or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding this particular installation, operation or maintenance of this equipment, the local ABB representative should be contacted.

CONSTRUCTION & OPERATION

The type SLB relay is a solid state package mounted in FT42 case (See I.L. 41-076). Referring to Fig. 3, the circuitry consists of 3 current to voltage transformers, 3 varistors, 3 sets of full wave rectifiers, 3 filters, 3 sensing circuits, 1 level detector, and a standard output circuit. It contains a 20-volt zener supply that energizes the relay logic. It also contains one (or two) timers for adjustable time delay applications. In addition, a telephone relay circuit (TR1) is included to keep the timer(s) deenergized until the level logic produces a "pole disagreement" output. This eliminates standby power dissipation in the timer power supply circuitry, keeping heat buildup inside the relay case to a minimum. All 3 transformers, TA, TB, TC have a center-tapped secondary which is connected to dc negative for a common ground. The transformer secondaries are connected to individual varistors to keep the secondary voltages at a safe level.

There are 2 sets of full wave rectifiers for each phase. The odd numbered diodes are used to rectify the quantities related to the I_H or high current. These quantities will be compared to a reference at the level detector. The even numbered diodes rectify quantities that will provide a signal for phase current detection. Rectified quantities are then filtered by a capacitor and the input to the current sensors is then kept at a safe value by means of zener diodes.

The level detector is adjusted by means of R45 & R46 to provide a 20-volt output whenever one or more phase current is equal to or greater than the "high-set" level (factory adjusted for 65 mA). This produces an output at TP9 if at least one of the phase currents drops below 20 mA as detected by the related current sensing circuit. The basic current sensing circuit consists of a transistor that is biased into a normally on condition for a phase current equal or greater than 20 mA. This biasing is performed through adjustments of R39, R40, and R41. If any phase current drops below 20 mA the related transistor (Q1, Q2, or Q3) will turn off allowing any output from the level detector to deliver power to the output circuit and thus producing a relay output.

The level detector output is delayed by about 15 ms to avoid undesired tripping due to normal breaker unsymmetries. This delay circuit consists of an R-C circuit, a zener diode, and an output transistor. The output of this time delay circuit is used as the B+ supply for the current sensing circuits. Figs. 5, 6, and 7 show some of the basic circuits described above. The SLB Relay produces telephone relay output which is delayed by means of the timer logic. Standard time delay ranges are 0.1 to 1.0 sec. asnd 0.2 to 4 seconds. Operation of the timer begins when an input signal to the starting transistors Q3 and Q11 is present at TP9 and an internal telephone relay contact (TR1) in series with the dc control voltage closes. The capacitor (C1) in the RC timing circuit begins to increase in voltage until it is greater than the voltage setting on the brush of the R48 potentiometer. At this point current will flow into the gate of the silicon controlled rectifier (Q2) which will conduct similar to the closing of a switch. This actuates the telephone relay (TR2) in the time set on the front dial.

The output contact (TR2) normally energizes a trip circuit, actuating the ICS contact as shown in the external connection diagram.

The rate at which the capacitor charges is determined by the rheostat setting. The charging rate is not a linear function of rheostat setting, since R6 gives a parallel resistive path. This has the effect of expanding the scale for short times and thereby permitting more accurate settings.

CHARACTERISTICS

A. Current Rating

Continuous	10 Amperes per phase
One Second	200 Amperes per phase

B. Operating Time *

Time Equal to Timer Settings

* Level Logic Time Delay & TRI Relay Time Delay Included In Timer Calibration.

C. Current Burden Per Phase

90 mA	.05 VA
5 A	11.5 VA

D. DC Burden

Timers Deenergized	0.10	Amps. continuous
One timer– 48 Vdc	0.20	Amps. additional θ
Two timer– 48 Vdc	0.40	Amps. additional θ
One timer–125 Vdc	0.15	Amps. additional θ
Two timer–125 Vdc	0.30	Amps. additional θ

θ = only during SLB relay operation.

E. Tripping Condition

At least one phase conducting 0.065 ampere or more while at least one phase is conducting less than 0.020 amperes.

F. Restraining Conditions

1) Sudden increase of current from 0.0 ampere to any value greater than 0.065 ampere in all phases, whether balanced or not.

2) Any sudden change in current, increase or decrease, balanced or not, as long as the minimum current is greater than 0.065 ampere in all three phases.

3) Simultaneous interruption of three currents, balanced or not.

G. Time Delay Range and Voltage Rating

Time Delay Range (Seconds)	Voltage Rating (Volts dc)
.10-1.0	48
.10-1.0	125
.10-1.0	250
0.2-4.0	48
0.2-4.0	125
0.2-4.0	250

H. Timer Reset Time

TR drop-out time = 0.1 sec. or less.

Discharge of timing capacitor; C1 is essentially instantaneous, the R-C time constant through R48 being less than 20 milliseconds, in most cases. However, the discharge path through R48 is limited by silicon voltage drops through Q2 and D7, totalling approximately through R48 down to about one volt and then more slowly through R6 down to zero volts.

I. Timer Accuracy

The accuracy of the time delay depends upon the repetition rate of consecutive timings, the supply voltage, and the ambient temperature. Self-heating has a neglibible effect on the time accuracy.

(1) Nominal Setting

The first time delay, as measured with the test circuit shown in Fig. 13, taken at 25°C. and rated voltage, will be within ±5% of its setting for settings of 0.2 seconds or less. For settings above 0.2 seconds, this accuracy will be ±3%.

(2) Consecutive Timings

Incomplete capacitor discharge will cause changes in time delay. These changes are a function of discharge rate. Timing accuracy for slow repetitions will be per Table I.

Table I

Relay Rating	Delay Between Readings	Accuracy as Percent of Setting
0.1-1.0 seconds	at least 3 seconds	±3%
0.2-4.0 seconds	at least 5 seconds	±3%

Timing accuracy for fast repetitions will be per Table II.

Table II

Relay Rating	Delay Between Readings	Accuracy as Percent of Setting
0.1-1.0 seconds	instantaneous	±5%
0.2-4.0 seconds	instantaneous	±5%

(3) **Supply Voltage**

Changes in supply voltage, between 80% and 110% of nominal, cause time delay variation of no more than ±3 milliseconds for settings of 0.3 seconds or less, and no more than ±1% for settings above 0.3 seconds.

(4) **Ambient Temperature**

Changes in ambient temperature cause changes in time delay. This variation in time delay is a direct function of capacitance change with temperature. Typical variation of time delay with temperature is shown in Figure 10.

SETTINGS

A. **Current Levels**

The I_H level is adjustable from 40 to 500 mA. The I_L level is adjustable from 18 to 60 mA. A setting of 20 mA is recommended. I_H should be set sufficiently high that it will not operate at light load when one phase current is below the I_L setting. It should be set no higher than necessary.

B. **Timer Settings**

A current comparison output condition could occur during a "breaker failure" in which case it is imperative that adjacent breakers be quickly cleared in order to maintain system stability. This is achieved through conventional breaker failure protection which incorporates a timer, device 62, which is set as fast as is required to maintain stability. This is very often a low setting (12 cycles or less) and is sometimes as low as nine cycles. The pole failure timers (T2 and T3) can be set considerably higher than the breaker failure timer, since system stability is not endangered. A suggested setting for T2 is one second.

The T3 timer, which either trips adjacent breakers via 86BF or optionally alarms to notify the operator that one of the breaker poles is stuck closed, should be set to coordinate with T2 with a comfortable margin. A suggested setting for T3 is two seconds.

Proper time delay is selected by turning the knob of potentiometers R47 and R50 (dialed).

C. **Indicating Contactor Switch (ICS)**

The only setting required on the ICS unit is the selection of the 0.2 or 2.0 ampere tap. This selection is made by connecting the lead located in front of the tap block to the desired setting by means of the connecting screw. The tap should be chosen to be compatible with the trip current that will flow through the coil. The ICS unit contacts will close and the operation indicator target will drop for any current above tap value.

EXTERNAL CONNECTIONS

Fig. 4 shows the external connections for the type SLB relay.

RECEIVING ACCEPTANCE

Make a visual inspection to make sure that there are no loose connections, broken resistors, or broken resistor wires.

Relay Check

A. Refer to Figs. 3 or 4.

B. Connect per test Fig. 14 and apply rated dc voltage.

C. Apply I_A = 15mA, I_B = I_C = 100mA. 18-20 volts peak output should be observed at logic PCB terminal #19, and telephone relay TR2 (and TR3 for 2 timer relays) should operate.

D. Apply I_B = 15mA, I_A = I_C = 100mA, and check relay output per step C.

E. Apply I_C = 15mA, I_A = I_B = 100mA, and check relay output per part C.

Timing Check

SLB timers and their dials are calibrated and set at the factory and should not be disturbed in the field. However, the maximum calibration point on the timer dial(s) may be checked to insure that the timers are operating properly.

The recommended test circuit for this check is shown in Fig. 13.

A. Connect per test Fig. 13 and apply rated dc voltage. Switch (S1) should be in the closed position.

B. Set I_A, I_B, & I_C = 1.0 amperes. Reset the electronic timer to zero.

C. Set SLB timer dial at the maximum calibration mark and open switch (S1). The electronic timer should display the time set on the SLB timer dial to within $\pm 3\%$.

D. Allow a minimum of 10 seconds between repeat readings.

E. Return setting to value desired for the application.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay vetically by means of the rear mounting stud or studs for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the moufiting screws may be utilized for grounding the relay. External toothed washers are provided for use in the locations shown on the outline and drilling plan to facilitate making a good electrical connection between the relay case, its mounting screws or studs, and the relay panel. Ground wires are affixed to the mounting screws or studs as required for poorly grounded or insulating panels. Other electrical connections may be made direcly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detail information on the FT case refer to I.L. 41-076.

ROUTINE MAINTENANCE

All relays should be checked at least once every year at such time intervals as may be dictated by experience to be suitable to the particular application.

CALIBRATION

Use the following procedure for calibrating the relay if the relay adjustments have been changed or disturbed. This procedure should not be used unless it is apparent the relay is not in proper working order.

A. **Level Detector** (**Refer to Fig. 12**)

1. Connect per test diagram Fig. 14 and apply rated dc voltage.
2. Apply $I_B = I_C = 0$, $I_A = 65$ mA or any other desired value for I_H up to 500 mA.
3. Monitor relay output at TP9 (current board Fig. 12 top left) and adjust R45 (trim-pot – same board) until full relay output (18-20 volts) each is *just* observed on an oscilloscope.
4. Reduce I_A by about 3 mA and adjust R46 (same board – top right), until output just drops to zero.
5. Increase I_A and relay output should be observed as current reaches 65 mA or some other desired I_H value.
6. Reduce I_A and recheck per step 4.
7. In general adjust R45 for pickup, and R46 for drop out until relay produces an output (full output) as current approaches 65 mA (or the desired I_H value) and drops out quickly if current is, then, reduced.

B. **Current Sensors (Refer to Fig. 12).**

1. Connect per test diagram Fig. 14 and apply rated dc voltage.

2. Apply I_A = 20mA, I_B = I_C = 1 Amp. Monitor relay output at TP9 (circuit board Fig. 12-top left).

3. Adjust R39 (circuit board – bottom left) until the first output indication (18-20 volts peak), is *just* observed on a scope. If relay was already picked up, adjust R39 until it drops out, and then adjust it again as specified above.

4. Reduce current I_A, observing the relay output. Complete relay output (Vo = 20) should be observed within 3mA. Recheck first output indication at 20mA.

5. Adjust R40 (bottom – center) per steps 3 and 4, this time setting I_A = I_C = 1 Amp, I_B = 20mA.

6. Adjust R41 (Bottom – right) per steps 3 and 4, this time setting I_A = I_B = 1 Amp, I_C = 20mA.

C. **Timing Check**

Check timers using procedure given under RECEIVING ACCEPTANCE.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data.

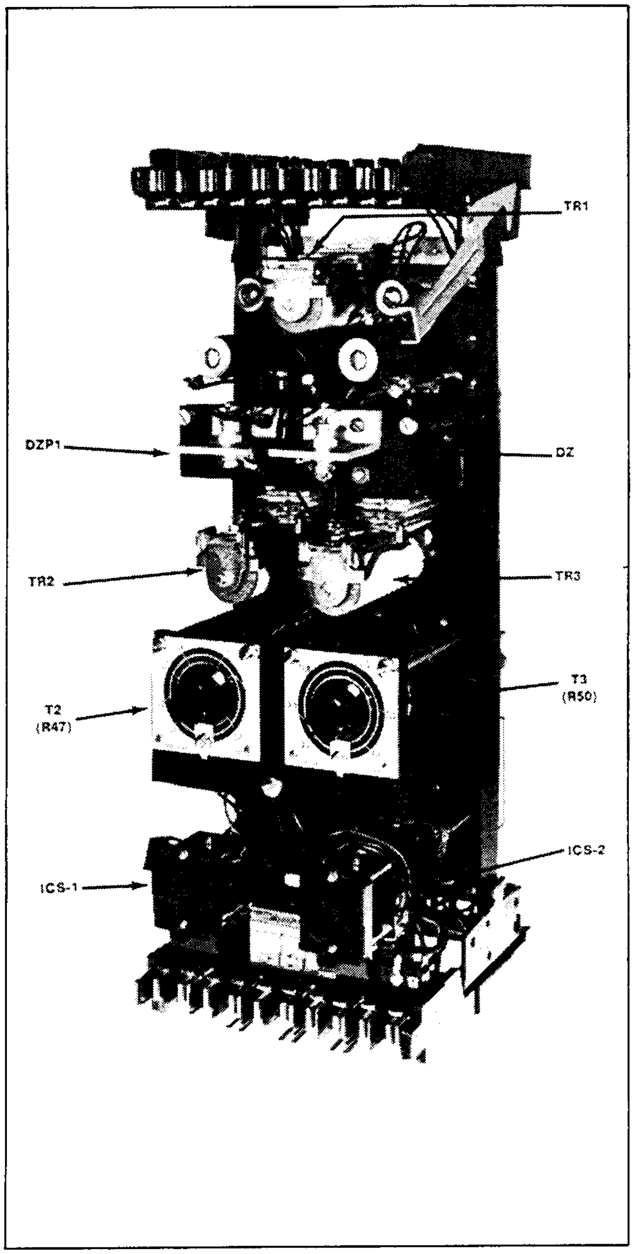


Fig. 1. SLB Relay (2 Timer) Chassis (Front View).

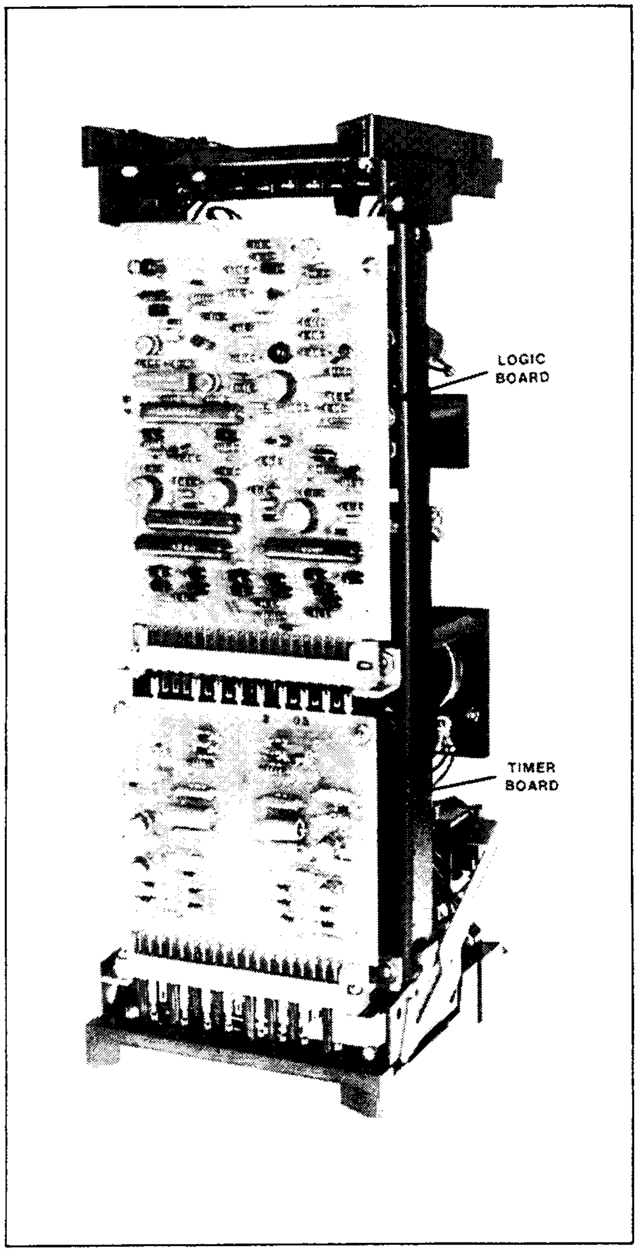
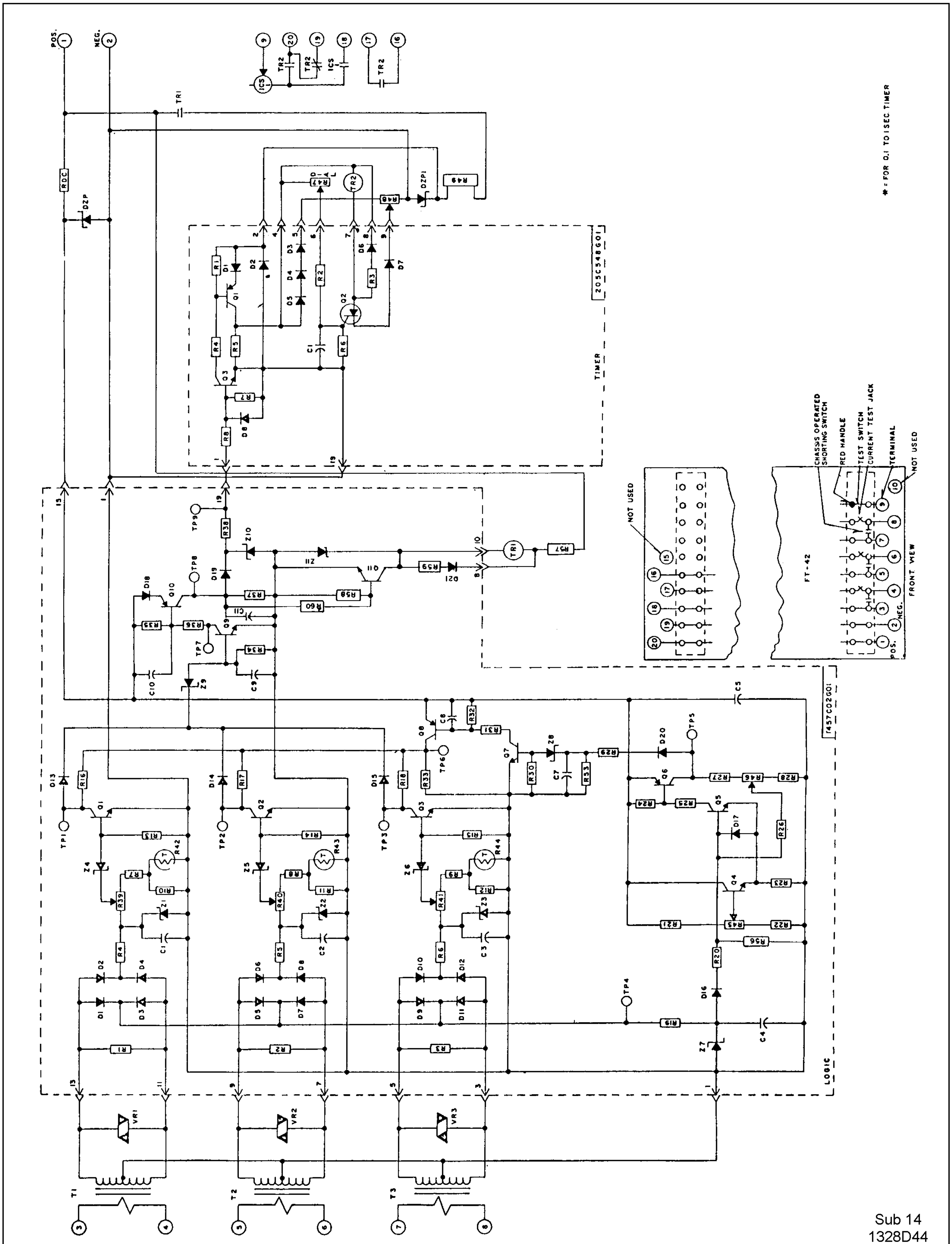


Fig. 2. SLB Relay Chassis (Rear View).

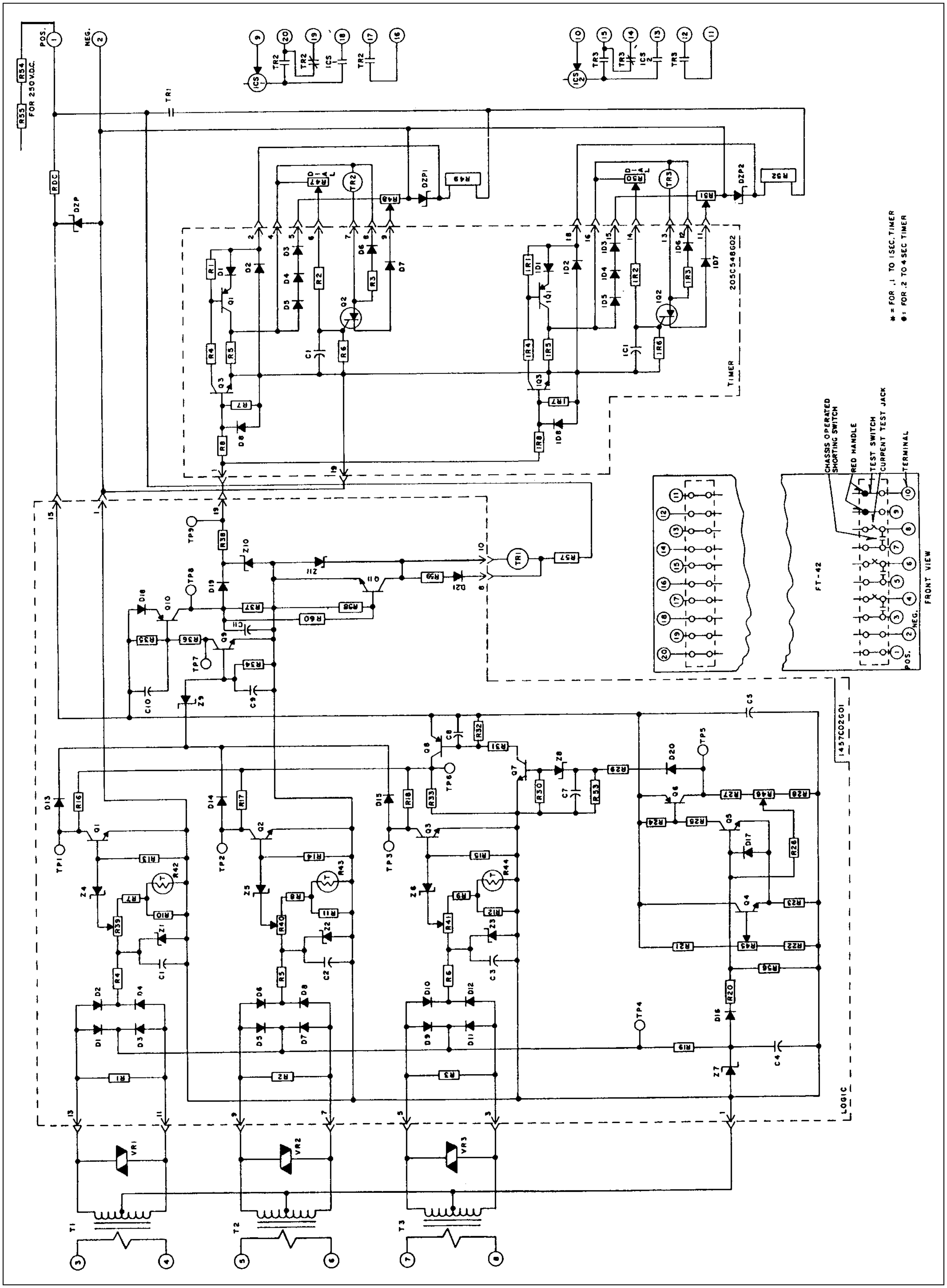


✪ *Figure 3. Internal Schematic SLB Relay (1 Timer).*

TIMER

CAPACITOR	STYLE	REQ.	REF.
C1	187A508H04	1	39 MFD.
DIODE			
D1 – D8	837A692H03	8	1N645A
TRANSISTOR			
Q1	184A638H20	1	2N1132
Q2	185A517H03	1	2N886
Q3	184A638H18	1	2N697
RESISTOR			
* R2	862A375H77	1	619Ω – 1/2W – ± 1%
R1 – R5	836A503H42	2	4,990Ω – 1/2W – ± 1%
R3	184A763H13	1	270Ω – 1/2W – ± 5%
R4	836A503H30	1	1,500Ω – 1/2W – ± 1%
R7	836A503H34	1	2,210Ω – 1/2W – ± 1%
R8	836A503H53	1	15K – 1/2W – ± 1%
* R6	862A377H77	1	61.9K – 1/2W – ± 1%
CAPACITOR			
C1–C2–C3–C8–C10	837A241H03	5	0.27 MFD
C4	876A409H09	1	1.0 MFD.
C5	187A508H10	1	18 MFD.
C11	3509A33H01	1	2.0 MFD
C7	837A241H16	1	2.2 MFD.
C9	876A409H01	1	.18 MFD.
DIODE			
D1 TO D12	188A342H11	12	1N4822
D13–D14–D15–D18	188A342H06	4	1N4818
D16 – D17	184A855H14	2	1N4385
D19–D21	837A692H03	2	1N645A
D20	184A855H07	1	1N457A
TRANSFORMER			
T1–T2–T3	2908300602	3	
TRANSISTOR			
Q11	837A617H03	1	2N3590
Q1–Q2–Q3–Q5–Q7–Q9	848A851H02	6	2N3417
Q4	184A638H18	1	2N697
Q6	184A638H20	1	2N1132
Q8 – Q10	849A441H01	2	2N3645
RESISTOR			
R28	184A763H41	1	3.9K 1/2W – ± 5%
R1–R2–R3	184A763H62	3	30K – 1/2W – ± 5%
R4 – R5 – R6 – R19	837A237H21	4	1200Ω – 11W – ± 5%
R60 – R25–R29–R32	184A763H47	3	6.8K – 1/2W – ± 5%
R10 – R11 – R12	629A531H67	3	30K – 1/2W – ± 2%
R13–R14–R15–R24 R30–R31–R34	184A763H51	7	10K – 1/2W – ± 5%
R16 – R17 – R18 – R35	184A763H59	4	22K – 1/2W – ± 5%
R20	184A763H61	1	27K – 1/2W – ± 5%
R21 – R22	184A763H35	2	2.2K – 1/2W – ± 5%
R23 – R36	184A763H43	2	4.7K – 1/2W – ± 5%
R26–R33–R37	184A763H73	3	82K – 1/2W – ± 5%
R27	184A763H53	1	12K – 1/2W – ± 5%
R38	762A679H01	1	150Ω – 3W
R46	629A430H01	1	50K – 1/4W – ± 20%
R42 – R43 – R44	185A211H05	3	20,000Ω – ± 10%
R45	862A406H02	1	20K – .5W – ± 10%
R48	185A067H05	1	250Ω
R49 (125 VDC)	1336173	1	560Ω – 40W – ± 5%
R49 (48 VDC)	04D1299H66	1	95Ω – 40W – ± 5%
R53	184A763H67	1	47K – 1/2W – ± 5%
ZENER DIODE			
Z1 – Z2 – Z3	849A515H05	3	1N4751A
Z4 – Z5 – Z6 – Z9	186A797H13	4	1N748A
Z8	188A302H17	1	1N3021B
Z10	862A288H01	1	1N3688A
DZP	762A631H01	1	1N2984B
DZP1	629A798H03	1	1N2986B
Z7	188A302H18	1	1N3035B
Z11	878A619H01	1	1.5 KE 200
VARSISTOR			
VR1 – VR2 – VR3	183A122H02	3	12K – ± 20%
TELEPHONE RELAY			
TR2	407C614H06	1	
TR1	407C280H19	1	
RESISTOR			
RDC (125 VDC)	1267293	1	1.5K – 25W – ± 5%
RDC (48 VDC)	1202587	1	400Ω – 25W – ± 5%
R47	184A756H01	1	40K
R39 – R40 – R41	629A430H05	3	200K – 1/4W – ± 20%
R7 – R8 – R9	629A531H60	3	15K – 1/2W – ± 2%
R57 (48 VDC)	1267283	1	800Ω 25W ± 5%
R57 (125VDC)	1208342	1	3550Ω 25W ± 5%
R58	184A763H37	1	2.7K 1/2W ± 5%
R59	184A763H13	1	270Ω 1/2W ± 5%
R56	848A821H13	1	49.9 1/2W ± 1%

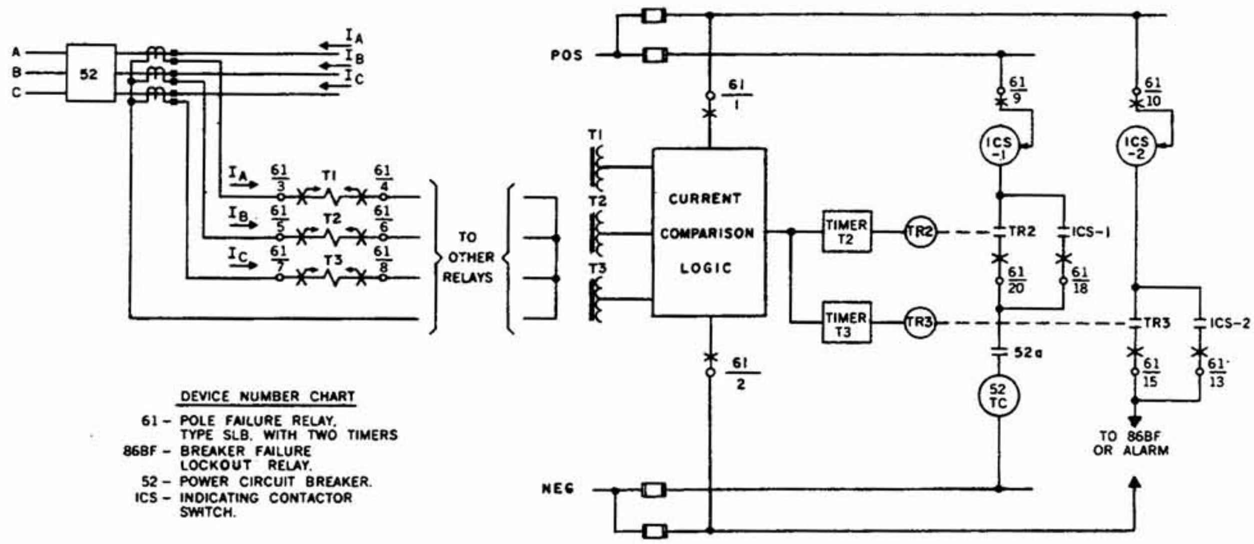
Sub 14
1328D44



✪ *Figure 4. Internal Schematic, SLB Relay (2 Timers).*

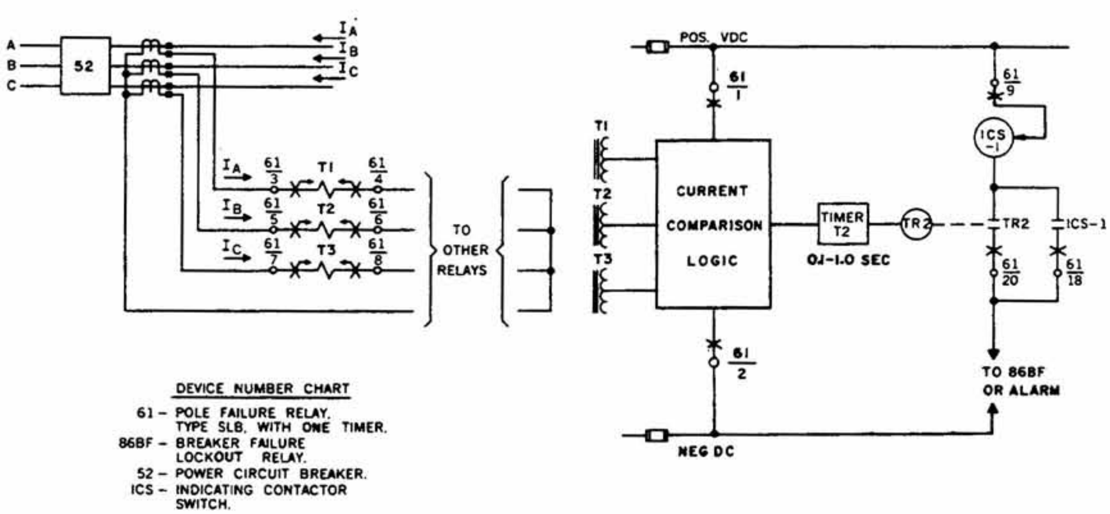
	CAPACITOR	STYLE	REQ.	REF.
TIMER	C1 - 1C1	187A508H04	2	39 MFD.
	DIODE			
	D1 TO D8 - 1D1 TO 1D8	837A692H03	16	1N645A
	TRANSISTOR			
	Q1 - 1Q1	184A638H20	2	2N1132
	Q2 - 1Q2	185A517H03	2	2N886
	Q3 - 1Q3	184A638H18	2	2N697
	RESISTOR			
	* R2	862A375H77	1	619 Ω - 1/2W - ± 1%
	R1 - R5 - 1R1 - 1R5	836A503H42	4	4,990Ω - 1/2W - ± 1%
	● 1R2	862A376H51	1	3.32 K - 1/2W - ± 1%
	R3 - 1R3	184A763H13	2	270Ω - 1/2W - ± 5%
	R4 - 1R4	836A503H30	2	1,500Ω - 1/2W - ± 1%
	* R6	862A377H77	1	61.9K - 1/2W - ± 1%
	R7 - 1R7	836A503H34	2	2,210Ω - 1/2W - ± 1%
	R8 - 1R8	836A503H53	2	15K - 1/2W - ± 1%
	● 1R6	862A378H42	1	267K - 1/2W - ± 1%
	CAPACITOR			
	C1 - C2 - C3 - C8 - C10	837A241H03	5	0.27MFD.
	C4	876A409H09	1	1.0 MFD.
	C5	187A508H10	1	18 MFD.
	C11	3509A33H01		2.0MFD
	C7	837A241H16	1	2.2 MFD.
	C9	876A409H01	1	.18 MFD.
	DIODE			
	D1 TO D12	188A342H11	12	1N4822
	D13 - D14 - D15 - D18	188A342H06	4	1N4818
	D16 - D17	184A855H14	2	1N4385
	D19 - D21	837A692H03	2	1N645A
	D20	184A855H07	1	1N457A
	TRANSFORMER			
	T1 - T2 - T3	2908300G02	3	
	TRANSISTOR			
	Q11	837A617H03	1	2N3590
	Q1 - Q2 - Q3 - Q5 - Q7 - Q9	848A851H02	6	2N3417
	Q4	184A638H18	1	2N697
	Q6	184A638H20	1	2N1132
	Q8 - Q10	849A441H01	2	2N3645
	RESISTOR			
	R28	184A763H41		3.9K 1/2W ± 5%
	R1 - R2 - R3	184A763H62	3	30K - 1/2W - ± 5%
	R4 - R5 - R6 - R19	837A237H21	4	1200Ω - 11W - ± 5%
	R60 - R25 - R29 - R32	184A763H47	4	6.8K - 1/2W - ± 5%
	R10 - R11 - R12	629A531H67	3	30K - 1/2W - ± 2%
	R13 - R14 - R15 - R24 R30 - R31 - R34	184A763H51	7	10K - 1/2W - ± 5%
	R16 - R17 - R18 - R35	184A763H59	4	22K - 1/2W - ± 5%
	R20	184A763H61	1	27K - 1/2W - ± 5%
	R21 - R22	184A763H35	2	2.2K - 1/2W - ± 5%
	R23 - R36	184A763H43	2	4.7K - 1/2W - ± 5%
	R26 - R33 - R37	184A763H73	3	82K - 1/2W - ± 5%
	R27	184A763H53	1	12K - 1/2W - ± 5%
	R38	762A679H01	1	150Ω - 3W
	R46	629A430H01	1	50K - 1/4W - ± 20%
	R42 - R43 - R44	185A211H05	3	20,000Ω - ± 10%
	R45	862A406H02	1	20K - .5W - ± 10%
	R47	184A756H01	1	40K
	R48 - R51	185A067H05	2	250Ω
	R49 - R52 (125VDC)	1336173	2	560Ω - 40W - ± 5%
	R49 - R52 (48VDC)	04D1299H66	2	95Ω - 40W - ± 5%
	R53	184A763H67	1	47K - 1/2W - ± 5%
	ZENER DIODE			
	Z1 - Z2 - Z3	849A515H05	3	1N4751A
	Z4 - Z5 - Z6 - Z9	186A797H13	4	1N748A
	Z8	188A302H17	1	1N3021B
	Z10	862A288H01	1	1N3688A
	DZP	762A631H01	1	1N2984B
	DZP1 - DZP2	629A798H03	2	1N2986B
	Z7	188A302H18		1N3035B
	Z11	878A619H01	1	1.5KE200
	VARSISTOR			
	VR1 - VR2 - VR3	183A122H02	3	12K - ± 20%
	TELEPHONE RELAY			
	TR2 - TR3	407C614H06	2	
	TR1	407C280H19	1	
	RESISTOR			
	RDC (125VDC)	1267293	1	1.5K - 25W - ± 5%
	RDC (48VDC)	1202587	1	400Ω - 25W - ± 5%
	R50	184A756H02	1	100K
	R39 - R40 - R41	629A430H05	3	200K - 1/4W - ± 20%
	R7 - R8 - R9	629A531H60	3	15K - 1/2W - ± 2%
	R54	1202499	1	150Ω - 40W - ± 5%
	R55	04D1299H77	1	180Ω - 40W - ± 5%
	R56	848A821H13	1	49.9K 1/2W - ± 1%
	R57(48VDC)	1267283	1	600Ω 25W ± 5%
	R57(125VDC)	1208342	1	3550Ω 25W ± 5%
	R58	184A763H37	1	2.7K 1/2W ± 5%
	R59	184A763H13	1	270Ω 1/2W ± 5%

Sub 6
1327D68



(5a)

Sub 2
719B480



(5b)

Sub 2
719B481

Fig. 5. External Connections (1 Timer) (2 Timer).

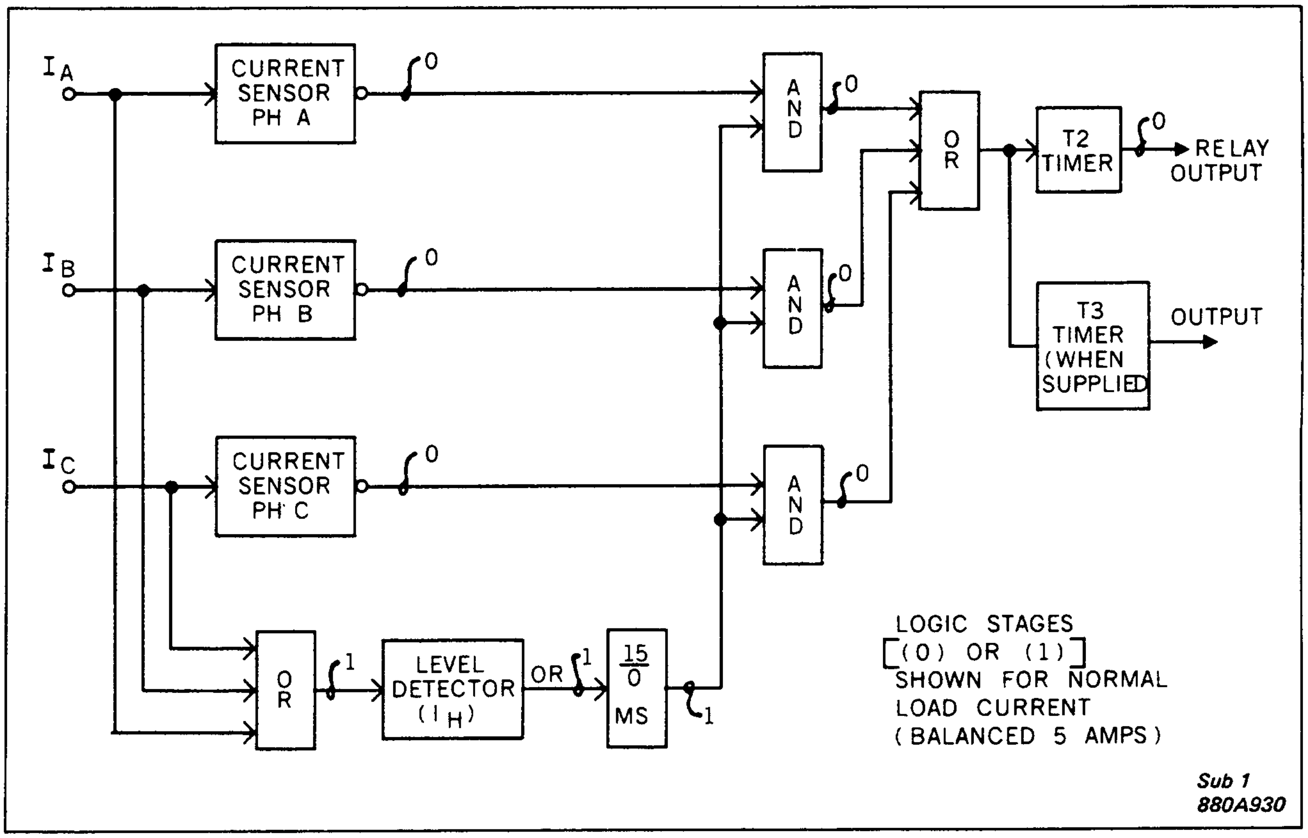


Fig. 6. Logic Block Diagram.

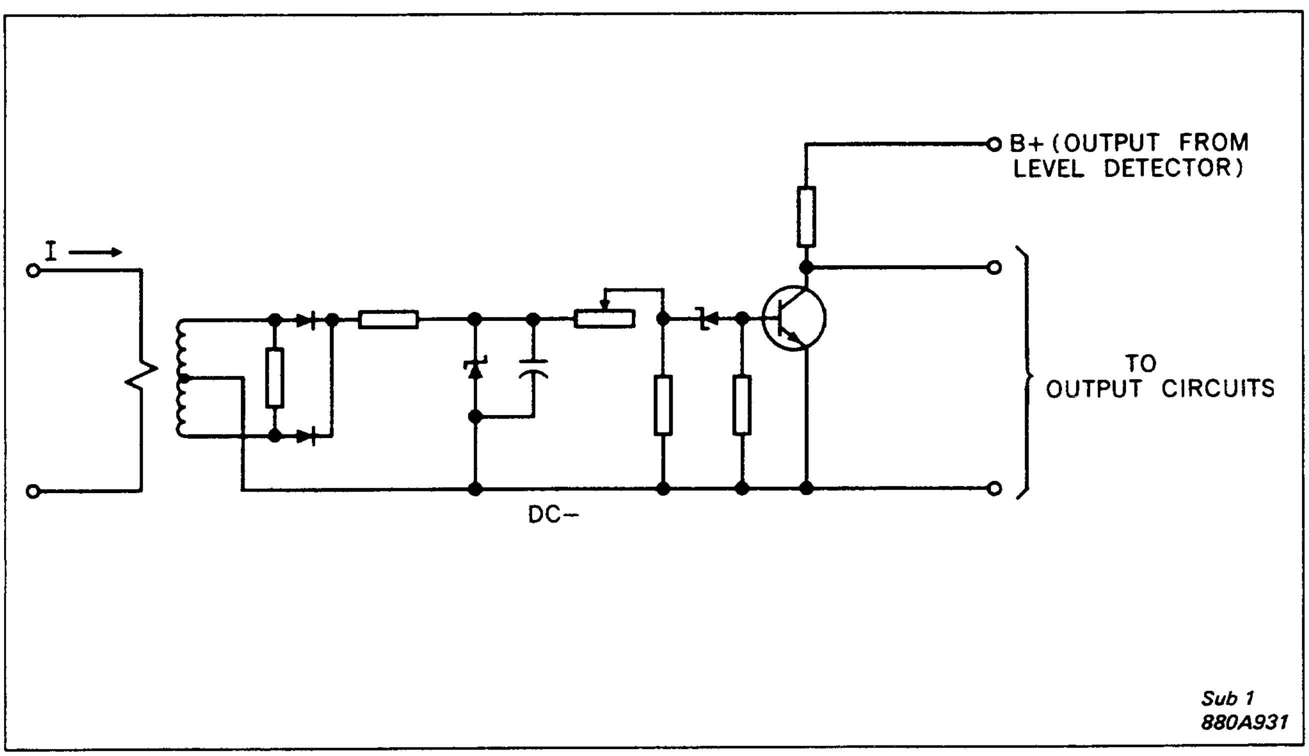


Fig. 7. Basic Current Sensor Circuit.

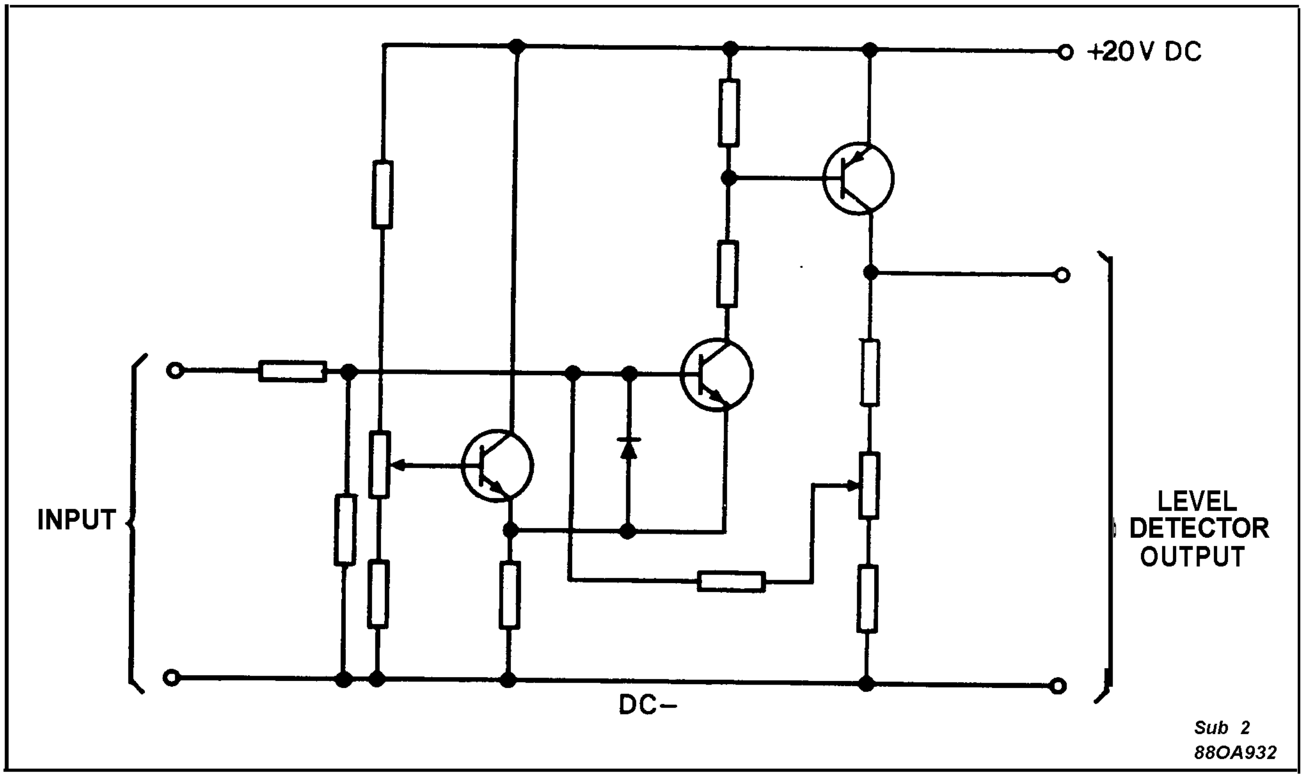


Fig. 8. Level Detector.

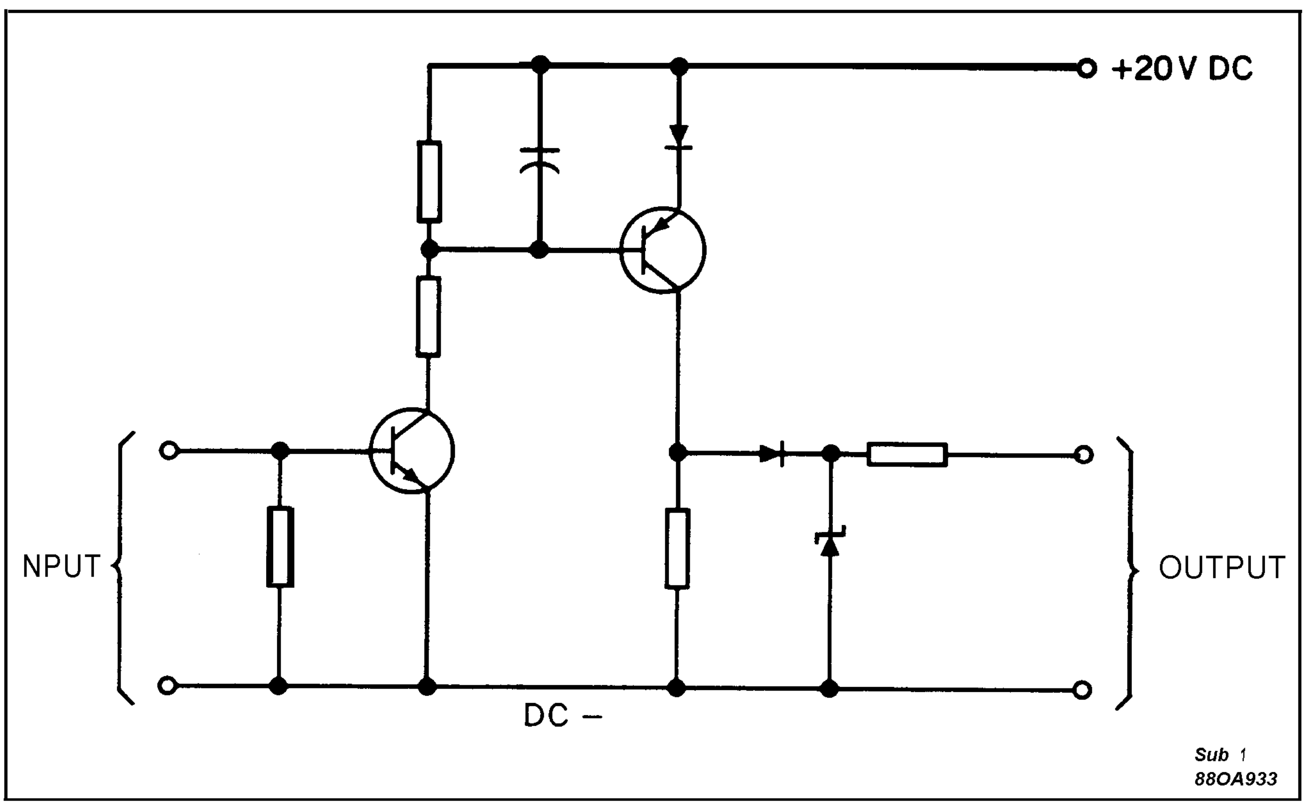


Fig. 9. Standard Output Circuit.

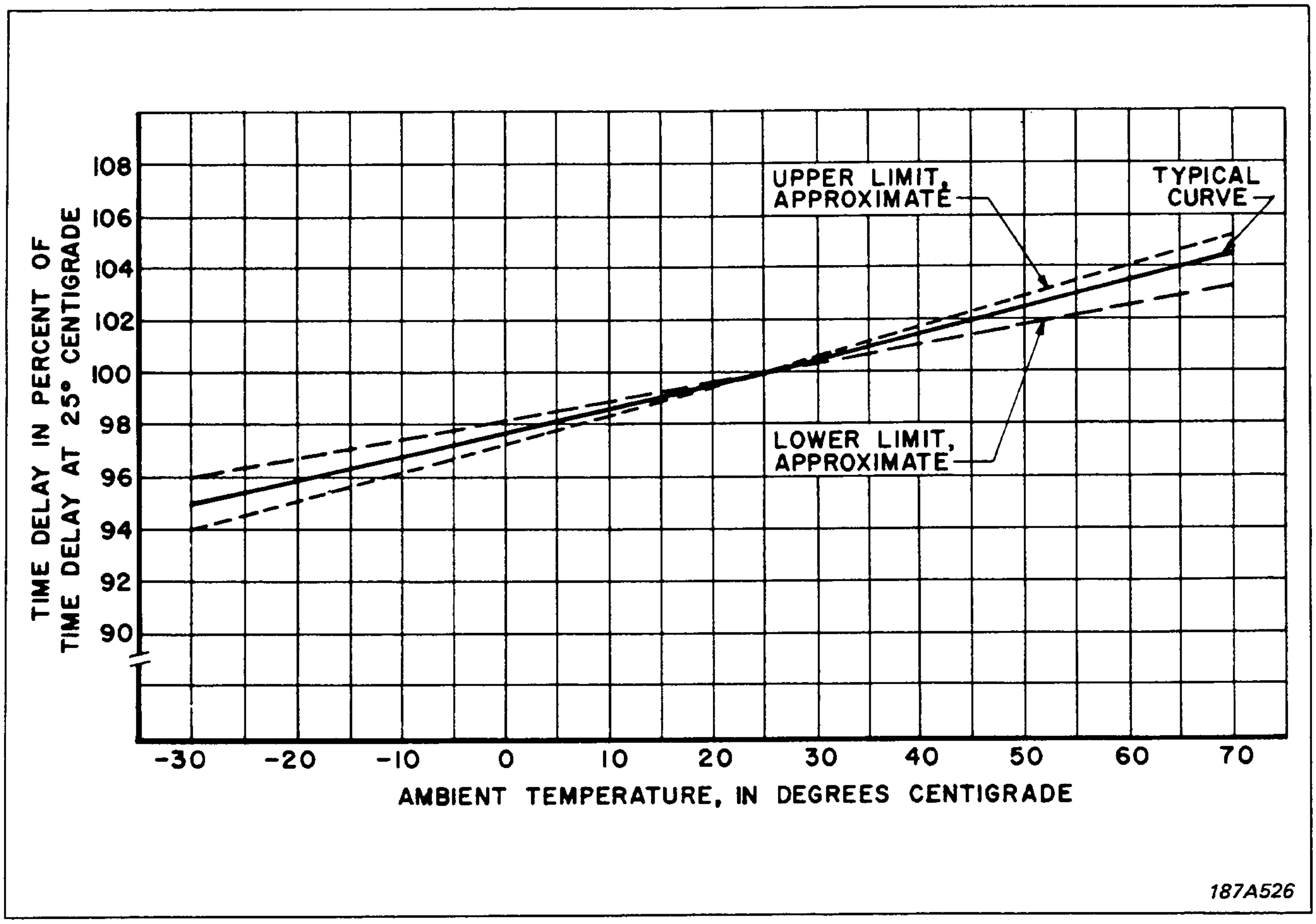


Fig. 10. Timing Variation with Temperature Changes.

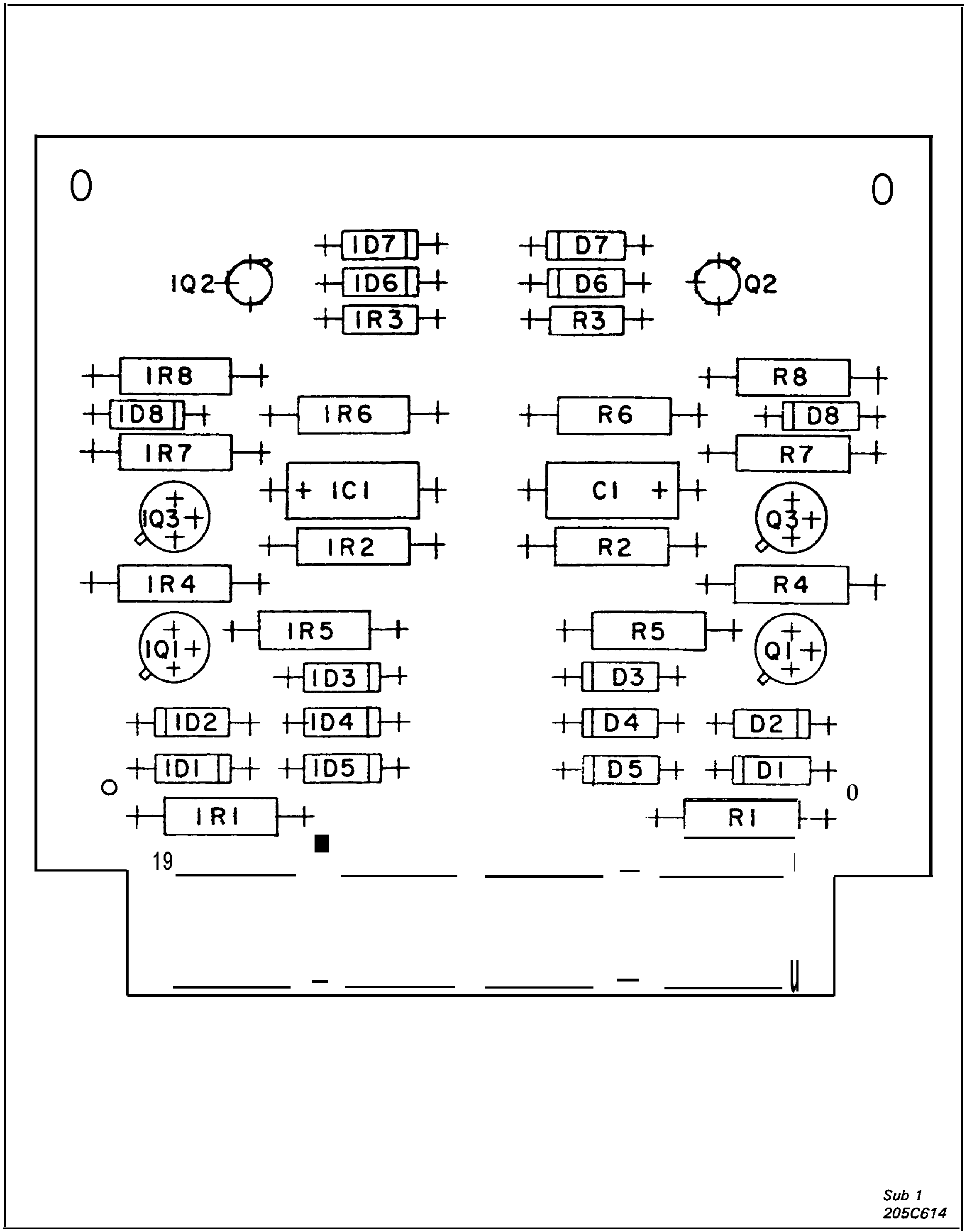
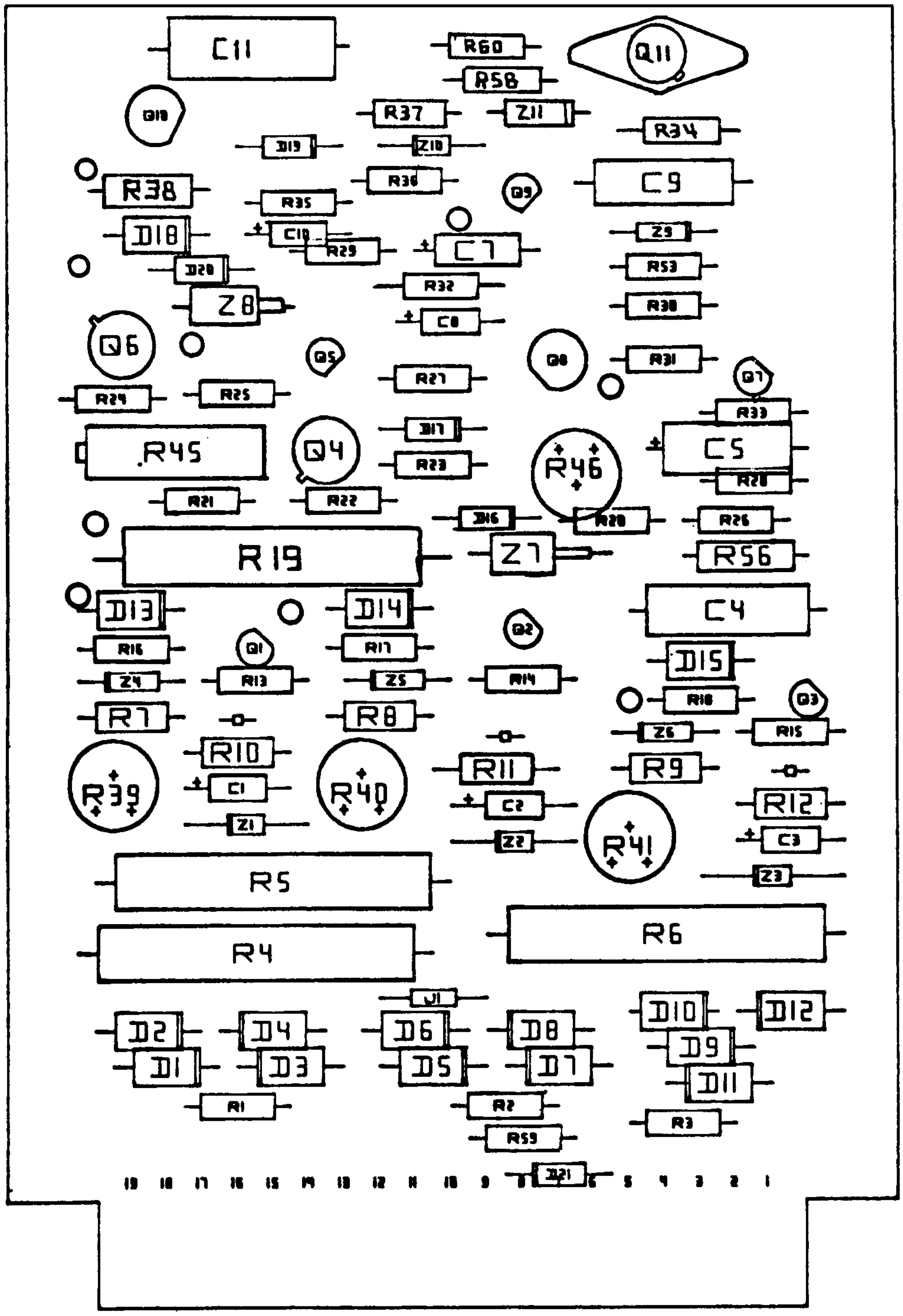
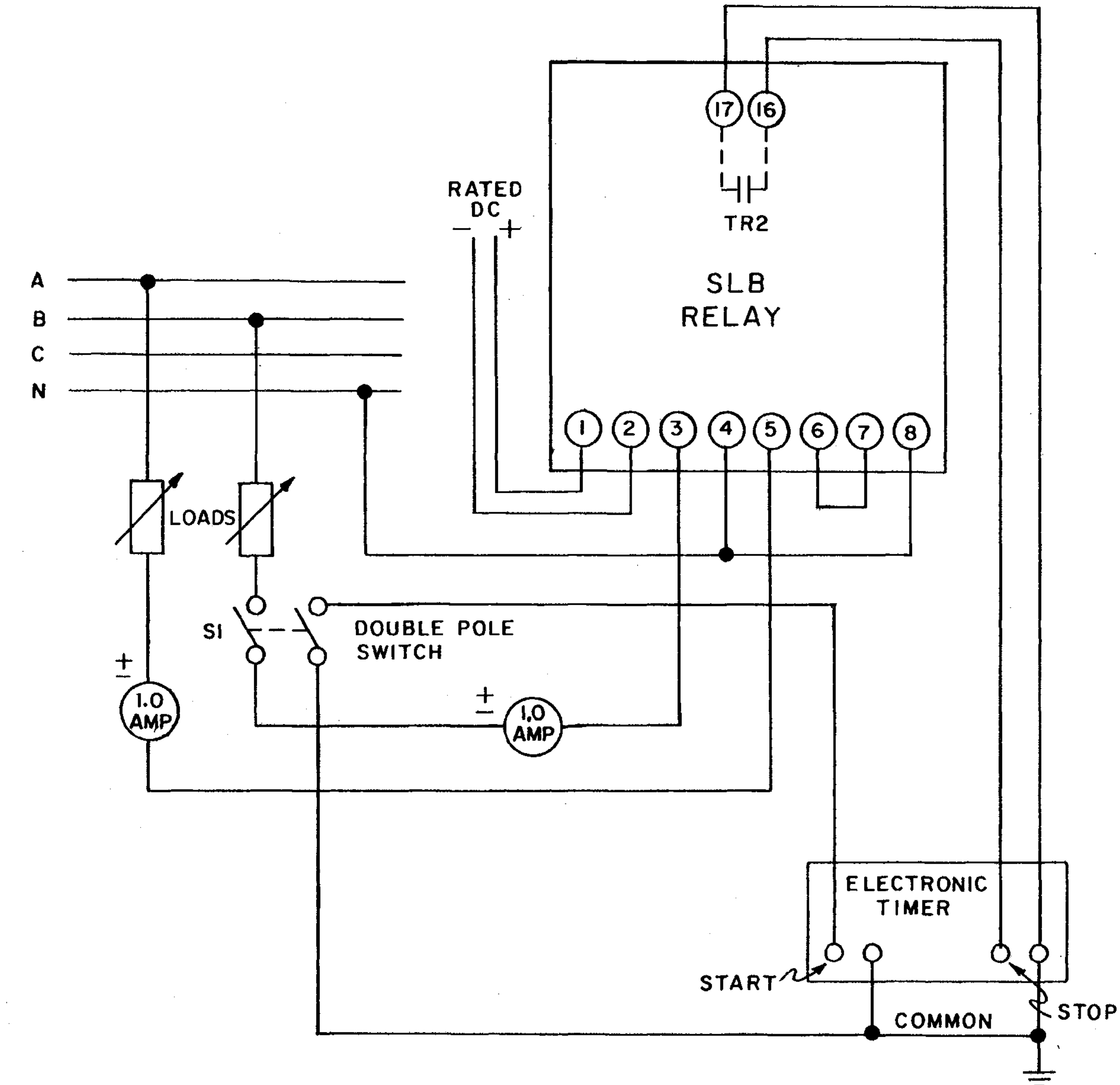


Fig. 11. Component Location (Timer Board).



Sub 1
3518A94

Fig. 12. Component Location (Logic Board).



NOTE:
ELECTRONIC TIMER STARTED BY OPENING SWITCH CONTACTS AND STOPPED BY CLOSING OF TR2 RELAY CONTACTS.

Sub 1
3521A51

Figure 13. Timer Test Circuit

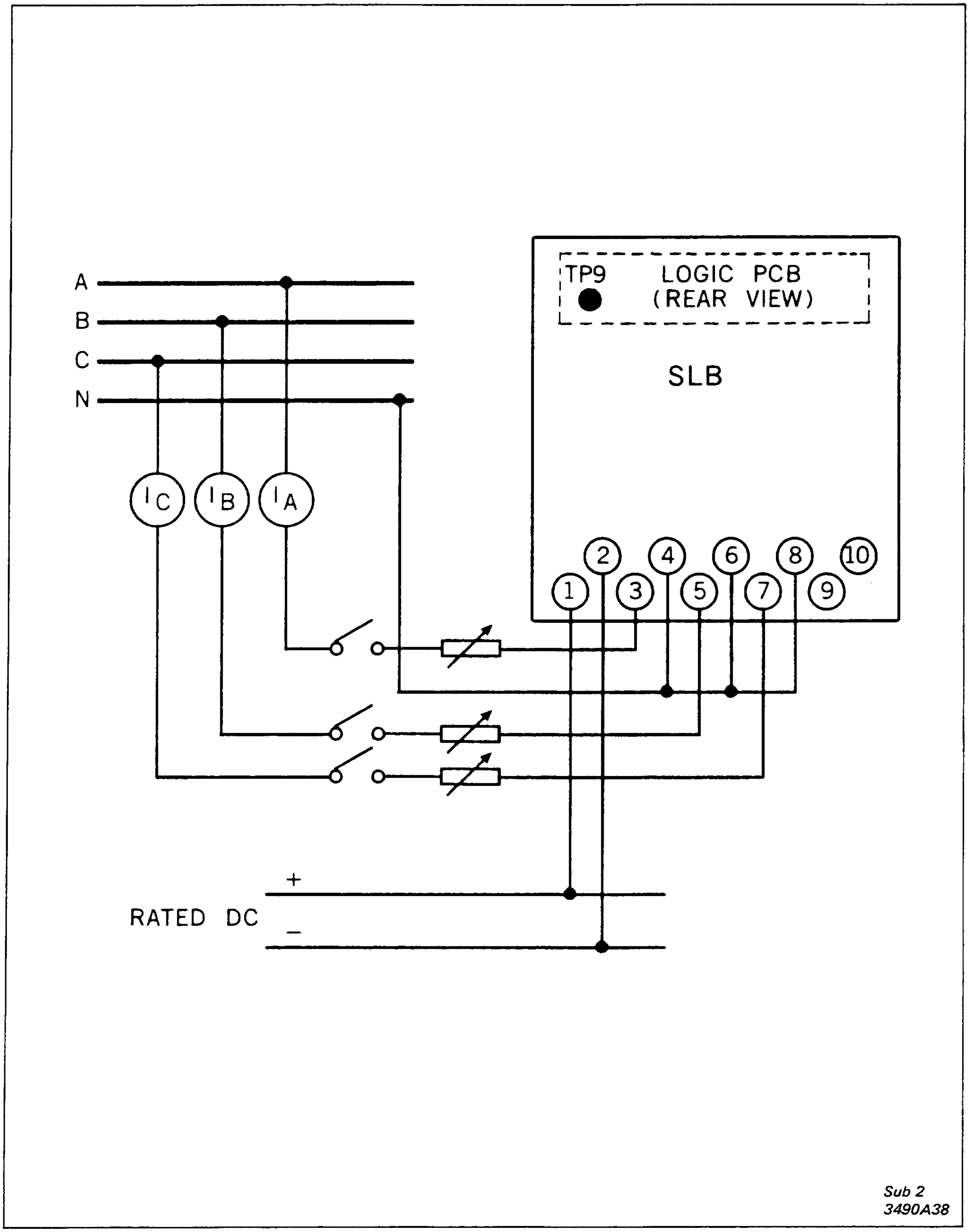


Fig. 14. Relay Test Circuit.

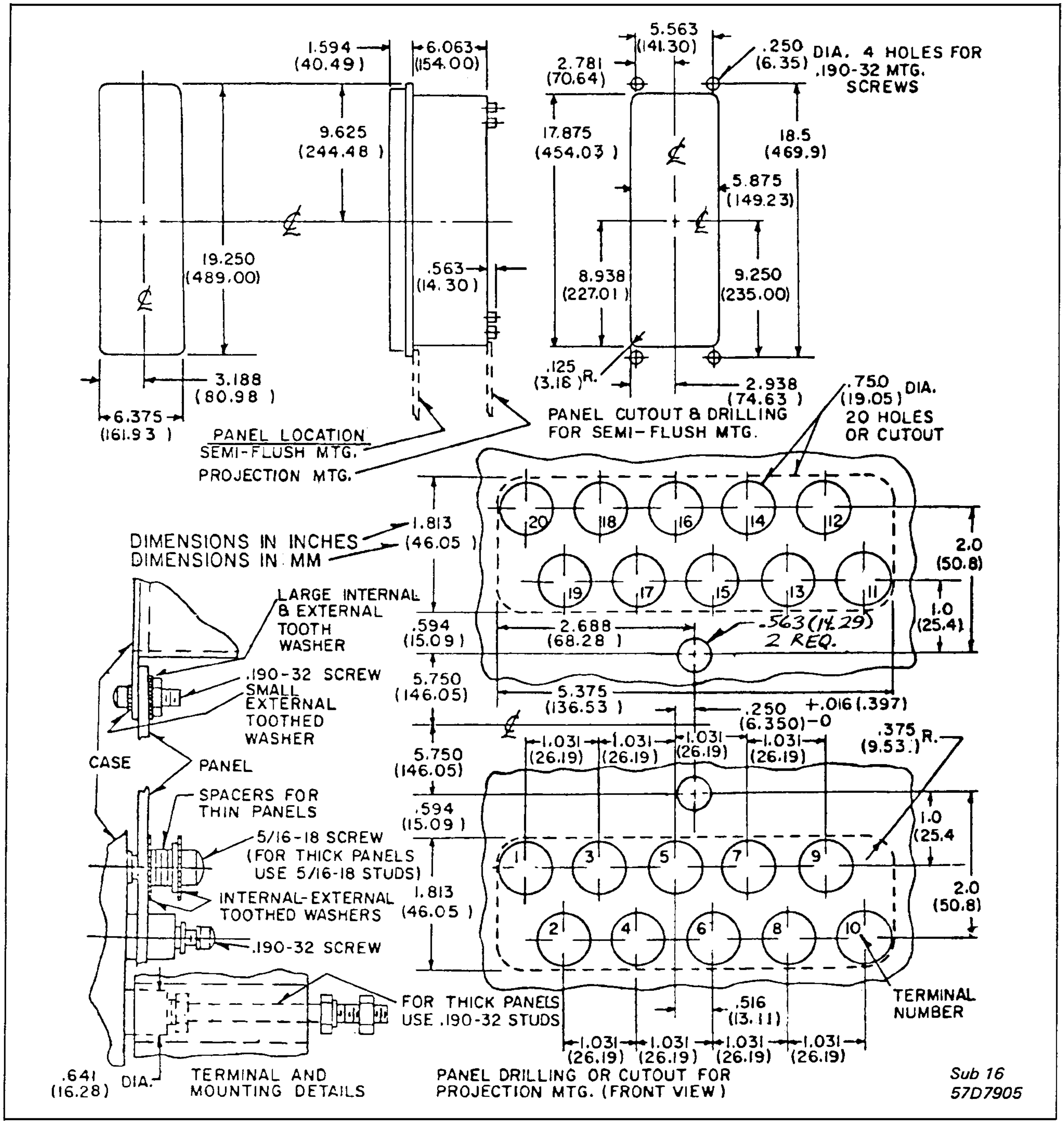


Fig. 15. Outline and Drilling Plan for Type SLB Relay in Type FT-42 Case.

ABB Inc.

4300 Coral Ridge Drive
Coral Springs, Florida 33065

Telephone: +1 954-752-6700
Fax: +1 954-345-5329

www.abb.com/substation automation