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1 SIMULATION LOGIC

Simulation logic is an optional function in all the REx 5xx series protection, control, and monitoring terminals.

1.1 Application

Simulation logic, as built optionally into the REx 5xx protection, control, and monitoring terminals, serves as a useful tool for protection and commissioning engineers during their work with the terminals, as well as for the personnel in control rooms and control centres in connection with the checking of information circuits and functions in a secondary power system.

It is of particular help when testing different parts of the disturbance report function, service values of different binary signals, binary outputs of the terminals, and remote serial communication.

The simulation logic will be active only when the terminal operates in “Test” mode, which is indicated by flashing of the yellow LED on the terminal man machine interface (MMI) unit.

When the simulation logic is active, only the logical signals connected to the logic can change their status. All other logical signals within the tested terminal will remain equal to logical zero, regardless of the configuration of the internal logical circuits.

Control of the simulation logic and setting of the corresponding parameters can be carried out locally by the built-in MMI unit, or a front connected personal computer, as well as remotely, when the option “remote communication” is installed in the terminal.

1.2 Design

The simulation consists of two functional parts, as shown in Fig. 1. They are the so-called “signal test” and “event test” parts.

The signal test part serves for the testing of different logical signals. The outputs of the unit, marked SIGn-SIGNAL (n goes from 1 to 6) will always follow the statuses of the input signals connected to the corresponding input terminals SIGn-INPUT, after the corresponding configuration has been initiated. These input terminals are freely programmable to the fixed signals FIXD-ON and FIXD-OFF, as well as to any of the binary input terminals of the unit.

The event test part serves for the testing of different sequential events. The output signals EVm--SIGNAL (m goes from 1 to 7) will follow the corresponding input signals EVm--INPUT according to the configuration and settings of the timers as shown in Fig. 1. The input terminals are freely programmable to the fixed signals FIXD-ON and FIXD-OFF, as well as to any of the binary input terminals of the unit.

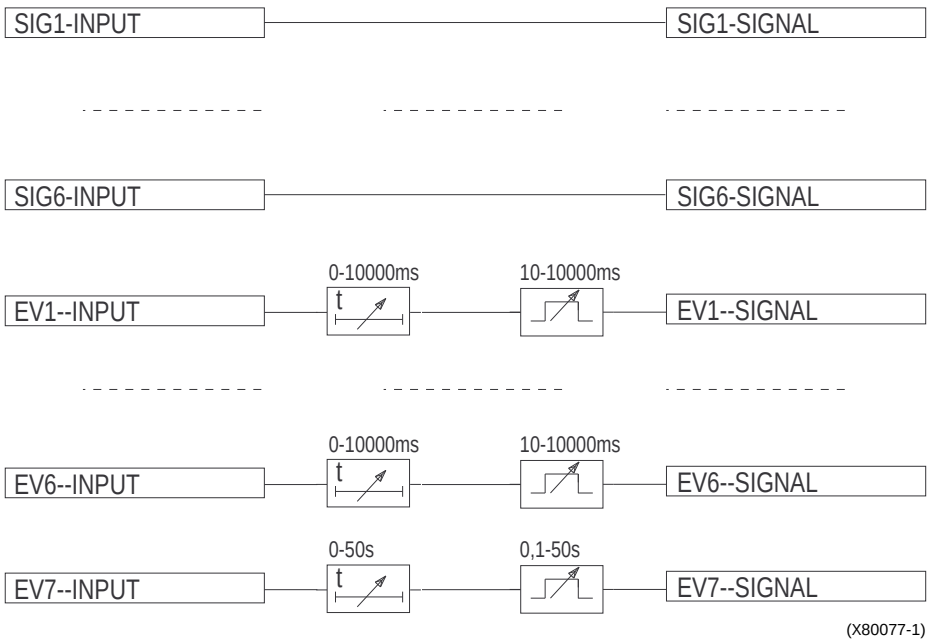

Fig. 1 Simulation logic - block diagram

1.3 Configuration and activation

A FIXD-OFF signal is connected as default to all inputs SIGn-INPUT and EVn--INPUT of the simulation logic.

All outputs SIGn-SIGNAL and EVn--SIGNAL are connected to the dummy signal SIML-NOSIGNAL.

All the unused output signals should always be connected to the SIML-NOSIGNAL. A logical signal can at the same time be connected to an only output signal of the simulation logic.

The user can configure and set different parameters of the configuration logic under the submenu:

Test
SimulationLog
Operation (Signal test, Event test)

1.3.1 Operation of the simulation logic

Menu tree:

Test
SimulationLog
Operation

The simulation logic can be put in operation only if the terminal is in test mode. An additional condition is that the terminal operating mode is changed to test mode by the setting and not by the activation of input signal TEST-INPUT.

1.3.2 Configuration and setting of the signal test logic

Menu tree:

Test
SimulationLog
Signal test
Signaln

Only the signals FIXD-ON, FIXD-OFF and IOx--BIyy (all of the binary inputs to the terminal) are configurable to the input terminals SIGn-INPUT of the simulation logic function.

The output terminals of the simulation logic function are configurable to all the internal logical signals and binary outputs IOx--BOyy, except the FIXD-ON and FIXD-OFF signals.

After the configuration has been initiated, the signal connected to the output terminals of the function will automatically follow up the status of the corresponding input signal.

1.3.3 Configuration and setting of the event test logic

Menu tree:

Test
SimulationLog
Event test
Eventn

Only the signals FIXD-ON, FIXD-OFF and IOx--BIyy (all binary inputs to the terminal) are configurable to the input terminals SIGn-INPUT of the simulation logic function.

The output terminals of the simulation logic function are configurable to all internal logical signals and binary outputs IOx--BOyy, except the FIXD-ON and FIXD-OFF signals.

The necessary time delays for each event tn (where n runs from 1 to 7) and pulse length tPulsen are settable under the same submenu in wide ranges. The event will always start when the signal connected to the corresponding input terminal EVn--INPUT assumes the logical value 1.

It is always necessary to deactivate the simulation logic after the test has been completed, to permit the operation of other functions while the terminal is still in test mode.

The simulation logic will automatically deactivate when the terminal switches from test to operation mode.

1.4 Testing

Each signal or event function should be tested separately. The best way of testing is to connect the input terminal of the function under test to one of the terminal binary inputs, and the corresponding output signal to one of the binary outputs.

The output signal must always follow the changes on the binary input, when connected to the signal test part. It must follow a typical logical scheme, including both timers in the same circuit, when connected to the event test circuits.

1.5 Appendix

1.5.1 Terminal diagrams

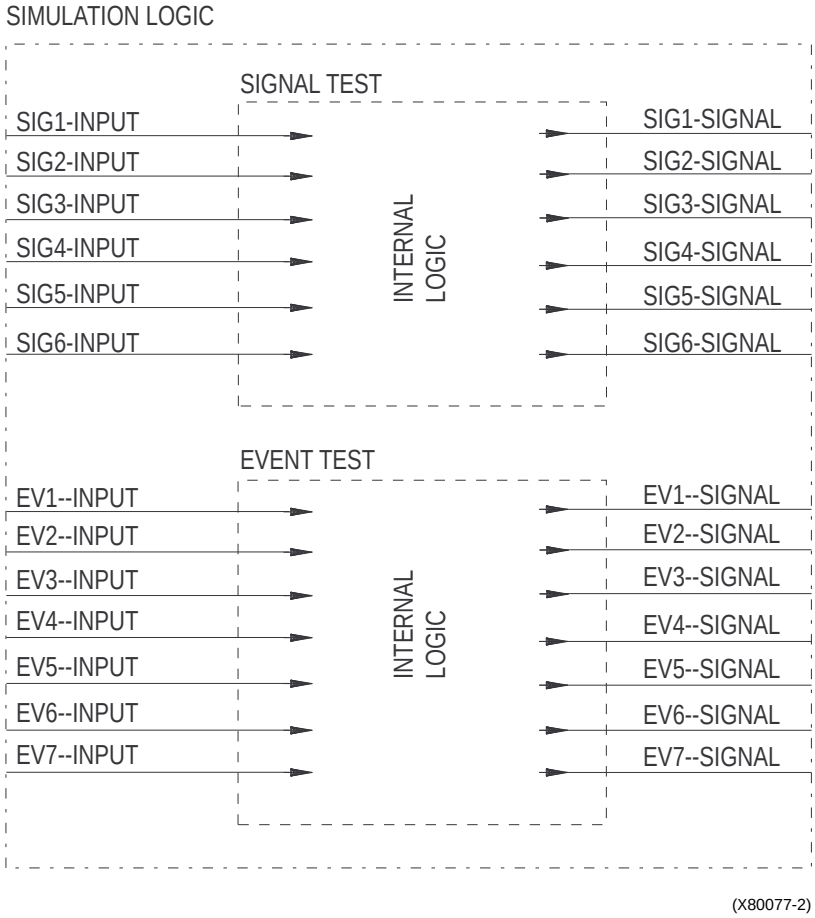

Fig. 2 Simplified terminal diagram of the function.

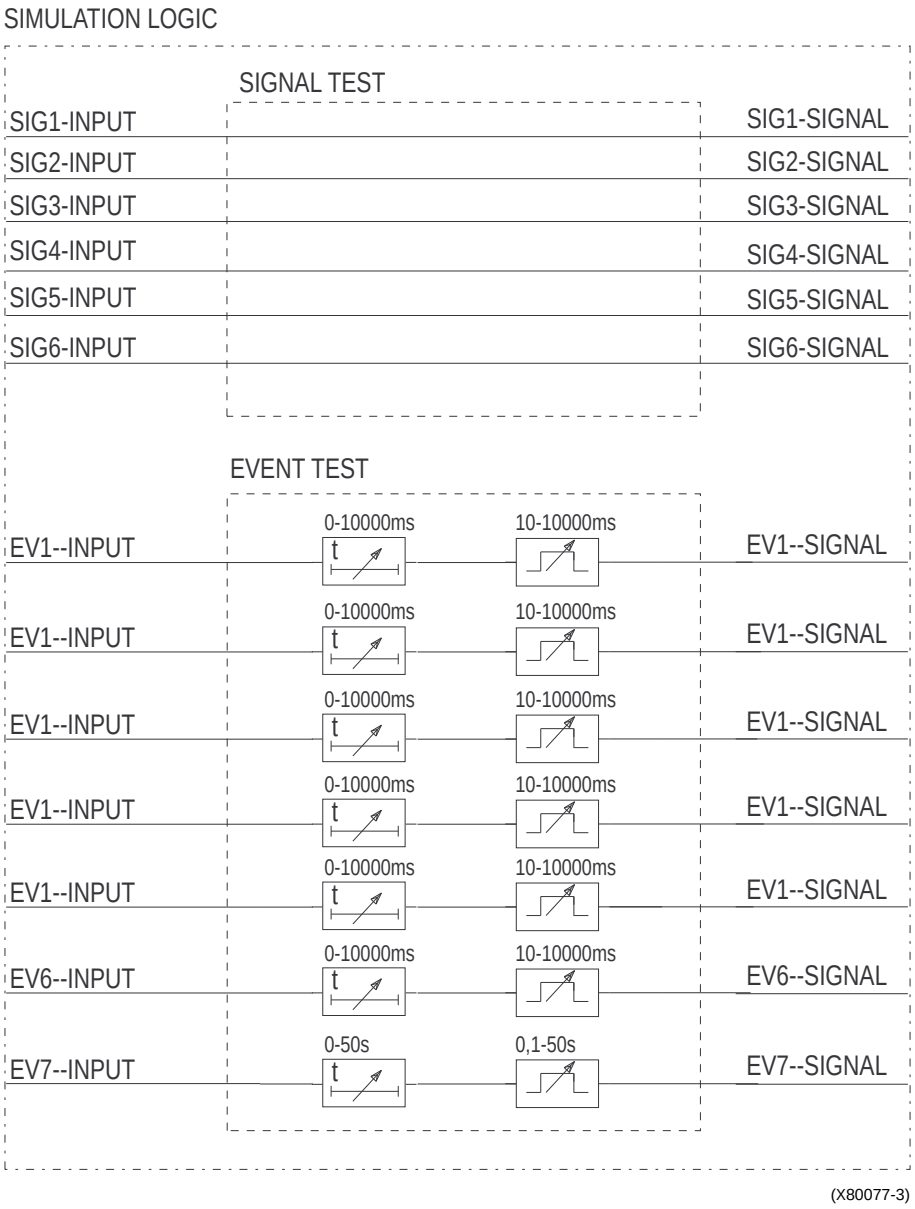

Fig. 3 Terminal diagram of the function.

1.5.2 Signal list

CONNECTIONS:	TO:	SETTING:	DESCRIPTION:
SIG1-INPUT	FIXD BI		Input No. 1 to the signal test part of the simulation logic
SIG2-INPUT	FIXD BI		Input No. 2 to the signal test part of the simulation logic
SIG3-INPUT	FIXD BI		Input No. 3 to the signal test part of the simulation logic
SIG4-INPUT	FIXD BI		Input No. 4 to the signal test part of the simulation logic
SIG5-INPUT	FIXD BI		Input No. 5 to the signal test part of the simulation logic
SIG6-INPUT	FIXD BI		Input No. 6 to the signal test part of the simulation logic
EV1--INPUT	FIXD BI		Input No. 1 to the event test part of the simulation logic
EV2--INPUT	FIXD BI		Input No. 2 to the event test part of the simulation logic
EV3--INPUT	FIXD BI		Input No. 3 to the event test part of the simulation logic
EV4--INPUT	FIXD BI		Input No. 4 to the event test part of the simulation logic
EV5--INPUT	FIXD BI		Input No. 5 to the event test part of the simulation logic
EV6--INPUT	FIXD BI		Input No. 6 to the event test part of the simulation logic
EV7--INPUT	FIXD BI		Input No. 7 to the event test part of the simulation logic

PRODUCTION:	TO:	SETTING:	DESCRIPTION:
SIG1-SIGNAL	BO		Output No. 1 from the signal test part of the simulation logic
SIG2-SIGNAL	BO		Output No. 2 from the signal test part of the simulation logic
SIG3-SIGNAL	BO		Output No. 3 from the signal test part of the simulation logic
SIG4-SIGNAL	BO		Output No. 4 from the signal test part of the simulation logic
SIG5-SIGNAL	BO		Output No. 5 from the signal test part of the simulation logic
SIG6-SIGNAL	BO		Output No. 6 from the signal test part of the simulation logic
EV1--SIGNAL	BO		Output No. 1 from the event test part of the simulation logic
EV2--SIGNAL	BO		Output No. 2 from the event test part of the simulation logic
EV3--SIGNAL	BO		Output No. 3 from the event test part of the simulation logic
EV4--SIGNAL	BO		Output No. 4 from the event test part of the simulation logic
EV5--SIGNAL	BO		Output No. 5 from the event test part of the simulation logic
EV6--SIGNAL	BO		Output No. 6 from the event test part of the simulation logic
EV7--SIGNAL	BO		Output No. 7 from the event test part of the simulation logic

1.5.3 Setting table

PARAMETER:	SETTING RANGE:	SETTING	DESCRIPTION:
		ACTUAL	
Operation	On / Off		Operation of the simulation logic set On or Off. Logic can be active only when terminal in the TEST mode.
t1	(0 - 10000) ms		Time delay set on the input timer No. 1 of the event test part of the simulation logic
tPulse1	(10-10000) ms		Pulse length set on the pulse timer No. 1 of the event test part of the simulation logic
t2	(0 - 10000) ms		Time delay set on the input timer No. 2 of the event test part of the simulation logic
tPulse2	(10-10000) ms		Pulse length set on the pulse timer No. 2 of the event test part of the simulation logic
t3	(0 - 10000) ms		Time delay set on the input timer No. 3 of the event test part of the simulation logic
tPulse3	(10-10000) ms		Pulse length set on the pulse timer No. 3 of the event test part of the simulation logic
t4	(0 - 10000) ms		Time delay set on the input timer No. 4 of the event test part of the simulation logic
tPulse4	(10-10000) ms		Pulse length set on the pulse timer No. 4 of the event test part of the simulation logic
t5	(0 - 10000) ms		Time delay set on the input timer No. 5 of the event test part of the simulation logic
tPulse5	(10-10000) ms		Pulse length set on the pulse timer No. 5 of the event test part of the simulation logic
t6	(0 - 10000) ms		Time delay set on the input timer No. 6 of the event test part of the simulation logic
tPulse6	(10-10000) ms		Pulse length set on the pulse timer No. 6 of the event test part of the simulation logic
t7	(0 - 50) s		Time delay set on the input timer No. 7 of the event test part of the simulation logic
tPulse7	(0,1-50) s		Pulse length set on the pulse timer No. 7 of the event test part of the simulation logic