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On Superior Power Cycling capability of a High Power Density SiC Power Module for e-Mobility Application

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The Power Point Presentation will be available after the conference.

Abstract

In this paper, the power cycling (PC) capability of RoadPak half-bridge SiC power modules is presented and the reliability fulfilment of the RoadPak power module for challenging e-Mobility mission profiles is assessed. The outstanding power cycling outcome has consolidated the competitiveness of the SiC-based RoadPak module backboned by the advanced packaging solutions. The failure mode analysis after PC_{min} and PC_{sec} shed light how advanced packaging system of RoadPak enables the full extraction of the power of SiC devices at elevated junction temperatures. Predicted RoadPak lifetime model is proposed with prudence yet fully sufficing harsh requirement. Furthermore, the challenges related to PC testing of SiC-based modules are discussed.

1 Introduction

Power semiconductor modules are the key components in the e-Mobility systems for various applications e.g., in traction inverter to drive electrical machine, on-board battery charger and DC/DC converter to support auxiliary systems or fast charging stations. Considering different applications such as eBuses, eTrucks or passenger cars, highly dynamic and harsh mission profiles for power module are expected [1]. Therefore, power modules with high power cycling capability are required to fulfill the lifetime requirement. To achieve the aggressive targets of electric-drive vehicles mass-market penetration, advanced power electronic technology with increased power density and efficiency is required [2].

A major advancement in power electronics towards higher power density and lower losses is recently achieved by using SiC-based devices. Reduced on-state resistance, minimized switching losses serve as the main technical advantage of SiC-based devices [3]. However, the SiC-based device can only make inroads with improved power electronics packaging technology which maximizes SiC benefit but not compromises its reliability [4]. Such a trend pushed the power electronics packaging to enable the higher current capability and to sustain extreme temperatures and stresses [5]. Therefore, higher reliability joining techniques must be developed. The lifetime limiting factors in conventional module packaging using e.g., aluminium wire bonding for the chip topside connection and soft soldering for chip-to-substrate connection are well known [6]. With the inherited size reduction of SiC chips, such technologies post even more limited suitability for SiC-based device application. Therefore, several investigations on different novel technologies have been conducted and discussed in the last decades. However, the reliability and robustness of the power module with promising technologies on a product level has seldom been demonstrated. In this paper, the power cycling lifetime capability of RoadPak module incorporating cutting-edge packaging technologies, is presented.

2 Automotive power cycling requirements

High reliability (power and thermal cycling, humidity resistance), low failure-in-time (FIT) rate, low losses and high efficiency to increase battery-powered range are among top requirements for power modules in e-Mobility applications. Hereby, the power cycling test serves as the basis of the power module lifetime model and therefore is one of the most determinative reliability tests for addressing power module durability in the

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operational stress situation. The main test variants are the on/off time of the load current (t_{on}/t_{off}), temperature swings (ΔT_j) and maximum junction temperature ($T_{j,max}$). Different from traction mission profiles, the e-Mobility mission profiles typically present highly diverse thermal cycles. As an example, cycling behavior analysis based on a typical e-Mobility mission profile shown in Fig. 1 presents mixed thermal cycles in a daily application profile. Both $T_{j,max}$ and cycle time (t_{cycle}) demonstrate wide distributions over ΔT_j. Besides the usual attention on high ΔT_j, more cycles are fallen into the low ΔT_j region as well as short cycle time as demonstrated by the color bar, emphasizing the importance of the robustness and reliability of power modules also on short loads. Therefore, careful selection of power cycling test parameter is of importance so that the consequent lifetime model better suits the lifetime calculation and is representative for the full range.

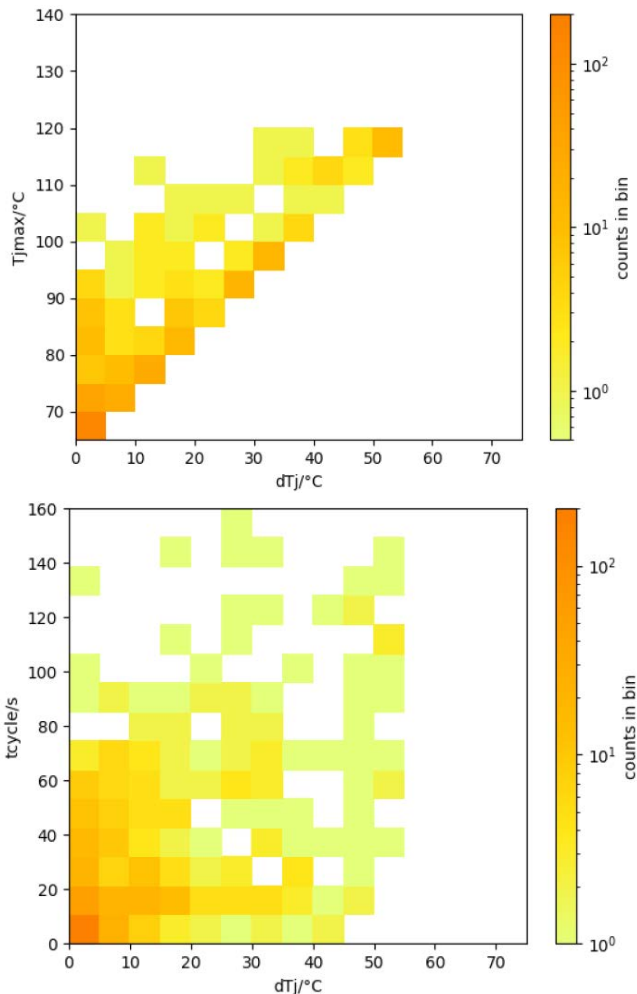

Fig. 1 Cycling analysis of a typical harsh e-Mobility mission profile.

In this paper, the power cycling test follows the AQG324 [7] requirement and methodology, where the power cycling tests are categorized in two types: PC_{sec} and PC_{min}. The PC_{sec} limits the t_{on} to smaller than 5 s and the PC_{min} limits the t_{on} to larger than 15 s. The PC failure criteria are defined as either thermal resistance (R_{th}) increase of 20% or MOSFET drain-source voltage (V_{DS}) / reverse MOSFET source-drain voltage (V_{SD}) increase of 5%.

3 Power cycling test on RoadPak module

3.1 Device-under-Test (DUT)

RoadPak half bridge SiC MOSFET modules (Fig. 2) with the latest packaging technology aiming at best performance with highest reliability are used in the power cycling test. Pressure silver sintering has been implemented for chip-substrate connection. Also, to enable the heavy copper wire bonding technology for chip top-side connection, sintered copper plate covering the chip source pads are implemented.

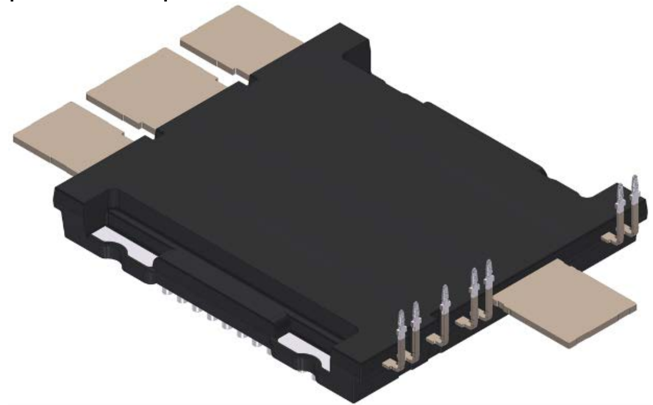

Fig. 2 RoadPak power module.

3.2 Testing execution

During the PC testing, both topological switches of each half-bridge modules were stressed with identical and constant current for each test type. The current flowed from source to drain through reverse MOSFET channel. The desired ΔT_j was reached by adapting gate-source voltage respectively, then gate-source voltage was kept unchanged for each switch. The virtual junction temperature was determined from indirect measurement via forward voltage drop of the SiC MOSFET body diode with small sensing current at sufficiently negative gate bias. The temperature-voltage dependency was measured for each topological switch via temperature-voltage

calibration of the body diodes with the same conditions as in the PC test.
The PC test conditions and respective results of PC_{sec} and PC_{min} on RoadPak according to the AQG 324 requirement are summarized in Table. 1.

Test type	t_{on}/t_{off} / s	ΔT_j / K	$T_{j,max}$ / °C	Avg. kcyc	End-of-Life (EoL) criteria
PC_{sec}	1.4/1.4	90	160	> 4,000	N/A
PC_{sec}	1.4/1.4	105	175	848	V_{SD} increase
PC_{min}	30/30	115	160	145	V_{SD} increase
PC_{min}	30/30	130	160	62	V_{SD} increase

Table. 1 PC_{sec} and PC_{min} test conditions and results summary.

For PC_{sec} at ΔT_j =90 K, the test has achieved superior cycling results as more than four million cycles without failure. Both V_{SD} and R_{th} did not indicate degradation before this number of cycles. For PC_{sec} at ΔT_j =105 K, the online V_{SD} has shown gradual increase and further developed to reach the EoL as 5%. R_{th} measurement result was stable without sign of degradation.
The result analysis on especially PC_{min} signified that a low increase of R_{th} (<10%) can already cause a high increase (>5%) in V_{SD} when it is monitored at hot condition (end of t_{on}). This is particularly relevant for SiC-based devices due to their strong dependency of $R_{DS,on}$ and temperature as shown in Fig. 3, where the PC testing temperature range falls into the positive-temperature-coefficient domain of the on-state voltage. Therefore, along the test when the junction temperature rises thanks to R_{th} degradation, the on-state voltage increases accordingly. Enhanced power loss caused by the on-state increase further aggregates junction temperature. This intrinsic superimposition together with the tight failure criterium of on-state voltage increase (5%) compared to R_{th} increase (20%) can therefore conceal R_{th}-related failure and exaggerate on-state degradation, when the on-state voltage is determined at hot condition. Such failure criteria are well accepted and applied in Si-based device PC testing, however proved to be unreliable if the same criterium is kept, based on the addressed SiC-based device characteristic.

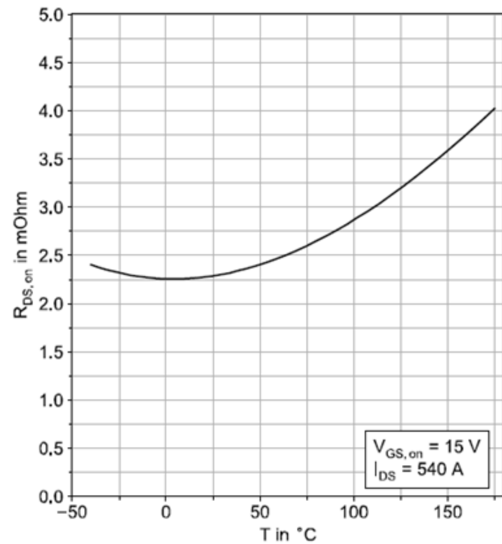

Fig. 3 Typical on-state resistance vs. temperature.

For this reason, more realistic lifetime and failure mode understanding can be achieved when the on-state measurement condition is clear and determined. Several methodologies have been proposed, such as measuring V_{DS} (or V_{SD}) at the beginning of the heating phase (first milliseconds of t_{on}) as cold measurement, or implementation of additional measurement cycles [8][9]. These methods require dedicated test set-up which limited its applicability.
In RoadPak PC_{min} testing, the V_{SD} failure criteria of online monitoring at end of t_{on} was lifted at 10% increase and DUTs were taken to conduct post cold measurement. The R_{th} failure criteria was kept the same 20% increase. Such empirical testing method was employed to keep the test set-up in minimum disturbance whereas taking the cold measurement for decisive judgement of failure.

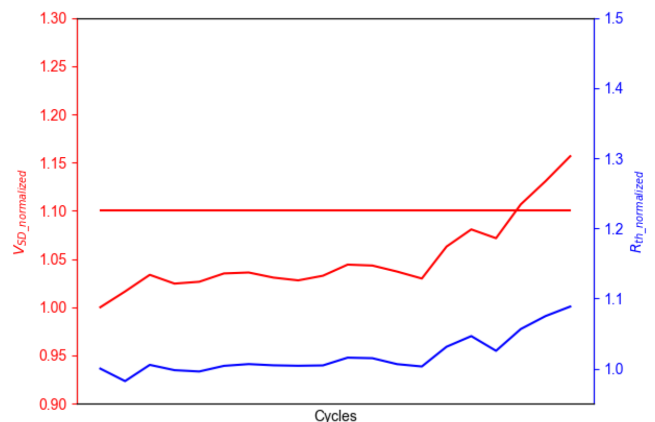

Fig. 4 Exemplary online monitoring of V_{SD}/R_{th} of RoadPak PC_{min} test, indicating the impact of R_{th} on hot V_{SD} measurement.

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A typical trend of V_{SD} in red line and R_{th} in blue line as shown in Fig. 4 revealed gradual degradation in the later cycles. The similarity of the increase trends along the cycles indicated the superimposition of R_{th} on V_{SD}. However, the gradual development of V_{SD} at the last cycles surpassed that of R_{th} and thereby resulted in V_{SD} failure. R_{th} increase was roughly 5% when V_{SD} reached 10% increase during monitoring as the defined failure criteria.
The 10% V_{SD} increase as failure criteria was considered as conservative selection, as confirmed from the post cold measurement that some DUTs did not reach 5% on-state increase. However, failure analysis including 100% optical microscopy and scanning acoustic microscopy (SAM) confirmed the same failure mode/degradation of the DUTs of the same test type. Therefore, those lifetime datapoints were taken as valid and used for the later proposed lifetime modeling with these initial results.

4 Failure analysis

Light microscopy inspection after epoxy mold removal and scanning electron microscopy (SEM) inspection were conducted to understand the failure root cause of PC tests. Unlike traditional power module packages with aluminium wire bonding, the implemented copper wire bonding itself was intact without lift-off from the copper plate or cracks. As shown in Fig. 5, visible cracks in copper top plate propagating from copper bond foot position can be seen, indicating a general topside degradation starting from the sintered copper top plate system.

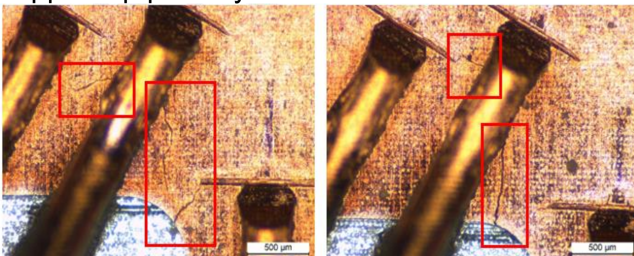

Fig. 5 Cracks of copper top plate after failure in PC_{sec}.

Moreover, the cross section performed right after confirmed the crack propagation into the top plate sinter layer but then it stopped at the first chip metallization layer, as shown in Fig. 6. It can be clearly seen in the top figure that the chip aluminium metallization has undergone severe degradation not only shown by the void in the chip top aluminium layer but also strong reconstruction, which is a well-known failure mechanism in the insulated-gate bipolar transistor (IGBT) module packaging [6]. In the presented RoadPak platform, the traditional aluminium wire bonding is replaced by harder copper wire bonding, which successfully eliminated the aluminium wire degradation and lift-off. However the soft chip aluminium alloy metalization is within the system and consequently left as the weakest point during the thermal cycles. The substrate-baseplate solder has also been inspected and confirmed as healthy via SAM analysis, conforming with the stable online R_{th} monitoring for all the DUTs under PC_{sec}.

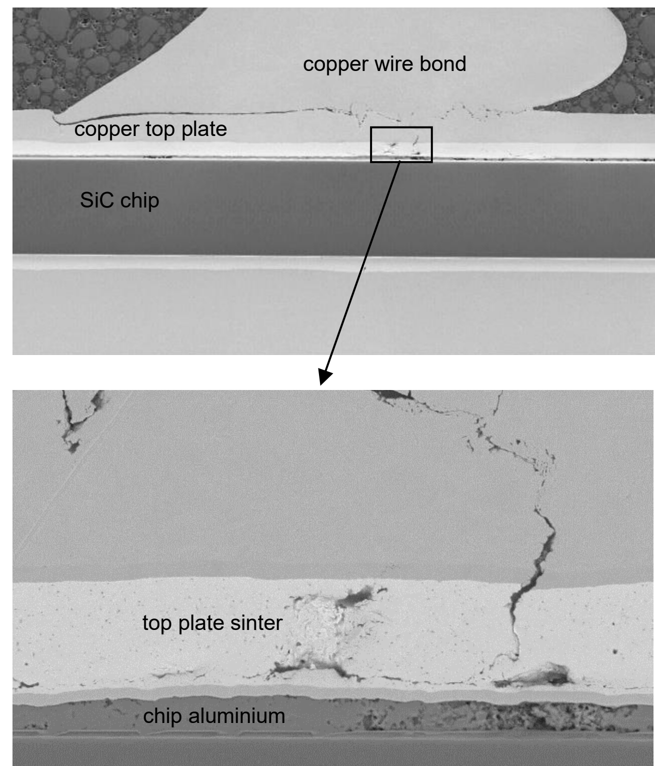

Fig. 6 Cross section after PC_{sec} showing crack propagation and chip aluminium thickness change (reconstruction).

Further cross-section analysis after PC_{min} in Fig. 7 elucidated that the failure root cause is mostly chip-near degradation including the packaging as well as the chip itself. Cracks in the top plate sinter layer and the chip-substrate sinter layer were identified in the cross section and highlighted by the black arrow in Fig. 7 a). Both cracks started from the sinter layer edges and occurred at interfaces with SiC chip. Chip aluminium degradation was also revealed as shown in Fig. 7 b). However, the R_{th} increase shown in the monitoring cannot be explained by the chip-near degradation. SAM analysis at the level of substrate-baseplate solder showed certain suspicious contrast indicating solder degradation from the edge. Further cross-section in the

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corresponding edges confirmed the solder degradation under the chip, as shown in Fig. 8. The crack occurred close to the interface between the substrate copper and the solder layer. Furthermore, voids are also observed within the solder layer. The solder degradation deteriorated the thermal path and thus increased the R_{th}, which is reflected on the online monitoring curve as shown in Fig. 4.

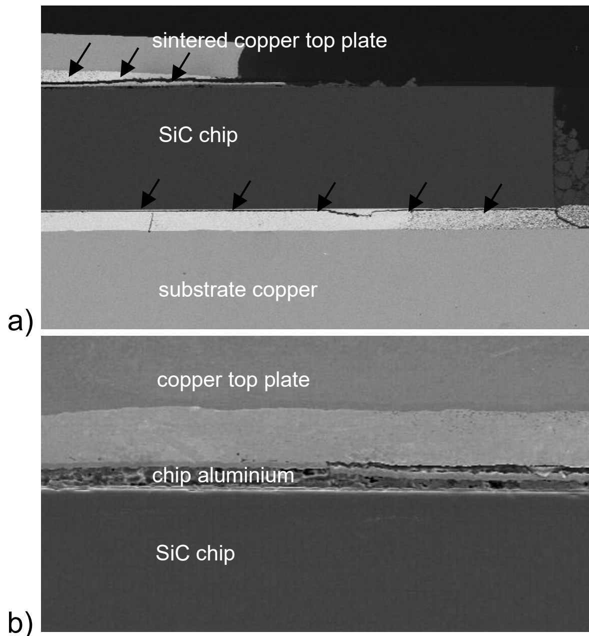

Fig. 7 Cross section after PC_{min}: a) chip top side and bottom side sinter layer delamination; b) chip aluminium degradation.

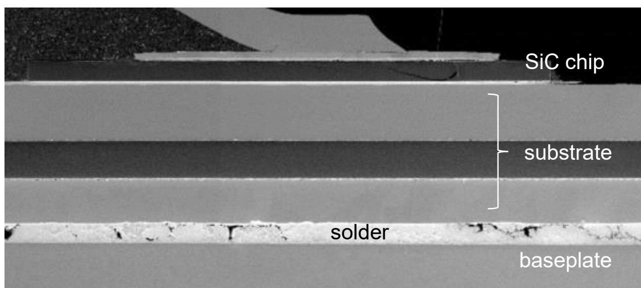

Fig. 8 Cross section after PC_{min} focusing on substrate-baseplate solder.

5 Lifetime modeling

Based on the PC test results, a first lifetime model for RoadPak was established. Conservative data collection strategy was employed to provide fair module reliablility characteristics serving for trustworthy yet conservative operation lifetime prediction based on diverse mission profiles. PC_{sec} cycle numbers of unfailed DUTs and aggressive judgement on on-state increase pass/fail criteria resulting in conservative cycle numbers for PC_{min} were used. As the degradation patterns of failed DUTs of PC_{sec} and PC_{min} prevailed distinctive characteristics, the lifetime models are created respectively.

5.1 PC_{sec} lifetime model

From the failure analysis, the failure occurred in the chip-near connection, where the materials are less prone to influenced by the creep effects than the chip-remote interconnection such as substrate-baseplate solder. Therefore, certain simplications on the first lifetime model can be possible thanks to negligible impacts of absolute-temperature as well as stress duration. Therefore, a fatigue lifetime model based on the Coffin-Manson approach emphasizing on ΔT_j dependency to portray the module capability is considered reasonable and empirical:

$$N_{f,PCsec} = A \cdot \Delta T_j^{\alpha} = 2 \cdot 10^{25} \cdot \Delta T_j^{-9.58} \quad (1)$$

The derived PC_{sec} lifetime model together with the test datapoints summarized in Table. 1 are plotted as the solid line and points in Fig. 9. The plot also included published lifetime models under comparable test conditions to confirm the benefit of advanced module packaging technologies.

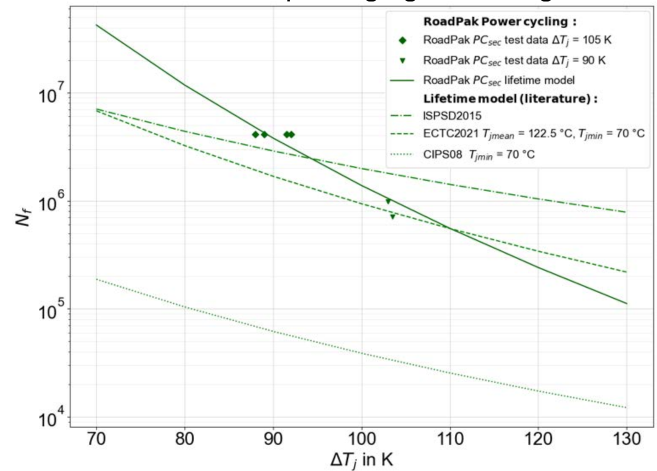

Fig. 9 RoadPak PC_{sec} lifetime modeling and comparison with relevant lifetime models in literature [10][11][12].

The classic CIPS08 model was generated under extensive statistical analysis enveloping various traditional module packaging technologies such as aluminium wire-bonding and solder as chip-substrate connection [10]. The lifetime model denoted as ISPSD2015 referred to the evolved version based on CIPS08 model to describe Si-IGBT baseplate-free modules employing more advanced packaging technologies such as copper wire-bonding, silver sintering or diffusion soldering

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as chip-substrate connection [11]. The model denoted as ECTC2021 essaied to depict lifetime of one-chip Si-IGBT modules with silver-sintered copper plates for copper wire-bonding, and silver sintering was selected for its chip-substrate connection [12]. Comparing among the four lifetime models, the lifetimes of the three on top of the plot with advanced packaging technologies including the copper wire-bonding and silver sintering as chip-substrate connection, are fostered more than an order of magnitude than the lifetime from conventional packaging technologies. To be noted, RoadPak among them, which is the only SiC-based full module, manifests reliability benefits especially at short loads and low ΔT_j, where most cycling occurrence is according to the analysis on the mission profile and thermal cycles exemplified in Fig. 1. Taking the predominant failure root cause of chip aluminium degradation into consideration, the robustness of RoadPak packaging is fully proved. Another remark can be made on sintered copper plate, which serving as the enabler of copper wire-bonding in IGBT samples in ECTC2021. ECTC2021 samples with sintered copper plate did not show siginificant lifetime improvement comparing with the IGBT modules without such sintered copper plate in ISPSD2015. This hints that copper wirebonding itself is the decisive contributer for the lifetime improvement.

5.2 *PC*min lifetime model

In-depth failure analysis after PC_{min} revealed degradation in subtrate-baseplate soldering although the DUTs failed with on-state increase. Dependency of absolute temperatures and load duration should not be excluded due to the expected influence of solder creep on the lifetime. However, due to the limited datapoints, lifetime model including all variables under interest is impossible. Hence, RoadPak PC_{min} model has adapted from established lifetime model in literature which failed in solder degradation, the exponent terms of the variables were taken from the ISPSD2015 lifetime model for power modules with baseplate [11]. The constant was fitted to the RoadPak test data. Therefore, RoadPak PC_{min} model is described as:

$$N_{f,PCmin} = C \cdot \Delta T_j^{\beta_1} \cdot t_{on}^{\beta_2} \cdot e^{\left(\frac{\beta_3}{T_{jmax}}\right)} \qquad (2)$$

$$= 4.06 \cdot 10^{11} \cdot \Delta T_j^{-6.28} \cdot t_{on}^{-0.58} \cdot e^{\left(\frac{7296}{T_{jmax}}\right)}$$

The PC_{min} model (solid line) and the test data points are visualized in Fig. 10. The adaption source model (ISPSD2015) and the classic CIPS08 model under the same test conditions were included in the same plot [10][11]. Both models are based on Si-IGBT modules.

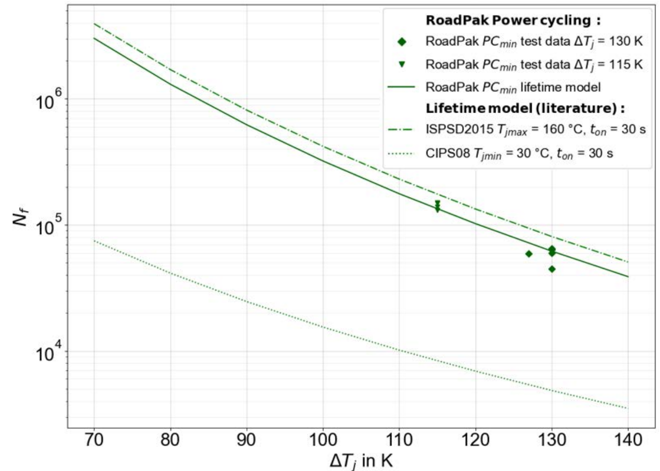

Fig. 10 RoadPak PC_{min} lifetime modeling and comparison with relevant lifetime models in literature [10][11].

Similar trend of lifetime enhancement by advanced packaging technologies can be concluded from the comparison with classic CIPS08 and other two models in the plot. In traditional power module packages, the dominating lifetime limiting factors are wire-bonds or soft chip-substrate solder, wheras novel packaging technologies such copper wire-bonding and silver sintering has eliminated such weak points and moved the failure spots to substrate-baseplate solder as shown in [11], thus realized more than tenfold lifetime improvement. The predicted lifetime of RoadPak is slightly below the predicted lifetime from source model (ISPSD2015) which modules failed with solder [10]; as the failure mechanism of RoadPak module after PC_{min} revealed a mixture of chip-near degradation as well as solder degradation. The retainment of weak spot such as chip aluminium can confine the transition of failure modes thus limit the full benefit of packaging technology upgrade. However, it has to be noted that the RoadPak platform has achieved comparable lifetime even with the use of SiC-based device, whose intrinsic material property such as higher young's modulus, already brings exceptional challenges for packaging design as well as production processes.

6 Conclusion

In this paper, the power cycling capability of RoadPak SiC module has been presented. The module packaging solution provided by RoadPak platform has demonstrated excellent capability to

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extract the most benefit of SiC chip technology and fulfilling the lifetime requirement of e-Mobility inverter, even in very harsh conditions. Operation lifetime requirement can be met without compromise.

It has been understood that the separation of failure modes due to high dependency of on-state characteristics of SiC-based device and R_{th} of module (cooling) is not trivial and needs to be better investigated.

The power cycling results as well as proposed lifetime model clearly showed the advantages and necessity of advanced module packaging technologies. The analysis has revealed that by using improved packaging technologies as of RoadPak, the failure mode will be shifted to chip metallization or the chip thermo-mechanical degradation. Thereby, one of the major bottlenecks as packaging reliability of SiC-based device is overcome and this unlocks the potential of SiC-based device.

7 Reference

[1] Mohn, Fabian, Chunlei Liu, and Juergen Schuderer. "Reliable interconnection technologies for high-temperature operation of SiC MOSFETs." In *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-8. VDE, 2017.

[2] U.S. Department of energy. “Electrification annual progress report FY2019”, available online: Electrification Annual Progress Report (FY2019) (Technical Report) | OSTI.GOV

[3] Mesemanolis, Athanasios, Milad Maleki, Samuel Hartmann, Antoni Ruiz, David Weiss, Gontran Paques, and Tobias Keller. "Fast and reliable switching of parallel SiC MOSFET chips in a Halfbridge module." In *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-8. VDE, 2020.

[4] Herold, C., J. Sun, P. Seidel, L. Tinschert, and J. Lutz. "Power cycling methods for SiC MOSFETs." In *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, pp. 367-370. IEEE, 2017.

[5] Maleki, Milad, Athanasios Mesemanolis, Lluis Santolaria, Antoni Ruiz, and Tobias Keller. "High power density SiC power module for Formula E: requirement, design considerations and the test results." In *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-7. VDE, 2021.

[6] Beyer, Harald, Milad Maleki, Martin Bayer, Swen Koenig, Fabian Fischer, and Gontran Paques. "Power Cycling Reliability and Failure Modes in Power Modules with Novel Emitter Contact and Sintering Technologies." In *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, pp. 1-6. VDE, 2020.

[7] ECPE Guideline AQG 324, “Qualification of power modules for use in power electronics converter units in motor vehicles,” available online: https://www.ecpe.org/research/workinggroups/automotive-aqg-324/

[8] Schmidt, Ralf, Ronny Werner, Jeffrey Casady, Brett Hull, and Adam Barkley. "Power cycle testing of sintered SiC-MOSFETs." In *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-8. VDE, 2017.

[9] Wagner, Felix, Gerhard Reber, Martin Rittner, Michael Guyenot, Maximilian Nitzsche, and Bernhard Wunderle. "Power cycling of SiC-MOSFET single-chip modules with additional measurement cycles for life end determination." In *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, pp. 1-6. VDE, 2020.

[10] Bayerer, Reinhold, Tobias Herrmann, Thomas Licht, Josef Lutz, and Marco Feller. "Model for power cycling lifetime of IGBT modules-various factors influencing lifetime." In *5th international conference on integrated power electronics systems*, pp. 1-6. VDE, 2008.

[11] Heuck, N., R. Bayerer, S. Krasel, F. Otto, R. Speckels, and K. Guth. "Lifetime analysis of power modules with new packaging technologies." In *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 321-324. IEEE, 2015.

[12] Schiffmacher, Alexander, David Strahringer, Shreyas Malasani, Juergen Wilde, Carsten Kempiak, and Andreas Lindemann. "In Situ Degradation Monitoring Methods during Lifetime Testing of Power Electronic Modules." In *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*, pp. 895-903. IEEE, 2021