# IGCT – a new, emerging technology for high-power, low-cost inverters

**The Integrated Gate-Commutated Thyristor (IGCT) combines the advantages of the hard-driven GTO thyristor, including its dramatically improved turn-off performance, with technological breakthroughs at the device, gate-drive and application levels. Homogeneous switching enhances the safe operating area of the IGCT up to the dynamic avalanche limits. Snubber circuits are no longer needed. Improved loss characteristics allow high-frequency applications extending into the kHz range. A new IGCT device family with integrated high-power diodes has been developed for applications in the 0.5–6 MVA range, extending to several 100 MVA with series and parallel connection. A first 100-MVA intertie based on the IGCT has been in commercial operation for nearly two years and confirms the very high level of reliability of this new technology. Other new applications using the IGCT platform include ABB's new ACS1000 drive for medium-voltage applications.**

Thyristor technology is inherently superior to transistors for blocking voltage values above 2.5 kV, plasma distributions equal to those of diodes offering the best trade-off between the on-state and blocking voltage. Until now, adding the gate turn-off feature has resulted in GTOs being constrained by a variety of unsatisfactory compromises. The widely used standard GTO drive technology results in inhomogeneous turn-on and turn-off transients that call for costly d*u*/d*t* and d*i*/d*t* snubber circuits [1, 2] combined with bulky gate drive units.

GTO technology has nevertheless found interesting applications in a power range of about 1 to 20 MVA, mainly involving adjustable-speed drives and railway interties. While developments in the new high-voltage IGBT [3] area have given these devices some advantages in areas where they compete with conventional GTO technology, dramatic improvements in the more traditional field have created a new technology known as IGCT, or Integrated Gate Commutated Thyristor [4]. The IGCT **1** represents the optimum combination of proven, low-loss thyristor technology and snubberless, cost-effective gate turn-off for demanding medium- and high-voltage power electronics applications.

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### Characteristics of the IGCT

The characteristics targeted in the IGCT development programme were achieved in steps that closely resembled the approach adopted for the IGBT. The development goals were:

- *Improved GTO switching characteristics* for operation without d*v*/d*t* snubbering at high current density
- *Reduced on-state and turn-off losses* through minimization of the silicon thickness
- *Reduced gate-drive requirements*, especially during conduction
- *Development of anti-parallel diodes* capable of snubberless turn-off at high d*i*/d*t*
- *High-frequency operation for continuous and dynamic conditions*
- *Integration of main switches* (GTO thyristor and diode) in one semiconductor package

For high-power applications some additional characteristics were necessary:

- *Enhanced reliability per MVA* by reducing the complexity and number of components
- *Extension of the power range* to several 100 MVA by means of cost-effective, reliable series and parallel connection

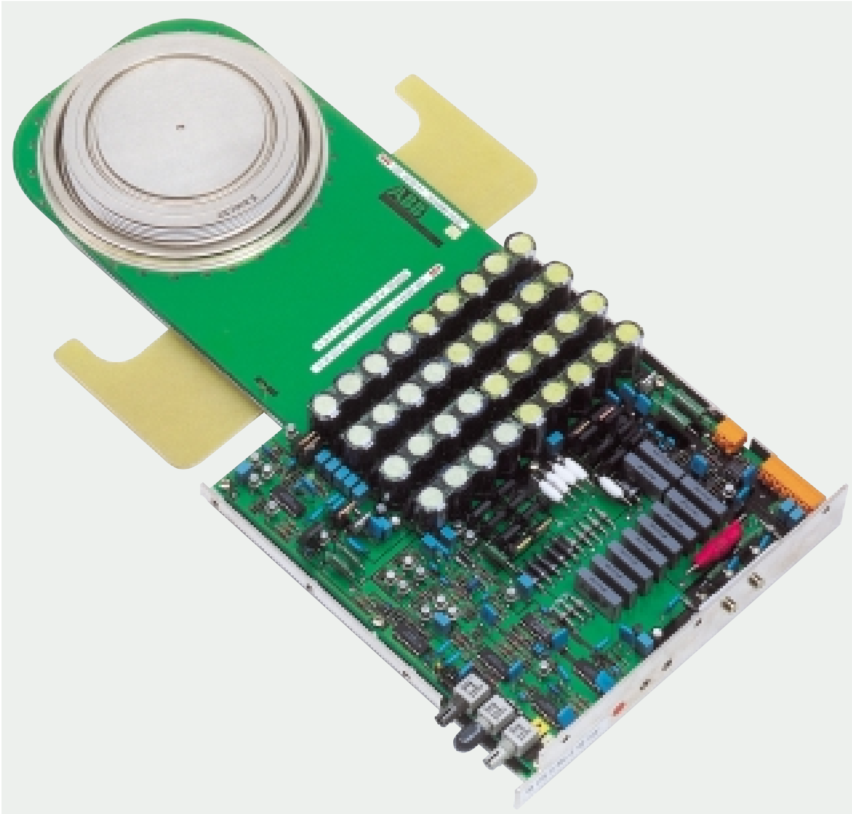
### Improved GTO switching characteristics

A dramatic improvement in the GTO turn-off SOA (Safe Operating Area) is achieved at high power (3 kA / 4.5 kV) with the so-called 'hard drive', in which an integrated gate drive commutates the cathode current to zero before the anode voltage starts to rise. The very low gate-circuit inductance that is required is obtained by means of a coaxial gate feed-through combined with a multilayer PCB gate drive connection; as a result, values ≥ 5 – 6 kA/µs can be achieved with a gate voltage of 20 V [5]. When the cathode current is zero, the remaining anode current is fully commutated to the gate unit, which remains in low-impedance mode. The gate-drive energy consumption is minimized by avoiding gate overdrive.

The 'hard' gate drive converts the thyristor from its pnpn latching state to a pnp mode within 1 µs. Turn-off takes place entirely in transistor mode, thus eliminating any possibility of latching. Turn-off is homogeneous as a result, enlarging the SOA to a full dynamic avalanche (peak turn-off energy equal to 250 kW/cm²). The device can be operated at the full-area physical limit of silicon. The possible turn-off currents per unit silicon area are on a par with the former snubbered turn-off currents of a best-in-class GTO device. **2** shows the typical turn-off waveform without dv/dt snubber.

### Reduced on-state and turn-off losses

A reduction in the device thickness of up to 30 % for the same forward breakdown voltage can be achieved by introducing a buffer layer on the anode side. Buffer layer power semiconductors easily outperform conventional devices, the main benefit of such thin devices being



***The IGCT (Integrated Gate-Commutated Thyristor)*** **1**

***Snubberless turn-off of the IGCT (storage time $t_s$ = 1.6 µs)*** **2**

| | | | |
|---|---|---|---|
| *U* | *Voltage* | Red | *Anode voltage* |
| *I* | *Current* | Green | *Anode current* |
| *t* | *Time* | Blue | *Gate voltage* |

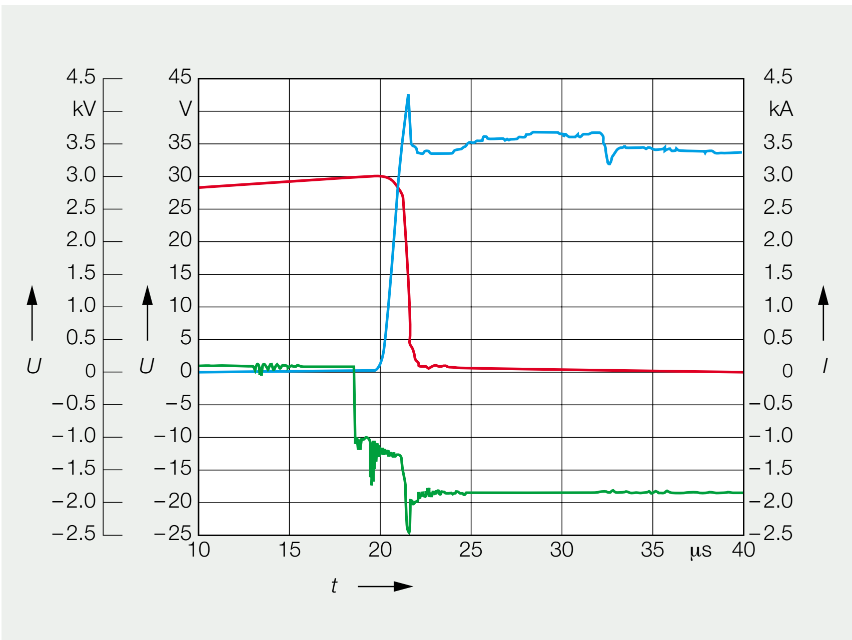


**Table 1:**
**Comparison of GTO, hard-drive GTO (HD-GTO) and the new IGCT**

*Junction temperature 125 °C; 85-mm wafer; 4.5-kV devices*

| | | GTO | HD-GTO | IGCT |
|---|---|---|---|---|
| On-state voltage | V | 3.2 | 3.2 | 2.4 |
| Max turn-on | A/µs | 500 | 3000 | 3000 |
| Typ turn-on energy | W | 5 | 1 | 0.5 |
| Turn-off energy at 3 kA | W | 10 (6 µF) | 13 (0 µF) | 10 (0 µF) |
| Snubber capacitance (3 kA turn-off) | µF | 6 | 0 | 0 |
| Max turn-off current | kA | 3 | 3 – 6 | 3 – 6 |
| Gate-drive power (500 Hz) | W | 80 | 30 | 15 |
| Gate stored charge | µC | 800 | 2000 | 2000 |
| Max turn-off (d*u*/d*t*) | V/µs | 500 | ≥4000 | ≥4000 |
| Storage time | µs | 20 | 1 | 1 |

an improved technology curve with lower on-state and switching losses. The buffer layer, within a four-layer device, eliminates anode shorts without compromising efficient extraction of electrons during turn-off. In the new IGCT devices the buffer layer is combined with a transparent anode, ie a pn-junction with current-dependent emitter efficiency. By means of an appropriate design, the electrons are extracted during turn-off as efficiently as with anode shorts. *Table 1* compares the improved characteristics of the new IGCT device with those of a conventional hard-driven and a standard GTO thyristor.

Due to its on-state operation in thyristor mode, the IGCT has inherently lower conduction losses than a comparable IGBT device. The buffer layer, which can be used with the IGCT as well as with the IGBT, is the common denominator that causes these two devices to have comparable switching losses (ignoring the higher turn-on losses of the IGBT, which implements gate-controlled d*i*/d*t* for the diode recovery protection). The improved loss characteristics and snubberless operation allow cost-effective IGCT applications with switching frequencies in the range of 500 Hz to 2kHz.

## Reduced gate-drive requirements

The characteristics usually having an impact on the design of a GTO thyristor gate drive are:

- The gate turn-off current (750 A at 3 kA turn-off) has to be pumped into a 300-nH gate circuit inductance. This requires a high gate charge ($Q_g$) per pulse ($Q_g = 0.5 t_s \times I_{GQM}$, where $t_s$ is the storage time and $I_{GQM}$ the peak turn-off

**Table 2:**
**IGCT product family with monolithically integrated anti-parallel diode**

| Voltage class | Silicon diameter [mm] | Item no | $I_{TGQM}$ [A] 3.3 kV DC | $I_{TGQM}$ [A] 2.7 kV DC | $I_{TGQM}$ [A] 1.9 kV DC | $E_{off}$ [Ws] | Max d*i*/d*t* [A/cm²] (diode part) | $I_{rr}$ [A] |
|---|---|---|---|---|---|---|---|---|
| | 38 | 5SGR04D4502 | | 340 | 480 | 1.1 | 130 | 110 |
| 4.5 kV $V_{DM}$ | 51 | 5SGX08F4502 | | 640 | 910 | 2.1 | 345 | 280 |
| (2.7 kV DC) | 68 | 5SGX14H4502 | | 1100 | 1560 | 3.6 | 525 | 430 |
| | 91 | 5SGX26L4502 | | 2250 | 3200 | 7.1 | 945 | 769 |
| | 38 | 5SGR03D6004 | 275 | | | 1.45 | 90 | 114 |
| 6 kV $V_{DM}$ | 51 | 5SGX06F6004 | 520 | | | 2.7 | 230 | 270 |
| (3.3 kV DC) | 68 | 5SGX10H6004 | 910 | | | 4.8 | 350 | 433 |
| | 91 | 5SGX19L6004 | 1820 | | | 9.6 | 630 | 780 |

$I_{TGQM}$ Maximum turn-off current
$E_{off}$ Turn-off energy at ITGQM
$I_{rr}$ Reverse recovery current at diode turn-off

current). Also, high losses are produced at the output MOSFETs.

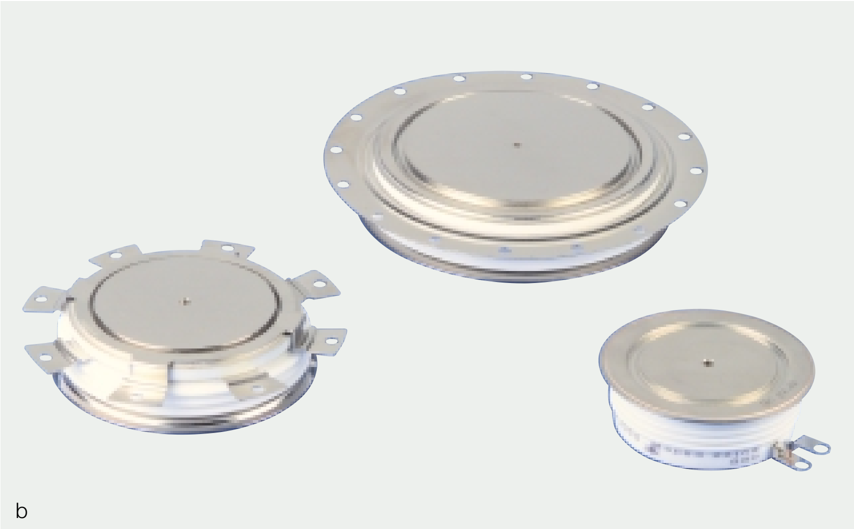
- The high gate back-porch current (typically 4 to 8 A for a 3-kA device) that is required, especially at low temperatures.

Considerably lower demands are made on the new GCT gate drives with respect to these characteristics:

- The storage time $t_s$ is reduced by a factor of approximately 20. Despite the increase in $I_{GQM}$ the required gate charge is reduced by a factor of about 4. Due to this and the larger number of paralleled devices needed to carry the high turn-off current pulse, the MOSFET losses are significantly reduced.
- The use of transparent anode technology reduces the back-porch current by factor of 20.

An additional requirement of the IGCT is low-inductive connection to the gate drive, which therefore has to be located as close as possible to the GCT. To achieve maximum robustness and compactness the gate drive has to surround the GCT, form an integral unit with the GCT and cooler, and carry only those parts of the circuit which are necessary for the gate drive 3a. As a consequence, the number of gate-drive components, the heat dissipation, electrical stress and internal thermal stress are all reduced, which significantly lowers the cost and failure rate of the gate drive. The IGCT, with its integrated gate drive, is easily snapped into the correct position in the stack and connected to its power supply and fiber-optic control. The carefully designed pressure contact system ensures that release of the spring causes a defined pressure to be exerted on the GCT, establishing both the required electrical and thermal contact. Maximum ease of assembly and the highest reliability are achieved in this way.

a



b

***The IGCT is designed for maximum robustness and compactness.*** **3**

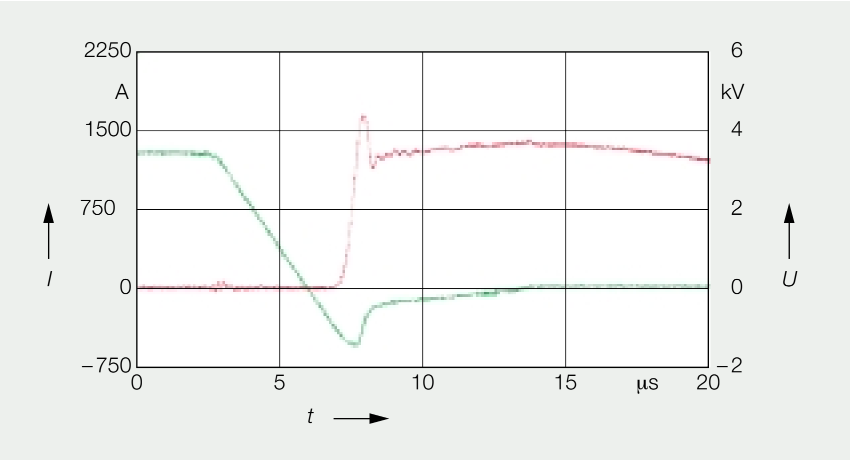
a *51-mm IGCT with integrated diode, gate drive and air-cooled heatsink*
b *Members of the IGCT family (51-mm, 68-mm and 91-mm, with integrated diode)*

### Snubberless turn-off at high d*i*/d*t* with anti-parallel diodes

Due to the snubberless operation of the IGCT, operation of its anti-parallel diode also has to be snubberless. Upgraded high-power presspack diodes manufactured using improved irradiation processes in combination with the classical (non-structured) processes fulfil these requirements 4. The d*i*/d*t* which is possible scales directly with the diode area.

### High-frequency operation for continuous and dynamic conditions

One of the most impressive capabilities of the GCT is its ability to handle high fre-




***Power diode characteristics during snubberless inductive turn-off (di/dt = 400 A/µs)*** **4**

*U* *Voltage*
*I* *Current*
*t* *Time*

Red *Anode voltage*
Green *Anode current*

quency turn-on/turn-off pulse bursts, whereas traditional GTO thyristors require a fairly long time between two consecutive turn-off operations. During turn-off, current redistribution across the GTO and current crowding lead to a non-uniform temperature distribution (which additionally provokes non-uniform turn-on). This situation can rapidly create hot spots and cause thermal runaway. Thus, the minimum time between consecutive GTO switching operations is basically determined by the time needed to return to uniform junction temperature. The GCT, however, overcomes this limitation because of its extremely uniform switching behaviour.

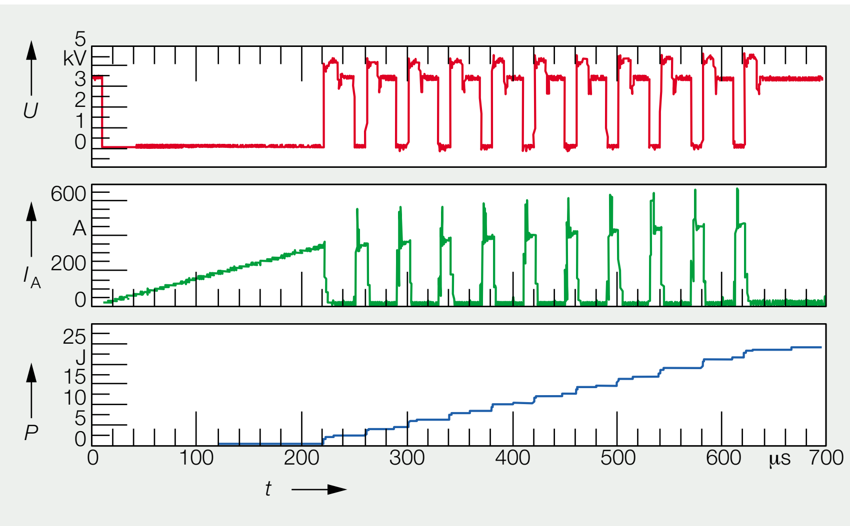
The heat that is generated during turn-off is evenly distributed across the entire device, which means that the GCT has no 'thermal memory' other than its virtual junction temperature. Therefore, the only parameter limiting the GCT switching frequency is its 'thermal budget'.

Since the thermal capacitances are much lower for short heating pulse durations than for steady state heating, short pulse bursts can be executed without excessive temperature excursions. **5** shows a 10-pulse, 25 kHz sequence with a 25 % duty cycle (10 µs on/ 30 µs off).

***25 kHz, 10-pulse test with 51-mm IGCT*** **5**

*DC-link voltage 3.3 kV; junction temperature 80 °C; turn-on 10 µs; turn-off 30 µs*

*U* *Voltage*
$I_A$ *Anode current*
*P* *Losses*
*t* *Time*




## Integration of main switches in one semiconductor package

In the past, the advantages of monolithic, non-punch-through GTO thyristor and diode combinations were always offset by the fact that the non-punch-through GTO thyristor required a thicker silicon wafer than its corresponding freewheeling diode. Thus, reverse-conducting GTO thyristor devices suffered from excessive diode losses. The new buffer layer concept of the GCT overcomes for the first time this trade-off in thickness. The optimum thickness of the punch-through GCT and its anti-parallel diode are essentially the same, making monolithic integration once again attractive.

This opportunity was seized for the purpose of developing a new IGCT product family **3b** (*Table 2*) with integrated freewheeling diode for snubberless operation [6]. A range of eight devices with integrated diodes covers the requirements of 2- and 3-level inverters for DC link voltages of up to 6.6 kV (2 × 3.3 kV) and turn-off currents of up to 3 kA (not concurrently), thus allowing the following inverters to be designed without series or parallel connection:

- 2-level inverters: 0.5 MVA to 3 MVA (4.5 MVA)
- 3-level inverters: 1 MVA to 6 MVA (9 MVA)

By using discrete 91-mm IGCT devices with separate anti-parallel diodes, maximum powers of about 4.5 MVA (2-level) or 9 MVA (3-level) are possible.

### Further improvement in reliability per MVA

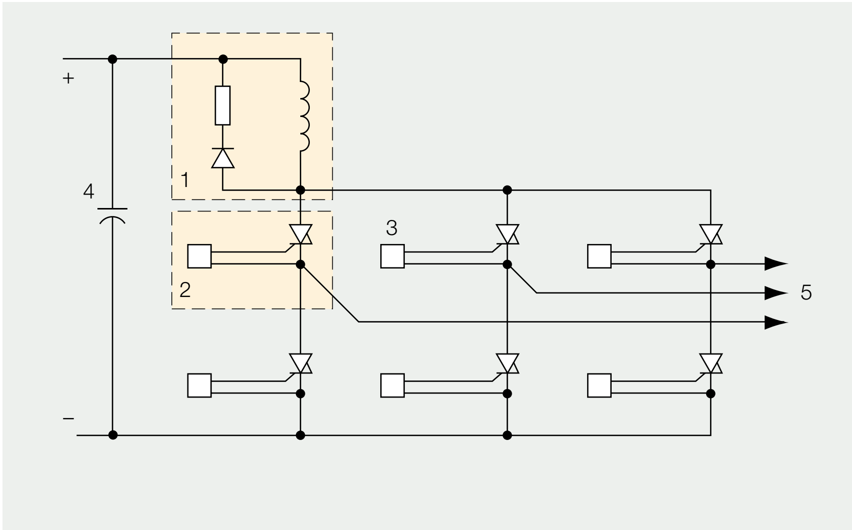
With the described devices, which can be operated without a d*v*/d*t* snubber, the classical GTO circuits are drastically changed. Omitting the snubber capacitors eliminates typical interactions such as:

- Oscillations between the snubber capacitor and inductor
- Conduction of snubber diodes due to changes in DC bus voltage
- Parasitic oscillations after device turn-on

The anti-parallel diode can be operated without a d*v*/d*t* snubber, but d*i*/d*t* control is still necessary to keep the reverse recovery of the diode within its safe operating area. Due to its thyristor nature, the GCT cannot provide d*i*/d*t* control. Instead, d*i*/d*t* control is achieved with an inductor, clamped by a diode and a resistor as in standard GTO circuits. This additional d*i*/d*t* clamp limits the current in the very unlikely event of a shoot-through.

A greatly simplified three-phase inverter circuit [7] can be obtained with only one d*i*/d*t* limiter **6** for all three phases. The preferred three-phase IGCT inverter therefore only needs 11 electrical components:

- 6 IGCTs
- 1 inductor
- 1 clamp diode
- 1 clamp capacitor (for high-inductive DC link only)



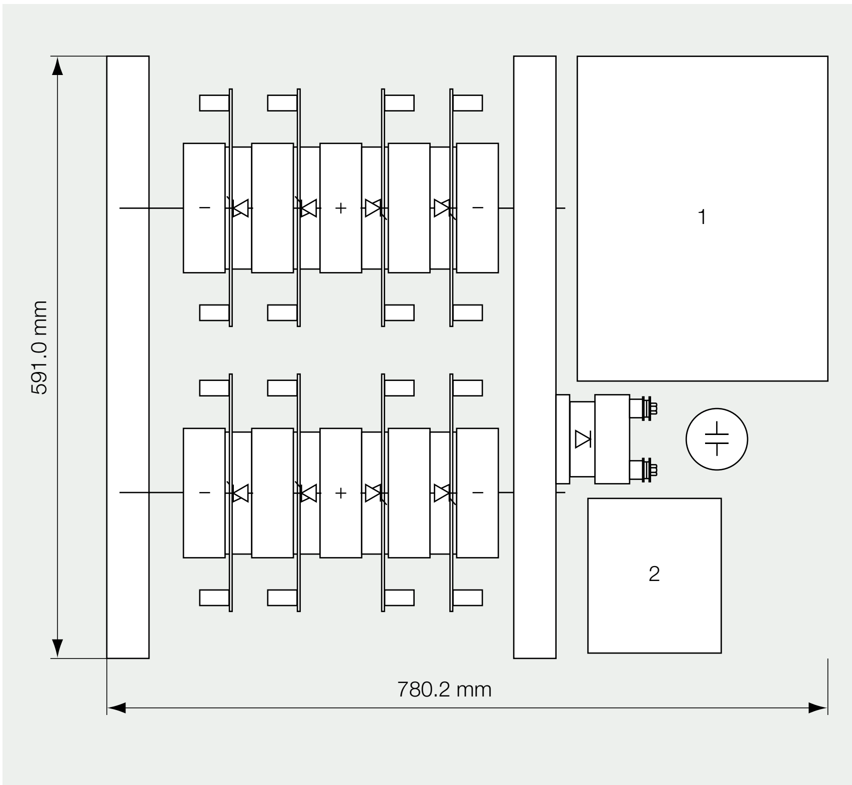

***Typical three-phase inverter circuit with IGCTs*** **6**

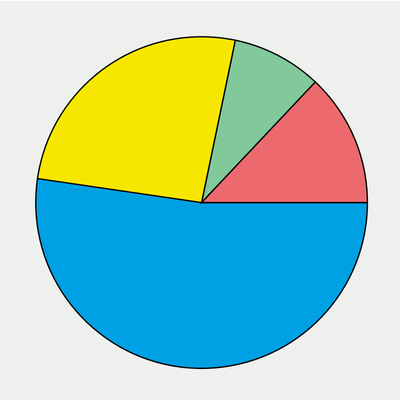
1 d*i*/d*t snubber*
2 *IGCT*
3 *Gate drive*
4 *DC link capacitor*
5 *3-phase output*

***Preliminary layout of 3-MVA sample inverter*** **7**

*Approx. size for 3 MVA: 780 × 590 × 330 mm*
*Approx. size for 0.9 MVA: 630 × 460 × 230 mm*

1 *Choke* 2 *Gate-drive supply*





***Break-down of predicted failure rate of a 3-MVA IGCT inverter (total MTBF > 45 years)*** **8**

| | |
|---|---|
| Blue | *Gate drive* |
| Yellow | *Gate-drive supply* |
| Red | *GCT* |
| Green | *Clamp* |

- 1 clamp resistor
- 1 gate-drive power supply

Due to the low parts count and proven technology, a high Mean Time Between Failures (MTBF) can be guaranteed for the inverter. A number of qualification tests, field experience with key components (up to 400 × $10^6$ device operation hours) and recent data obtained from a 100-MVA railway intertie [8] indicates that an MTBF ≥ 45 years or Failure In Time (FIT) ≤ 2300 (where 1 FIT = 1 failure in one billion hours) can be expected with a full 3-MVA, three-phase IGCT inverter **7**, **8**. The gate drives make only a very small contribution to the FIT rate, the main contribution coming from the fiber optics and logic circuits. The power devices (including the pulse capacitors) have low, predictable FIT rates, as in the case of standard GTO gate drives.

## Expansion of power range by several 100 MVA

Typical maximum values for GTO technology are at present 6 kV for the dynamic blocking voltage and 6 kA for the turn-off current. These figures correspond to a maximum NPC inverter power (NPC = neutral-point clamped or 3-level inverter) without series-connected devices of about 15 MVA. The future power electronics systems market will, however, require converter powers which clearly exceed this value. Inverter ratings of several 100 MVA will be needed in the near future. The key to future high-power applications lies in the series connection of controlled turn-off devices.

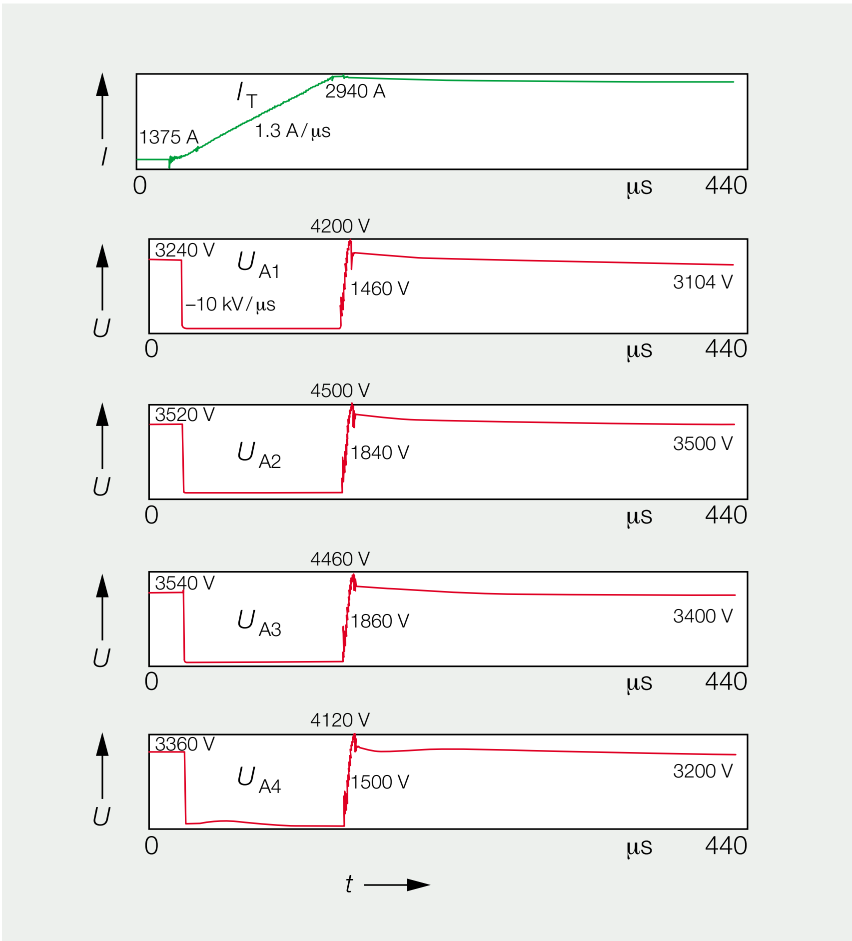
Series-connected thyristors are a proven high-voltage DC transmission technology, and such configurations have been used successfully for decades in this area. Due to its inherently short storage time of 1 µs, the IGCT allows the simple, reliable series connection which is fundamental to the design of extra-high-power inverters.

In series connections, the established method used to ensure maximum equipment availability is to insert more IGCTs in series than are necessary. This makes sense since it improves the installation in a number of ways:

- In the event of an IGCT or anti-parallel diode failure operation will continue without interruption. This is because the IGCT, being a presspack device, is

***Turn-off of four series-connected 3-kA IGCTs at a DC link voltage of 13.2 kV*** **9**

| | |
|---|---|
| $I_T$ | *Load current* |
| $U_{A1\text{-}A4}$ | *Anode voltages of GTOs 1,2,3,4* |
| $t$ | *Time* |



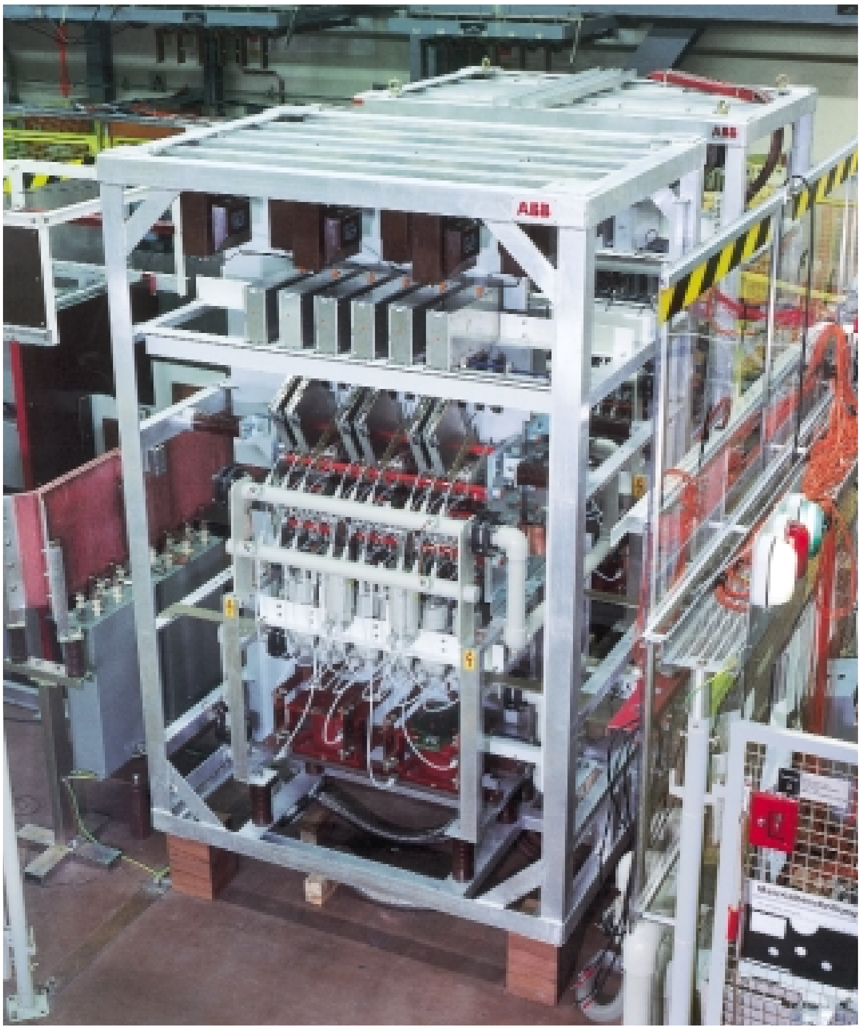
designed to behave as a short circuit when it fails. The failure is detected by an electronic circuit and signalled over fiber-optic cables. The failed device can be replaced at leisure, during routine maintenance.

- The addition of redundant IGCTs reduces the voltage load of each individual device, including any eventual snubber circuit. It is known that the lifetime of an individual device depends strongly upon the voltage stress. When it is reduced, eg by one third, the average lifetime of the device is increased by a factor of about 20.
- The incorporation of redundant devices reduces the risk of shoot-through in a converter phase, thereby allowing fuseless high-power converters to be built. This fuseless design improves converter reliability and efficiency. Thus shoot-through in a converter phase is very unlikely. Nevertheless, the converter is constructed to withstand the stresses during such fault conditions.

**9** shows the oscillogram of the simultaneous turn-off of four series-connected IGCTs. Due to the very short storage time of the IGCT (1 µs) and therefore the even smaller spread in turn-off times of the different devices (less than 0.2 µs), very good voltage sharing of the series-connected devices is achieved. To minimize dynamic overvoltages, the high-power phase module was constructed with very low inductance.

Future innovations that may be expected in the application of IGCTs include:

- Further reduction or elimination of the d*u*/d*t* snubbers for series-connected turn-off devices
- Higher switching frequencies of up to 1 kHz or more
- An anode-derived drive supply, made possible by the reduced gate drive power requirements of transparent-anode IGCTs

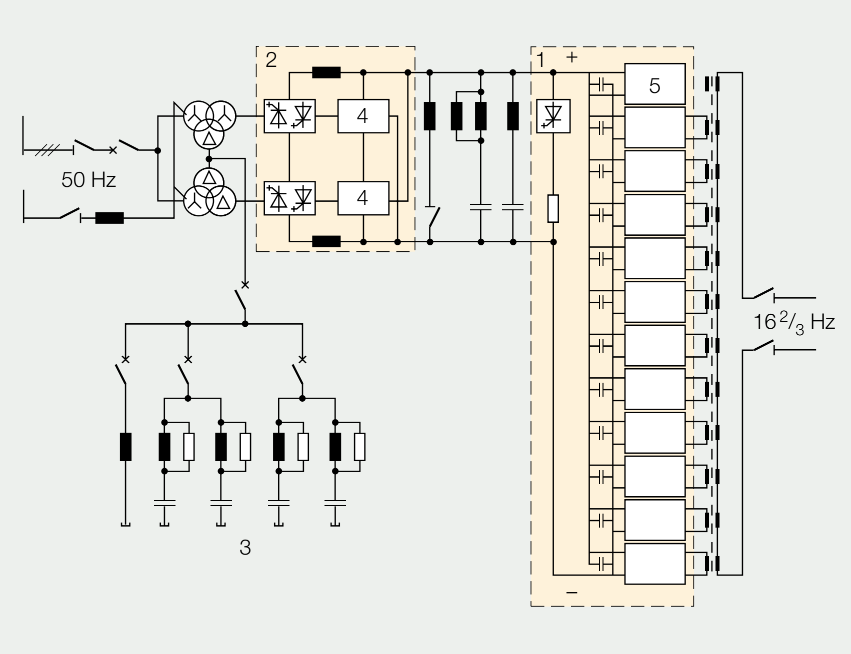


***High-power IGCT inverter module, for which a design with 6 series-connected devices is normally chosen. Each 4.5-kV device of the module can be loaded with a maximum of 3 kV DC. It is equipped with reduced du/dt snubbers of a simple RCD type. The gate-drive supply is realized with special isolation transformers.*** **10**

The first commercial application of the high-power IGCT inverter modules – in a 100-MVA intertie [8] that has been operating since mid-1996 **10**, **11** – followed an extensive programme of simulation and verification. The field experience gained with this installation has been excellent. Of the more than 300 IGCTs installed in the intertie only one unit has failed to date, having been due to a contact problem involving a light-emitting diode. This confirms the high reliability figures expected of IGCT technology (<400 FIT per IGCT level).

The impressive reliability figures are partly due to the reduced voltage stress that results from series connection of IGCTs with redundant devices. The further reduction in components due to snubberless operation will increase the reliability in the future, pushing it even closer to that of conventional thyristor technology (<100 FIT per level).

The inherent reliability of IGCT operation coupled with device redundancy is the cornerstone on which future extra-high-power converters will be built, in particular for the new emerging FACTS and Custom Power markets.




***100-MVA intertie based on series-connected IGCTs (in operation since mid-1996)*** **11**

1 *IGCT converter*
2 *Thyristor converter*
3 *Harmonic filters*
4 *Common turn-off circuit*
5 *H-bridges*

**Conclusions**

The IGCT combines all the important innovations needed for future power electronics applications and will become the key component for future medium- to high-voltage applications in the range from 0.5 MVA to several 100 MVA. It inherently enables simple and robust series connection of turn-off devices for high-power applications. The additional advantages of the IGCT over other turn-off devices (eg, low cost, low complexity and high efficiency) means that it has no real competition in this power range. The IGCT is available today from several manufacturers of high-power semiconductors.

The IGCT has also demonstrated high reliability in its first 100-MVA intertie application at Bremen. A second intertie, based on the same technology and rated at 2 × 66 MVA, has been ordered by German Railway (DB) on the basis of the excellent experience with this installation.

Additionally, ABB has successfully launched a new medium-voltage drive family – the ACS 1000, for applications in the range of 0.5 to 6 MVA [9] – several units of which are already in successful operation in industry.

**References**


[1] **T. M. Undeland:** Snubber for pulse width modulation bridge converters with power transistors or GTO. Int. Power Electr. Conf. (EPCD), Tokyo, 1983, 313–323.

[2] **W. McMurray:** Efficient snubber for voltage source GTO inverter. IEEE Trans. Power Electron., vol PE-2, no 3, 1987, 264–272.

[3] **K. Ishil, Y. Konishl, M. Takeda, E. Thal, G. Debled:** A new high power, high voltage IGBT. Conf. Rec. of PCIM, Nuremberg, 1997.

[4] **H. M. Stillman:** IGCTs – megawatt power switches for medium-voltage applications. ABB Review 3/97, 12–17.

[5] **H. Grüning:** Low-inductive GTO terminal. Patent EP 0588026 and US 5345096, 1992.

[6] **S. Linder, S. Klaka, M. Frecker, E. Carroll, H. Zeller:** A new range of reverse conducting gate-commutated thyristors for high voltage, medium power applications. EPE, Trondheim, Norway, 1997.

[7] **H. Grüning, B. Ødegård:** High performance low cost MVA inverters realized with integrated gate commutated thyristors (IGCT). EPE, Trondheim, Norway, 1997.

[8] **R. Boeck, O. Gaupp, P. Dähler, E. Bärlicher, J. Werninger, P. Zanini:** Bremen's 100 MW static frequency intertie. ABB Review 9/10-96, 4–17.

[9] **S. Malik, D. Kluge:** ACS 1000 – world's first standard AC drive for medium-voltage applications. ABB Review 2/98, 4–11.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