Technical Data

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Forward counter, 1 out of 10 with LED R 441.4

Description
The forward counter R 441.4 counts the 0-1 transitions at the counter input Z. A 1-signal at the blocking input S will stop the counting process, while the counter record is maintained. A 1-signal at the clearing input R or applying the operating voltage causes clearing of the counter. A 1-signal will then appear at the output Q0, 0-signal at the outputs Q1 ... Q9. One of the ten outputs will always carry a 1-signal, the remaining nine outputs have 0-signal. After the first counting impulse, a 1-signal will therefore be at output Q1, after the second one at Q2 and so on.

The inputs Z, S and R are delayed for noise suppression. There is an additional possibility to increase the clearing delay by linking the terminals 8 and 9 and of increasing the counting delay by linking the terminals 9 and 10.

For multi-decade counting the output UT of the unit decade is connected to the counting input Z of the tens counter etc. If such a multi-decade counter is to run in delayed operation, only the unit counter may be delayed by linking the terminals 8 and 10.

For multidecade counting and use of the disable input, only the first decade may be disabled. The subsequent decades must be operated without delay. If a delay of the reset input R is required, connections 8 and 9 must be linked at all decades.

The transition output UT gives a 1-signal when the outputs Q0 ... Q4 carry 1-signals.

The signal state of outputs Q1 ... Q6 is indicated by LEDs. One yellow LED each lights up in the case of a 1 signal at outputs Q1 ... Q9 and a green LED lights up in the case of a 1 signal at output Q0.

The outputs can switch inductive loads without use of free running diodes.

Order code for module:
GH R441 0400 R1
Order code for circuit symbol transparency:
GH R700 1901 R55
Order code for application:
D NG 80770 D
Identifying colour:
blue
Mechanical structure:
double width
Weight:
approx. 200 g

Technical data
Current consumption
Input
1 load
10 loads
Fan out per output
2 kHz
Maximum counting frequency without link
200 Hz
with link 9–10
Making delays (typical)

\[ t_d (0-1) \]

<table>
<thead>
<tr>
<th>Condition</th>
<th>( t_d (0-1) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>at Z (without link)</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>at Z (with link 9–10)</td>
<td>2.0 ms</td>
</tr>
<tr>
<td>at S</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>at R (without link)</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>at R (with link 8–9)</td>
<td>2.0 ms</td>
</tr>
</tbody>
</table>
Description

The up/down counter R 444.3 counts the 0-1 transitions at the counting input Z. A 1-signal at the blocking input S will block the counting process, while the counting record is maintained. A 1-signal at the clearing input Ü or applying the operating voltage will cause setting of the counter to a value pre-determined by signals at the inputs A - D. The desired counter record is fed to the inputs A - D in the form of a binary coded decimal number (see table below).

One of the ten outputs will always carry a 1-signal, while the remaining nine outputs show 0-signals.

The counting direction is always set at the input for up/down counting VR. An 0-signal means reverse counting, that is, D, 0, 9, 8, 7 etc. A 1-signal means forward counting, that is, 1, 2, 3 etc. The counting direction may only be changed during a 1-signal at the counting input Z, with simultaneous 0-signal on blocking input S if multi-decade counting is desired.

In the case of multi-decade counting the inputs S of the decades 2 to n should not be used.

The inputs Z, S and Ü are delayed for noise suppression. There is the additional possibility of increasing the counting delay by a link between the terminals 10 and 0.

For multi-decade counting the transition output Ü of the unit counter is connected to the counting input of the tens counter etc. For multi-decade counting and use of the disable input, only the first decade may be disabled. If a multi-decade counter of this type is to be operated in delayed run, only the counting input Z on the unit counter may be delayed by a link between the terminals 10 and 0.

In forward counting a 1-signal will appear at the transition output ÜT during the counter states 0 - 8; at 9 only so long as at Z a 1-signal also exists. Only by S = 0 and Q9 = 1 does a 0-signal appear at ÜT.

In reverse counting the transition output ÜT will have a 0-signal when S = 0-signal and Q9 = 1-signal. By all other counter states a 1-signal appears at ÜT.

Order code for module:

Order code for circuit symbol transparency:

Order code for application:

Identifying colour:

Mechanical structure:

Weight:

This unit replaces the version GH R444 0000 V0

### Technical data

Current consumption

20 mA

Input at Z, S, Ü, VR, A - D

1 load

Fan out of each output

10 loads

The inputs VR and A - D are not delayed

Max. counting frequency without linking

2 kHz

with linking D - 10

200 Hz

Making delays (typical)

<table>
<thead>
<tr>
<th>at Z (without link)</th>
<th>0.2 ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>at Z (with link 0-10)</td>
<td>2.0 ms</td>
</tr>
<tr>
<td>at S</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>at Ü</td>
<td>0.2 ms</td>
</tr>
</tbody>
</table>

### Binary-code decimal figure (BCD)

<table>
<thead>
<tr>
<th>Decimal figure</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
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<tr>
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<tr>
<td>6</td>
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<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

0-1 combinations other than given above should not be fed to inputs A to D in the case "setting".
Description

The up/down counter R 444.4 counts the 0-1 transitions at the counting input Z, or the 1-0 transitions on S (Z = 1-signal). A 1-signal at the blocking input S will block the counting process, while the counting record is maintained.

A 1-signal on the clearing input R brings the counter into the 0-state. The counter remains cleared so long as this signal is applied.

The changing of counting direction is carried out at input VR. An 0-signal means reverse counting, a 1-signal forwards counting. If multi-decade counting is desired the counting direction may only be changed during a 1-signal at Z and an 0-signal at S. In the case of multi-decade counting the inputs S of the decade 2 to n should not be used.

The outputs give the counter state in BCD or BINARY 1 out of 16 code.

The counter can be pre-set to a specific number. This number is applied to outputs Q1…Q4 in BCD or BINARY code. The information is transferred to the counter by means of a transfer pulse at the input U. The information may not be modified during the transfer pulse.

For multi-decade counting the transition output UT of the unit counter is connected to the counting input of the tens counter etc.

For multi-decade counting and use of the disable input, only the first decade may be disabled.

The signal inputs of the counters are delayed for noise suppression.

The outputs can switch inductive loads without flywheel diodes.

Order code for module, output BCD code: GH R444 0004 R1
Order code for module, output BINARY code: GH R444 0004 R2
Order code for circuit symbol transparency: GH R700 1901 R51
Order code for application: D NG 80707 D
Identifying colour: blue
Mechanical structure: single width
Weight: approx. 110 g

Technical data

Current consumption 20 mA
Input, at R
at Z, S, VR and U
1 load
Fan out, output Q1—Q4
100 loads
output UT
3 loads
Maximum counting frequency 100 Hz
Signal delay times, input Z, S
Input R
Input VR
Input U
typical
2.5 ms
typical
4 ms
typical
0.2 ms
typical
4 ms

Binary-code decimal figure (BCD)

<table>
<thead>
<tr>
<th>Decimal figure</th>
<th>A</th>
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<th>D</th>
</tr>
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<tbody>
<tr>
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<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

0-1 combinations other than given above should not be fed to outputs Q1 to Q4 in the case “setting”.

The following additionally applies for BINARY 1 out of 16 code:

| 10 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |
| 12 | 0 | 0 | 1 | 1 |
| 13 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 |
Description
The synchronization module R 445.1 precedes the up/down counters R 445.4 or R 445.5 for the configuration of one decade or multidecade counters. It synchronizes the signals controlling the counters and, after time matching, passes them on to the counter stages, thus eliminating the need for further preceding modules for the configuration of multidigit counters.
The 0-1 transitions at the counting input Z are counted. A 1 signal at the reset input R sets all counters to 0.
The counters remain reset as long as this signal is applied.
The counting process is prevented and the counter reading remains, by means of a 1 signal at the disable input S. No counting pulses can be triggered off with the disable input and disabling can start or can be cancelled irrespective of the signal state in the input Z. The disable input is actuated while the counter is just processing a pulse, this completely finishes its cycle.
The counting direction is switched over at input VR. A 0 signal signifies down counting and a 1 signal signifies up counting. The input VR can be actuated independently of the signal states of the remaining inputs. Switchover of the counting direction at the maximum counting frequency also ensures errorless counting. If, in this case, the counter pulse edge falls in the direct proximity of the up/down switchover signal, the counting pulse is either counted up or down, or, in threshold cases, simply suppressed.
A 1 signal at the transfer input QS results in transfer to the counter of the data superimposed at the counting decade outputs.
The verify input RM is linked to the carry output QU of the highest order counting decade in order to ensure that the counter does not run past its "stop position". In the case of three-digit operation, the counter then does not count further than 999 in up direction and 000 in down direction. If this behavior is not desired, a 1 signal (+ supply voltage Uo) must be applied to the verify input.
The transfer output QUS is linked to all transfer inputs US of the following counter stages. The output QUS is also used to supply the "self proselect switch". Noise suppression decoupling and perhaps also amplification may be necessary for this purpose.
The up/down output QVF is linked to all up/down inputs VR of the subsequent counter stages.
The counting pulse output QZ is linked to all counting inputs ZT of the subsequent counter stages. QZ has a constant 1 signal and only briefly changes to a 0 signal during processing of a pulse.
The reset output QR is linked to all reset inputs R of the subsequent counter stages.
The inputs reset R and transfer US are synchronized, i.e. the first counting pulse is reliably recognized by all counter stages after their deactivation.
Together with 1 to 6 up/down counters R 445.4 or R 445.5, the synchronization module processes a frequency from 0 to 2 kHz. The delays of the other signal inputs are chosen such that a maximum counting frequency from 700 to 2000 Hz (depending on the application) is guaranteed also in the case of differing applications.
The outputs can switch inductive loads without free running diodes.

Technical data
Current consumption, all inputs 0 signal
Input loads, per input
Fan out, per output
Signal delay,
After a switchover of counting direction, no counting pulses are processed for approximately 0.5 ms for synchronization. After a set or reset signal has been cancelled, the first counting pulse is once again assumed at the latest after 0.35 ms.

Order code for module:
GH R445 0100 R1
D NG 3124 80 D
Identifying colour:
blue
Mechanical structure:
single width
Weight:
approx. 120 g
Rotating direction logic R 445.2

Description
The rotating direction logic R 445.2 precedes the up/down counters R 445.4 or R 445.5 for the configuration of single-decade or multidecade counters. It synchronizes the signals controlling the counters and passes them on to the counter stages after time matching to eliminate the need for further preceding units for the configuration of multifigigit counters.

The module processes shaft encoder inputs arriving via two channels (K1 and K2) with a 90° phase shift. The signals are converted to counting pulses and a rotating direction signal. Shaft encoders with TTL outputs can also be connected. For this purpose, the wire links A and B must be removed from the module. If the counter counts in the wrong direction after connection of the shaft encoder, the wires at inputs K1 and K2 must be interchanged.

A signal at the reset input R sets all counters to zero. The counters remain reset as long as this signal is pending.

A signal at the disable input S prevents the effects of counter inputs K1 and K2. No counting pulses can be triggered off with the disable input and disabling can start or be cancelled independently of the signal state at K1 and K2. If the disable input is actuated, while the counter is just processing a pulse, this pulse is still completed.

Technical data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption, all inputs 0 signal</td>
<td>20 mA</td>
</tr>
<tr>
<td>all inputs 1 signal</td>
<td>40 mA</td>
</tr>
<tr>
<td>1 load</td>
<td></td>
</tr>
<tr>
<td>Input loads, per input</td>
<td>100 μA each</td>
</tr>
<tr>
<td>If inputs K1 and K2 used as TTL inputs (links A and B removed)</td>
<td>240 μA each</td>
</tr>
<tr>
<td>Input current</td>
<td>30 loads</td>
</tr>
<tr>
<td>at input voltage 2.4 V</td>
<td>typically</td>
</tr>
<tr>
<td>at input voltage 5.0 V</td>
<td>typically</td>
</tr>
<tr>
<td>Fan out, per output</td>
<td></td>
</tr>
<tr>
<td>Signal delay, encoder inputs K1 and K2</td>
<td>0.15 ms</td>
</tr>
<tr>
<td>typically</td>
<td></td>
</tr>
<tr>
<td>other inputs R, S and US</td>
<td>0.20 ms</td>
</tr>
<tr>
<td>The first counting pulse is taken on once again after cancelling a set or reset signal at the latest after 0.30 ms.</td>
<td></td>
</tr>
</tbody>
</table>
**Description**

The simultaneous logic R 445.3 proceeds the up/down counters R 445.4 or R 445.5 in the configuration of single and multidecade counters. It synchronizes the signals controlling counters and passes them on at the proper times to the counter stages in order to omit the need for further preceding units in the configuration of multidigit counters. The module processes the incoming counting pulses on two mutually independent counting pulse lines. In this case, the pulses of the first counter line have counting action and those of the second line cause down counting. If required, both counting lines can also be processed in the same counting direction.

Counting is by means of the 0-1 transitions at the up counter input ZV and the down counter input ZR. The counting signals of the two pulse inputs may be asynchronous with respect to each other and may also occur simultaneously. If both inputs are to have an up counting effect, inputs VR must be connected to the supply voltage + U, in the case of the subsequently connected counters R 445.4 respectively R 445.5. The counter inputs VR are left unwired if both inputs are to operate in down counting mode. A 1 signal at the reset input R resets all counters to 0. The counters remain reset as long as this signal is applied.

Counting is prevented and the counter reading is filled by means of a 1 signal at the disable input S. No counting pulses can be triggered off with the disable input and disabling can start or be cancelled independently of the signal state at inputs ZV and ZR. If the disable input is activated while the counter is just processing a pulse, this pulse is still completed.

A 1 signal at the transfer input US causes transfer to the counter of the data superimposed at the counting decade outputs.

The verify input RM is linked to the carry output QO of the highest order counting decade in order to ensure that the counter does not run past its 'stop point'. In the case of three-digit operation, the counter then does not count further than 999 in up counting direction and does not count past 000 in down counting direction. If this behavior is not desired, a 1 signal (+ U) must be applied to the verify input.

The transfer output QUS is linked to all transfer inputs US of the following counter stages. The output QUS is also used to supply the "set preselect switch". Noise decoupling and perhaps also amplification is necessary for this purpose.

The up/down output QVR is linked to all up/down inputs VR of the following counter stages. During arithmetic counting, the signal is inverted in the case of negative numbers. The output QVR remains unaltered when the pulses ZV and ZR are to be processed in the same counting direction. The up/down inputs VR of the counter stages are then linked either to + U (up counting) or remain unwired (down counting).

The counting pulse output QZ is linked to all counting inputs ZT of the subsequent counting stages. QZ constantly has a 1 signal and only briefly changes to a 0 signal when a pulse is processed.

The reset output QR is linked to all the reset inputs R of the subsequent counting stages.

The inputs reset R and transfer US are synchronized, that is to say the first counting pulse from all counter stages is reliably recognized after their deactivation.

In conjunction with 1 to 6 up/down counter R 445.4 or 445.5, the simultaneous logic processes input counting frequencies from 0 to 1 kHz per counter input. The maximum counting frequency may be lower in the case of certain applications. Excessively high input frequencies result in single pulses either no longer being accepted or may cause entire failure of pulse processing.

The outputs can switch inductive loads without free running diodes.

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**Order code for module:** GH R445 0300 R1
**Order code for application:** D NG 3122 80 D
**Identifying colour:** blue
**Mechanical structure:** single width
**Weight:** approx. 130 g

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**Technical data**

**Current consumption, all inputs 0 signal:** 20 mA
**all inputs 1 signal:** 40 mA
**Input loads, per input:** 1 load
**Fan out, per output:** 30 loads
**Signal delay, all inputs:** 0.2 ms

At the latest after 0.6 ms, the first counting pulse is once again accepted after cancelling a set, disable or reset signal.
Description
The up/down counter R 445.4 is included in the counter unit concept R 445. Counter chains configured with these counters always require a preceding logic in order to match the incoming signals to each other (e.g., R 445.1, R 445.2, R 445.3). The maximum counting frequency depends on the signal delay of the preceding logic.

Counting is by means of the 0-1 transitions at the counting input ZT.

A 1 signal at the reset input R sets the counter to zero. The counter remains reset as long as this signal is applied.

The counting direction is switched over at the input VR. A 0 signal signifies down counting and a 1 signal signifies up counting.

Outputs QA to QD give the counter reading in BCD or BINARY 1 out of 16 code.

The counter can be preset to a certain number. This number is applied to the outputs QA to QD in BCD or BINARY code. The information is transferred to the counter by means of a transfer pulse (1 signal) at the input US. The information must not be changed during the transfer pulse.

For multidecade counting, the carry output QU of the units counter is linked to the carry input ZU of the tens counter etc. No more than six decades should be connected.

The outputs can switch inductive loads without free running diodes.

Order code for module:

| output BCD code: | GH R445 0400 R1 |
| output BINARY 1 out of 16 code: | GH R445 0400 R2 |
| Order code for circuit symbol transparency: | GH R700 1901 R75 |
| Order code for application: | see modules R 445.1, R 445.2 and R 445.3 |

Identifying colour: blue
Mechanical structure: single width
Weight: approx. 120 g

Technical data
Current consumption:
- all inputs and outputs 0 signal: 11 mA
- all inputs 0 signal, four outputs 1 signal: 40 mA

Input loads, per input:
- 1 load: 100 loads
- 30 loads

Fan out, outputs QA . . . QD, per output QU:

Signal delay:
- counter input ZT: typically 15 µs
- counter input ZU: typically 26 µs
- reset input R: typically 26 µs
- up/down switchover VR: typically 26 µs
- set input US: typically 26 µs
Up/down counter
BCD and 1 out of 10
R 445.5

Description
The up/down counter R 445.5 is included in the counter unit concept R 445. Counter chains configured with these counters always require a preceding logic in order to match the incoming signals to each other (e.g. R 445.1, R 445.2, R 445.3). The maximum counting frequency depends on the signal delay of the preceding logic.

Counting is by means of the 0-1 transitions at the counting input ZT. A 1 signal at the reset input R sets the counter to zero. The counter remains reset as long as this signal is applied.

The counting direction is switched over at the input VR. A 0 signal signifies down counting and a 1 signal signifies up counting.

Outputs QA to QD give the counter reading in BCD code. Outputs Q1 to Q0 give the counter reading in 1 out of 10 code, which is indicated by LEDs.

The counter can be preset to a certain number. This number is applied in BCD code to outputs QA to QD via a decade selector switch (see figure). The information is transferred to the counter by means of a transfer pulse (1 signal) at the input US. The information must not be changed during the transfer pulse.

For multidec count, the carry output QU of the units counter is linked to the carry input ZU of the tens counter etc. No more than six decades should be connected.

The outputs can switch inductive loads without free running diodes.

Order code for module:
Order code for circuit symbol transparency:
Order code for application:

Identifying colour:
Mechanical structure:
Weight:

Technical data
Current consumption, counter reading 0, all inputs 0 signal:
  count reading 7, all inputs 0 signal:
Input loads, per input:
Fan out, outputs QA ... QD, Q1 ... Q0, per output:
  output QU:
Signal delay, counter input ZT:
  counter input ZU:
  reset input R:
  up/down switchover VR:
  set input US:
Colours of LEDs, outputs Q1 ... Q9:
  output Q0:

<table>
<thead>
<tr>
<th>Decimal figure</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
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<tbody>
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<td>0</td>
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</tbody>
</table>

0-1 combinations other than given above should not be fed to outputs QA to QD.
Description

The R 447.4 shift register can take in or give out information up to 8 bit (digits) either in sequence or at the same time.

The register can deal with all four possible operation modes:

- Parallel input → parallel output
- Parallel input → series output
- Series input → parallel output
- Series input → series output

For parallel input of information at inputs A ... H a 1-signal must be applied at input PS. With 0-1 transition at T, all input information on A ... H will be switched through to the corresponding outputs Q1 ... Q8.

The series input works with an 0-signal at PS. The information from input A is transferred through an 0-1 transition at the impulse input T to the output Q1 as a 1-signal. At each successive 0-1 transition at T, the relevant information at outputs Q1 ... Q8 is shifted one place in the direction of the arrow in the circuit symbol.

With the application of a 1-signal at input S, the impulse input T is blocked.

The register can be cleared by an 0-1 transition at input R (Q1 ... Q8 = 0-signal). Should the register be stopped in a cleared position, a 1-signal must be applied simultaneously at S.

It is guaranteed that, with applying the supply voltage, no matter what the information is present at the inputs, all outputs will show 0-signals until the impulse signal at T is applied. Inputs T, S, R and PS are fitted with a delay for noise suppression.

In serial shift mode (PS = 0), the input A is also delayed. Inputs A ... H are undelayed in parallel setting mode.

The delayed clock (disabling AND gate T and S) is available at output QT. QT is the + terminal on the left-hand side of the unit, the power supply being connected to the + and 0 V terminals on the right-hand side.

Outputs Q1 ... Q8 are indicated by yellow LEDs. All outputs can switch inductive loads without flywheel diodes.

Order code for module:
GH R447 0004 R1
GH R700 1901 R30

Order code for circuit symbol transparency:
D NG 3132 80 D
blue
double width
approx. 230 g

Technical data

see page 6/11
Impulse diagram for shift register R 447.4

Technical data

Current consumption, all outputs 0 signal
all outputs 1 signal
Input load, per input
Fan out, per output

Signal times (typical values)
Min. impulse duration at input T 0.7 ms
Min. pause duration at input T 0.7 ms
Min. impulse duration at input R 0.4 ms
Min. duration between two reset procedures 3 ms
Max. shifting frequency 200 Hz

Delay times (typical values)
0-1 delay input T 0.4 ms
1-0 delay input T 0.4 ms
0-1 delay input S 0.4 ms
1-0 delay input S 0.4 ms
0-1 delay input A 0.22 ms
1-0 delay input A 0.22 ms
0-1 delay input R 0.2 ms
0-1 delay input PS 0.25 ms
1-0 delay input PS 0.2 ms
Delay of inputs A...H and outputs Q1...Q8 negligible
Description

The silo register R 448.2 can take in information up to 8 bit (digits) in sequence at 64 storage places. The stored information can be read out again in the sequence in which they were read in.

A 1-signal appears at the empty signalling output QL when the supply voltage is connected, after the register has been reset or after all information has been read out. The data outputs Q1 ... Q8 give, in this case, 0-signals.

The initial information applied on the inputs A ... H, will be read into the register with an 0-1 transition on the impulse input TE. This first information immediately appears at outputs Q1 ... Q8 and is indicated on the unit by means of an LED for visual verification. Information subsequently inserted occupies then the next relative positions in the register. If the register is filled with 64 informations, there appears a 1-signal on the output QV register full. With this 1-signal subsequent reading in of information is blocked.

The read of the register appears via an 0-1 transition on the impulse input TA. Thereby the data occurring on the outputs Q1 ... Q8 will be cleared. Simultaneously all inserted information stored in the register will be moved automatically back one position so that the outputs pass on the next information.

When the last information is read out there appears on output QL empty register a 1-signal and the outputs Q1 ... Q8 show 0-signals.

A 1-signal on the clearing input R clears all information in the register. The data outputs show 0-signals in this case and the empty signalling output QL a 1-signal.

The supply voltage is only connected to terminals + and 0 on the right hand side of the unit. On the left hand side the terminal normally used for 0 V is occupied by a clearing input. The + terminal is not used.

All inputs, except the data inputs, are delayed for noise suppression.

The outputs can switch inductive loads without use of flywheel diodes.

Order code for module: GH R448 0002 R1
Order code for circuit symbol transparency: GH R700 1901 R81
Order code for application: D NG 3116 80 D
Identifying colour: blue
Mechanical structure: double width
Weight: approx. 200 g

Technical data

Current consumption, register cleared
all outputs 1-signal

<table>
<thead>
<tr>
<th>Input load, per input</th>
<th>1 load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fan out, per output</td>
<td>100 loads</td>
</tr>
<tr>
<td>Delay times, clearing delay</td>
<td></td>
</tr>
<tr>
<td>read in delay</td>
<td>1 ms</td>
</tr>
<tr>
<td>read out delay</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>Data delay A ... H, Q1 ... Q8</td>
<td></td>
</tr>
<tr>
<td>read-out request tact</td>
<td>negligible</td>
</tr>
<tr>
<td>following clearing</td>
<td>1.2 ms</td>
</tr>
<tr>
<td>Signal times, minimum clearing time</td>
<td></td>
</tr>
<tr>
<td>minimum read-in time</td>
<td>2 ms</td>
</tr>
<tr>
<td>minimum read-out time</td>
<td>0.3 ms</td>
</tr>
<tr>
<td>minimum time between two read-in impulses</td>
<td>0.8 ms</td>
</tr>
<tr>
<td>minimum time between two read-out impulses</td>
<td>8 ms</td>
</tr>
<tr>
<td>Colours of LEDs, output QV</td>
<td></td>
</tr>
<tr>
<td>output QL</td>
<td>red</td>
</tr>
<tr>
<td>outputs Q1 ... Q8</td>
<td>green</td>
</tr>
</tbody>
</table>

yellow |
Decoder with LED
BCD to 1 out of 10
R 454.3

Description
The decoder R 454.3 converts a 1 decimal number in BCD code to the 1 out of 10 code.
After application of four BCD-coded signals on inputs A → D, the decoded 1-signal appears at the respective outputs Q0 → Q9.
The two equivalent inputs S block the total operation, i.e. with a 1-signal at S, all outputs show a 0-signal, independent from the information at A → D.
The signal status of the outputs are indicated by LEDs. One yellow LED each lights up in the case of a 1 signal at output Q1 to Q9 and one green LED lights up in the case of a 1 signal at output Q0.
The outputs can switch inductive loads without free running diodes.

Order code for module:
Order code for circuit symbol transparency:
Identifying colour:
Mechanical structure:
Weight:

Technical data
Current consumption
Input at A → D
at S
Fan out at Q0 → Q9
Delay times

<table>
<thead>
<tr>
<th>Decimal figure</th>
<th>inputs</th>
<th>outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
<td>B</td>
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<tr>
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<td>0</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
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</tbody>
</table>

For inputs a 1-signal appears.

x = 0- or 1-signal!
Decoder, 1 out of 10 to BCD
R 455.1

Description

The decoder R 455.1 converts a 1 decimal number in (10) code to the BCD code.

After application of a 1-signal in (10) code on the inputs A–L, the decoded signal in BCD code appears at the outputs Q1 – Q4.

The unit is passively built; has no amplifying effect and does not load the supply.

Order code for module:
Identifying colour:
Mechanical structure:
Weight:

GH R455 0001 R1

green
double width
approx. 140 g

Technical data

The input load is independent of the subsequently connected units. The output fan out is independent of the previously connected units.

The function is not delayed.

Operation table:

<table>
<thead>
<tr>
<th>Decimal figure</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>K</th>
<th>L</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
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</table>
Description

The computing module R 456.1 can add 2 BCD coded 4-bit numbers (Z3 = Z1 + Z2) or subtract them (Z3 = Z1 – Z2). Likewise, these numbers can be evaluated as smaller, larger or equal. In the operating mode „comparison” the two numbers can be applied in any arbitrary 4-bit code. The number Z1 is applied to inputs 3–6 and the number Z2 to the inputs 7–10. The result Z3 appears at the outputs 13–16. At the input AS one can choose if the numbers should be added or subtracted. An 0-signal at AS implies addition and a 1-signal subtraction.

1-signal at QÜ > implies Z1 > Z2
1-signal at QÜ < implies Z1 < Z2
0-signal at QÜ > and QÜ < implies Z1 = Z2

The input JÜ ± as well as output QÜ ± is required for decade extension in the operating mode Addition and Subtraction. The other transfer inputs or outputs are required for extension in the operating mode „Comparison”.

The input F ensures that in the operating mode „Subtraction” the inputs QA to QD complementary results occur (at Z1 < Z2).

Note:

Contact 2 must be connected to contact 11 and contact + Ue for one-decade subtraction.

The outputs can switch inductive loads without flywheel diodes.

Order code for module:
Order code for circuit symbol transparency:
Order code for application:
Identifying colour:
Mechanical structure:
Weight:
GH R456 0001 R1
GH R700 1901 R71
D NG 80849 D
green
double width
approx. 180 g

Technical data

Current consumption, all in and outputs 0-signal
five outputs 1-signal
approx. 18 mA
approx. 50 mA
Input:
inputs 17 and 18
all other inputs
2 loads
1 load
Fan out, per output
100 loads

The interface functions of the computing system and the comparator operate undelayed.