Reliability test for Subsea Power Semiconductors

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Following the demand from a new domain of application, a test setup was developed to evaluate the performance of high-power semiconductor device when exposed to a dielectric liquid and high pressure. The specific test conditions were established to emulate the conditions inside a tank place in a deep-sea environment. Those conditions can be characterized by two key parameters: the pressure and the chosen dielectric/thermal liquid. The power semiconductor device is to be tested at high and low temperature to simulate operation under maximum load as well as when turned off, respectively. The reliability tests outlined here serve to support the development and the validation of Subsea technology for semiconductors power modules.

1.New application new challenges

The oil and gas industries have recently promoted the vision of a subsea factory, as the preferred way to enable cost-effective field development of more dispersed, deeper, smaller, and possibly arctic oil and gas fields. Today, power electronic devices for driving large compressor and pump electrical loads are located at atmospheric pressures either on-shore or on a platform with long, variable-frequency step-out cables feeding the electrical loads. Removing the station and the cables has great cost- and environmental advantages. In support of this vision, a power conversion unit (or also called Drive), which is suitable for operation in deep-sea environment has to be developed.

In this study the authors consider the approach where the equipment is passively pressurized to the hydrostatic pressure level of the ambient sea water. Since the pressure increases by 1 bar each 10 m, the typical subsea installation will be submitted to a pressure between 100 to 300 bar. This is achieved by filling the subsea tank with a dielectric liquid of negligible compressibility. Similar as in power transformers, the tank walls are no built to sustain special pressure differences. Consequently, each component of the converter, including the semiconductor power module has to be compatible with the dielectric liquid and this without any reduction of its electrical capabilities. Those components also have to be pressure tolerant in order to guarantee the robustness of the system. In the meantime, the accessibility of the drive is nearly non-existent resulting in the demand for unprecedented reliability. To fulfil those added requirements new power modules as well as new testing capabilities have to be developed.

1.1. Subsea environment

As for many of the components in the subsea power conversion unit, some adaptations from existing component products are necessary to create a component “fit-for-purpose” for the subsea tank conditions. The adaptations are guided by the need to be chemically compatible with the dielectric liquid as well as to withstand the pressure environment under full operating electrical load or storage conditions and this for the intended design lifetime, typically 30 years. In general, the two environmental conditions at subsea are referred to as “Pressure and Liquid tolerance” (PLT). In addition to the PLT requirements, the conventional specification of the components and subassemblies, such as electrical, mechanical, thermal, or functional aspects have to also be fulfilled.

1.1.1 Pressure:

A typical design pressure for subsea equipment located down to 3000 m depth is 345 bar according to API 17F. However, the exact pressure at which a system will be exposed is project dependent and can be located anywhere between 1 to 300 bar. In any application this pressure is held constant by the pressure compensator. It is therefore assumed that if the system capability can be proven at 1 bar as well as at 300 bar, any pressure in between will also be managed accordingly.

1.1.2 Tank liquid:

In developing subsea power modules, one should consider material compatibility of semiconductors submersed in dielectric liquid, especially regarding long term effects like degradation of the oil (e.g. by water accumulation or partial discharges) and swelling of polymers in the oil. Altering dielectric properties of material protecting the semiconductors alters the electrical fields present on the chip surface between collector and emitter and also the general insulation properties of the drive. This is one of the important factors to be considered in the design of the subsea semiconductor modules.

2. Test philosophy

2.1. Motivation

The semiconductor package for subsea is a further improvement based on Hitachi ABB Power Grids' most reliable semiconductor module, from StakPak family, generally used in power system applications. While the functional electrical, thermal and mechanical demands on the components are quite similar to the conditions, when the drive operates in air at 1 bar “top-side”, the operating environment for these components are vastly different. The primary difference compared to “top-side” is the application of the hydrostatic load due to the pressure. This load is superimposed on the loads resulting from thermal-elastic stresses coming from the temperature gradients inside the component, or pre-stresses generated during module. In a homogenous isotropic material, the hydrostatic load leads generally to a harmless compression. However, every interface, or anisotropic material, will see various additional mechanical stresses despite the fact that the hydrostatic pressure is uniform. In addition to the pressure, the semiconductor needs to be protected from the natural convection of the dielectric liquid, which may have constituents adversely affecting the semiconductor's passivation layer. Degradation of the passivation layer would lead to an increase of leakage current, to electrical flash-over on the chip termination, or other blocking capability failure.

2.1.1 High Temperature Reverse Bias

The High Temperature Reverse Bias (HTRB) test is a standard reliability test designed to check the time stability of the main blocking junction under reverse bias and high temperature. conditions. In this test the chip passivation is stressed most strongly when the IGBT is in blocking mode at rated voltage, thus handling the full voltage drop over the passivation while only a leakage current is conducted in the chip. In this study, in addition to the standard conditions, the HTRB test has to be conducted under oil and high pressure. For HTRB tests, the vessel is heated externally to a few degrees below 125 °C. The electrical blocking losses of the semiconductor provide the remaining heat source to maintain the Device Under Test (DUT) at 125 °C. Here, extra care must be taken as to not exceed the maximum temperature, as else a thermal runaway and failure could occur.

2.1.2 Low Temperature Reverse Bias

The Low Temperature Reverse Bias (LTRB) test is designed to check the robustness of the power devices under low temperature conditions and pressurized oil, emulating storage mode when the converter is turned off. This test is specific to subsea application and even without pressure, this test is normally not performed on standard power module. For this test a thermal runaway due to the high leakage current under blocking voltage is not expected. However, the maximal blocking capability and the mechanical strength of the materials is of concern. Applying the high hydrostatic pressure to polymers affected by cold embrittlement may generate cracks in one of the passivation layers which will lead to a blocking failure of the device under test. Therefore, the time stability of the device is verified by applying a high reverse bias and monitoring the generated leakage current.

2.2. Pressure vessel

The Subsea laboratory is built with a modular concept providing independent testing cells. Each testing cell may be equipped with a pressure vessel capable of supporting more than 150% excess test pressure, providing heating up to 150°C and cooling down to 0°C as well as some electrical feedthrough with capability up to 3.5kV. The electrical circuit present in one cell is normally composed of a high voltage DC source and a high voltage resistor used to dissipate the electrical power and limit the current in case the DUT failed into a short circuit. A schematic of the electrical test circuit is presented in Figure 3. Also visible in this electrical schema is a safety switch installed on the door of the cell.

Inside the pressure vessels there are sample holders which are connected to the outside cell electrical circuit with the help of appropriate feedthroughs. The pressure vessel, visible in Figure 2 is placed in a cabinet made with a 10 mm Polycarbonate combined to a 3 mm thick stainless-steel walls to protect the environment from sudden pressure release or hot oil spraying in case of leakage. The pressure vessel consists of a high-pressure tube, one top cover, one bottom cover, tension rods, electrical penetrators, vessel support structure, thermal insulation, valves, safety equipment and manometer accessories. Both covers and the high-pressure tube are engineered for 10000 full pressure cycles. One full pressure cycle is defined by pressurization from atmospheric pressure to the maximum vessel operating pressure.

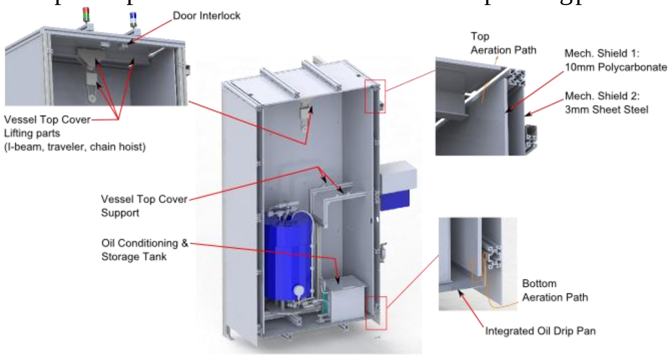

Figure 1:Drawings of the cabinet with the pressure vessel in blue showing the safety features, electrical safety circuit allow for voltage application only in case of closed cabinets.

Figure 2: overview of closed pressure vessel (10 l)

The main challenge of the HTRB test is visible on the oil temperature and pressure curves presented in Figure 5. If the vessel is filled with degassed dielectric liquid and all valves are closed, a change in the temperature will also generate a change of the pressure typically 10bar/°C. If both parameters are not kept in good equilibrium, this could result in overstressing the modules and therefore a non-test related module failure. In order to account for the pressure and temperature rise due to power heat dissipation in long-term aging experiments, this behavior was characterized.

As for the LTRB test the main challenge sit on a vicious cycle affecting the cooling system. The cooling system efficiency is reduced due to the accumulation of ice on the liquid to air heat exchanger. The ice formation is driven by condensation and solidification of the moisture normally present in air. The lower cooling performance due to the ice formation is coupled back to a higher need in cooling ability resulting in an amplified growth of the ice layer. This can result in an increase of temperature and due to this also a pressure increasement inside the vessel. This vicious cycle was broken, and the ice accumulation was greatly reduced by minimizing the air exchange between the laboratory room and the testing cabinet where the heat exchanger is located.

2.3 Electrical circuit diagram for test set up

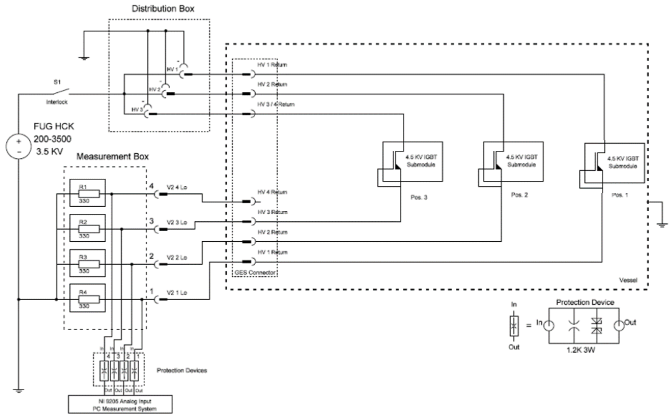

Figure 3: Electrical diagram for testing of IGBT chips (here for three StakPak submodules)

Figure 3 shows the electric circuit diagram for three independently powered DUT. All chips are switched in parallel and the gate-emitter path of each chip is electrically shorted. The collector-emitter blocking voltage is provided by the FUG-HCK power sources. Resistors enable measurement of the DUT leakage current. In the eventuality where one of the chips will fail into a short circuit, the current and voltage input must be constrained. This current limitation is needed to prevent excessive chip damages and excessive heating of the vessel interior. In addition, in case of DUT failure, the FUG must shut down, removing all the cell voltages and the measuring system must be protected from the high voltage which is done with the protection devices. Due to the big leakage current difference between HTRB and LTRB test, the measurement accuracy by the LTRB test, is not sufficient due to the resistor value. Hence, the leakage current values by the LTRB test are not correct.
As seen in figure 4, two or three devices were stacked with or without the help of heat sinks depending on the temperature condition for heat dissipation. This testing assembly was then fixed to the vessel lid. Thermocouples monitoring the temperature at different positions were also assembled. The vessel was then closed, heated up to 120°C and then pressurized.

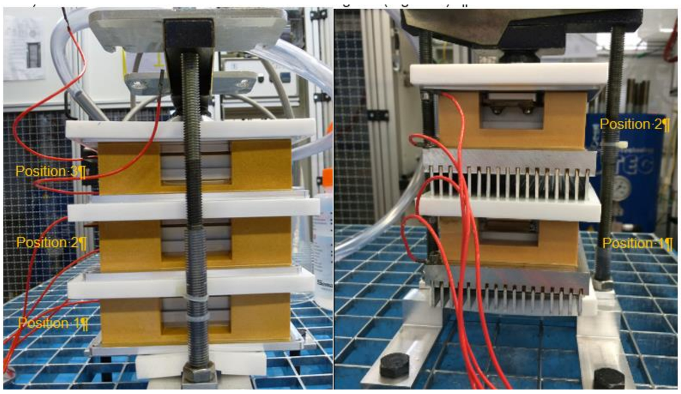

Figure 4: StakPak submodules assembly for 3 submodules for LTRB (left side) and for two submodules HTRB (right side)

3. Test results

In order to apply the collector to emitter voltage, the gate to emitter contacts from all IGBT's are electrically shorted. During the test, the following parameters are monitored: collector to emitter voltage ($V_{(BR)CE}$, the leakage current I_{CE}, the gate to emitter voltage V_{GE} as well as the gate to emitter leakage current I_{GE}. Two adapted Hitachi ABB Power Grids StakPak 4.5kV IGBT submodules, with integrated antiparallel diode, have been tested. The test conditions were the following:

- 4.5kV StakPaks: >3400V ±3%, VGE = 0 V (shorted)
- Time: >1000 h
- oil T° 120±1°C or 5°C ±1°C
- P = > 345 bar

The criteria for a successful test were set to no significant increase of I_{CE} or I_{GE} during the test (change smaller than a factor of 2). After testing, the DUTs are cooled down and both leakage currents are measured at room temperature. Like for standard HTRB test, the DUT functionality is controlled after the test. Note that in the application, only the DC-link voltage of about 50 – 60 % from the maximum rated blocking voltage is applied on the semiconductor. Short voltage peaks, higher than this 60% are expected but not in a continuous mode. This test at increased voltage is a good indicator of device quality and reliability during operation.

Typical measurement profiles are shown in Figure 5. From Figure 5, a slight leakage current overshoot can be observed in the beginning of the experiment. The decline of leakage current caused the oil temperature to decrease as well. Stable conditions were reached at around 100 h by adjusting the heater temperature accordingly. The vertical peak visible at around 330 h of testing comes from a communication interruption between the laboratory computer and the test setup. This had no influence in the process of the experiment. These tests were finished successfully, and the samples met the criteria of acceptance in the post-stress reliability test.

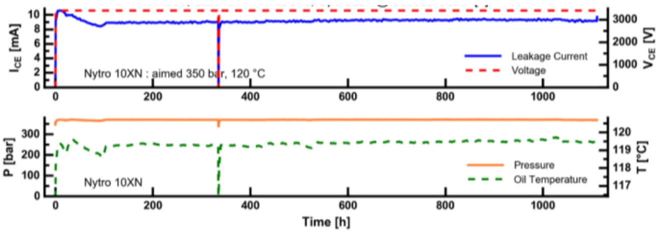

Figure 5: The HTRB measurement shows in the first graph the applied voltage and the measured leakage current vs. time, where in the second plot the oil temperature and the pressure are indicated as well, respectively

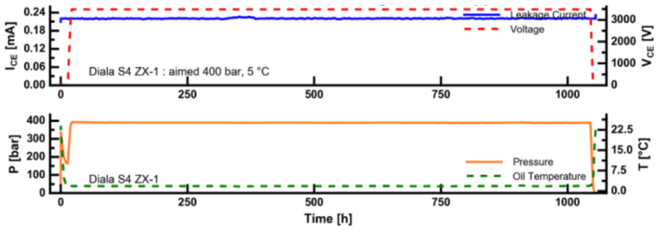

Figure 6: The LTRB measurement shows in the first graph the applied voltage and the measured leakage current (offset on Ice values) vs. time, where in the second plot the oil temperature and the pressure are indicated as well, respectively

4. Conclusion

This paper outlines the test philosophy for qualifying semiconductor power modules for Subsea application meaning being pressure and liquid tolerant. Three challenges connected with the test setup were discovered such as the power dissipation at high temperature, the influence of the temperature variation on the pressure as well as the reduced cooling capability due to ice formation. The challenges were successfully overcome, and meaningful results were obtained to confirm the pressure liquid tolerant specification.

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