The Next Generation Bimode Insulated Gate Transistors Based on Enhanced Trench Technology

The combined advantages of the low loss Enhanced Trench cell concept and BIGT chip integration sets a new milestone for delivering higher output power for the next generation BIGT power modules.

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High voltage IGBTs have undergone major breakthroughs in the past two decades with respect to their power handling capabilities. Nowadays the next step to enable higher output power capability for high voltage devices is following two different development paths. The first is an IGBT/Diode integration concept by combining both the IGBT and diode modes of operation in a single chip and hence eliminating the need for a separate antiparallel diode. This step was realized with the introduction of the high voltage and hard switched Reverse Conducting RC-IGBT (or the Bimode Insulated Gate Transistor or BIGT). The BIGT was based on the Enhanced Planar (EP) MOS cell platform, called SPT$^+$. The second development path was achieved with the introduction of an Enhanced Trench (ET) MOS cell or TSPT$^+$ to provide further plasma enhancement (i.e. losses reductions) combined with improved controllability.

Both the BIGT and ET-IGBT device concepts provided separately an additional increase in the output power compared to state of the art HiPak 2 modules with current ratings reaching up to approximately 1800A/3300V and 900A/6500V. The preferred choice of either approach depends heavily on the application in terms of topology, switching frequency, gate drive / control adaptations, and diode loading / surge current requirements. Figure (1) shows the nominal current carrying capability increase with each improved IGBT generation for the reference HiPak 2 modules rated at 3300V, 4500V and 6500V.

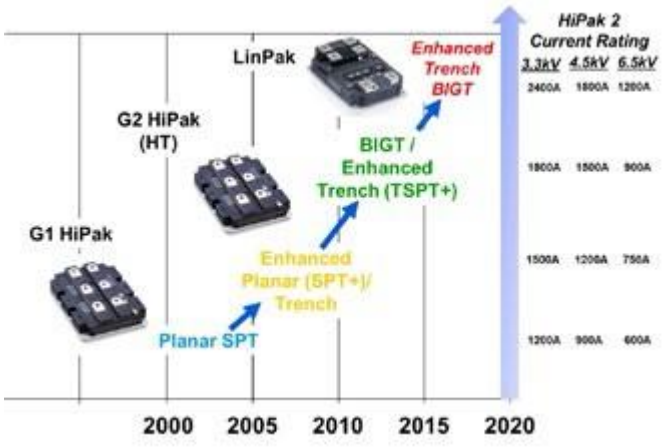

Figure 1: High voltage standard HiPak 2 module (140 x 190 mm) current ratings for 3300V, 4500V and 6500V with different generations of IGBT technologies.

In this article, we demonstrate how the next step in device evolu- tion for targeting even higher current ratings can be achieved by combining the ET-IGBT MOS cell and the BIGT integration structure. The reported results offer the possibility to reach another significant milestone where the current ratings can be doubled to 2400A/3300V and 1200A/6500V when compared to the first IGBT module products at these voltage ratings.

THE ENHANCED TRENCH ET-BIGT

The high power performance and advantages of the BIGT concept based on the EP MOS cell technology have been previously reported for different voltage ratings ranging between 3300V and 6500V. Also recently, lower losses and higher current ratings were achieved with an IGBT, which is based on the ET MOS cell technology. Therefore, it is natural to follow on the next step and provide the combined advantages of both design concepts by introducing a BIGT based on the ET MOS cell design.

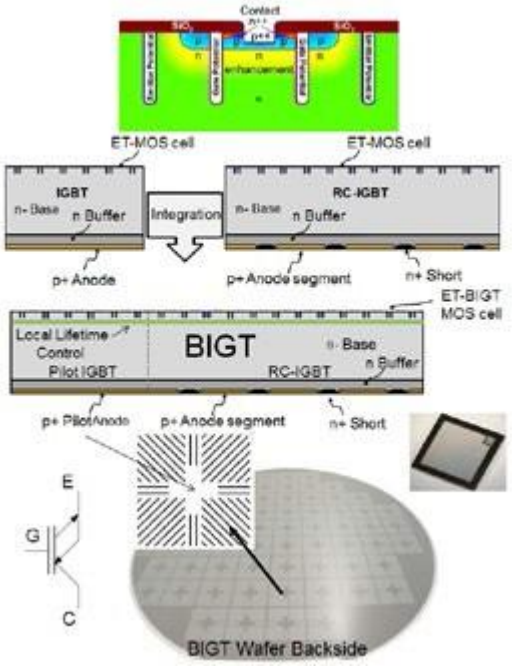

Figure 2: The Enhanced Trench ET-BIGT basic design concept including the wafer backside design.

The ET-BIGT structure shown in Figure (2) was designed by employing the previously reported BIGT backside architecture with respect to the p^+ pilot IGBT region and the radial layout p^+/n^+ shorting design for providing a snap-back free on-state characteristics.
The main focus of the ET-BIGT was to optimize the ET MOS cell for providing good diode performance. For the targeted performance gain, it is critical that the diode mode on-state losses of the BIGT remain relatively low even under positive gate biasing conditions for ease of control and for maintaining good surge current capability. In principle, trench cell concepts in an RC-IGBT provide a stronger gate shorting effect since a planar cell design has a lateral gate and can still provide relatively high diode hole injection at the centre of the p-well under the contact. Hence, the introduction of a diode p-type anode pilot region in the third dimension is necessary to obtain low conduction losses even under positive gate biasing. Introducing the diode pilot region in this manner does not adversely affect the ET cell plasma enhancement for lower losses as far as the dimensions between the repetitive pilot diode regions are kept large.

For reducing the diode mode reverse recovery losses, the well proven Local p-well Lifetime (LpL) control region in the emitter p-well is also included for lowering the injection efficiency in diode mode without adversely affecting the excess carriers in transistor mode for low conduction losses. Furthermore, a uniform local lifetime control layer is introduced across the whole device at a depth beyond the trench bottom regions as shown in Figure (2). The uniform local lifetime dose is varied to adjust the recovery losses to the desired target as discussed in the following section.

THE 3300V ET-BIGT ELECTRICAL PERFORMANCE

The first 3300V/62.5 A ET-BIGT prototype chips were manufactured and tested. To demonstrate the impact of the different lifetime control steps, Figure (3) shows the reverse recovery current waveforms without any lifetime control, with LpL only, and with two doses for the uniform lifetime control layer (A implant dose < B implant dose).

To assess the full impact of the lifetime control, static and dynamic electrical characterization was carried out on the new ET-BIGT chips and compared to reference devices including EP-IGBT, EP-BIGT and ET-IGBT having a similar active area of approximately 1 cm2. The different chip designs were dynamically tested under nominal current and voltage conditions at 150°C, RGon = RGoff = 33 ohm, Cge = 10nF and a stray inductance of 2400 nH. The losses technology curves in both transistor and diode modes are shown in Figures (4) and (5) respectively. Figure (4) shows that the ET-BIGT uniform lifetime control results in an increase in the Vce values. Figure (5) shows that ET-BIGT design (B) matches the diode losses of the EP-BIGT.

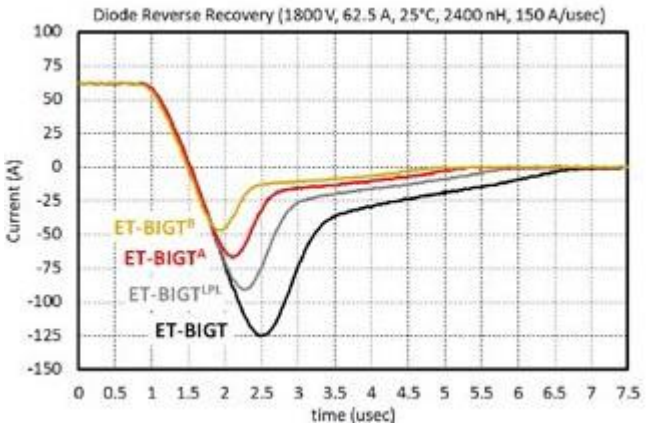

Figure 3: ET-BIGT Diode mode reverse recovery current waveforms at 25°C for different lifetime control steps

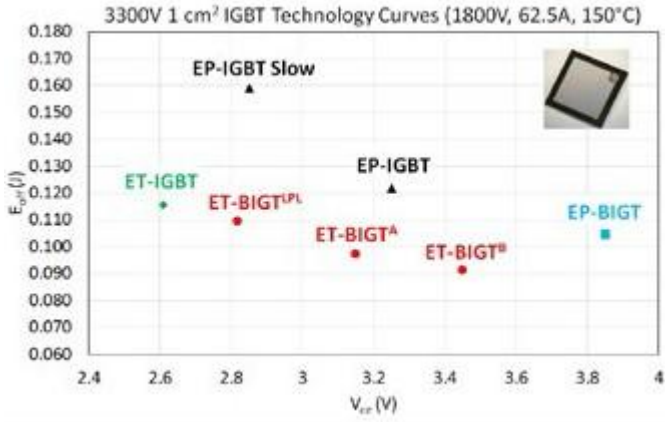

Figure 4 : 3300V Transistor mode technology curves (V_{ce} vs. E_{off})

It is important to note that the uniform local lifetime dose of design (B) is close to half of that of the EP-BIGT due to the lower injection efficiency of the trench cell when compared to the planar cell. While the higher EP-BIGT conduction losses results in a chip current rating of approximately 50 A/cm^2, the ET-BIGT can be rated at 62.5 A/cm^2 (similar to EP-IGBT). This can then provide the increased module current ratings as discussed previously.

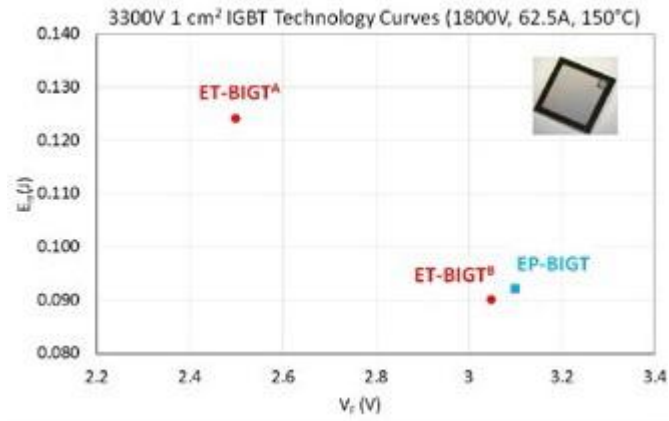

Figure 5 : 3300V Diode mode technology curves (V_F vs. E_{rr})

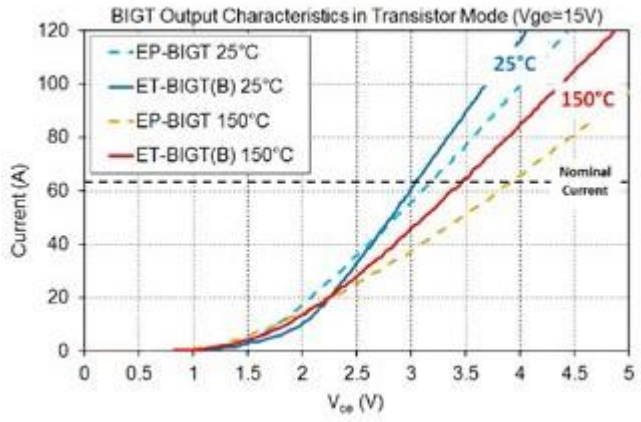

Figure 6: 3300V Transistor mode on-state curves at 25°C and 150°C

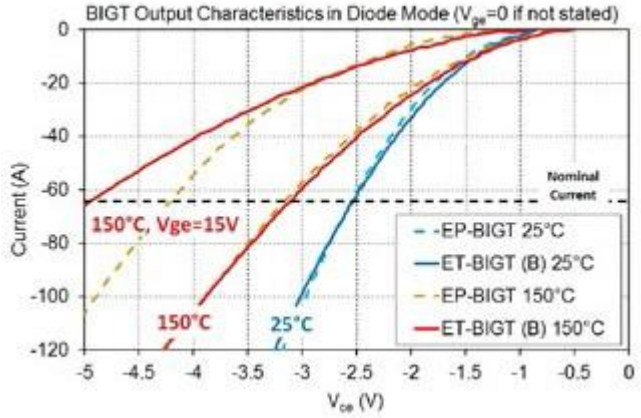

Figure 7: 3300V Diode mode on-state curves at 25°C and 150°C

Figures (6) and (7) show the EP-BIGT and ET-BIGT design (B) static conduction curves in both IGBT and diode modes respectively. The diode mode on-state are recorded with an applied gate voltage of 0V and 15V. The impact of the trench cell is clearly visible having a higher VF with a positive gate emitter bias voltage.

The ET-BIGT design (B) chips were then employed in a HiPak 1 (130mm x 140mm) to demonstrate the chip capability at module level. Each module contained 24 chips and was tested with nominal current (1600A) and voltage (1800V) conditions at 150°C, $R_{Gon} = R_{Goff} =$ 3.3 Ohm, C_{ge} = 330 nF and a stray inductance of 100 nH. The turn-off waveforms are shown in Figure (8), while in Figure (9) the reverse recovery performance is demonstrated. The dynamic losses were recorded having E_{off}= 2.4 J, E_{on}= 3 J, and E_{rec}= 1.9 J.

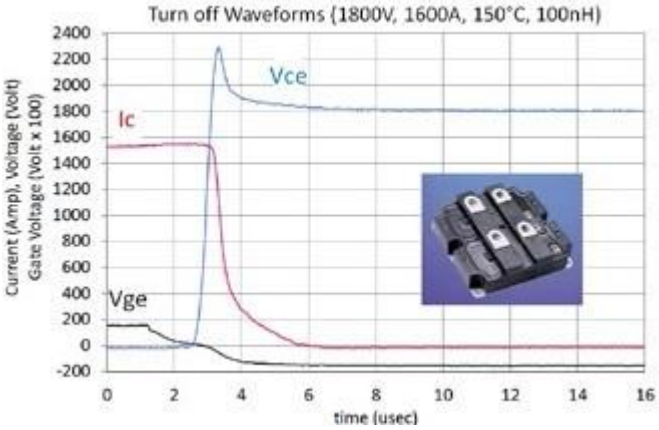

Figure 8: 3300V/1600A HiPak 1 ET-BIGT Transistor mode turn-off waveforms at 150°C

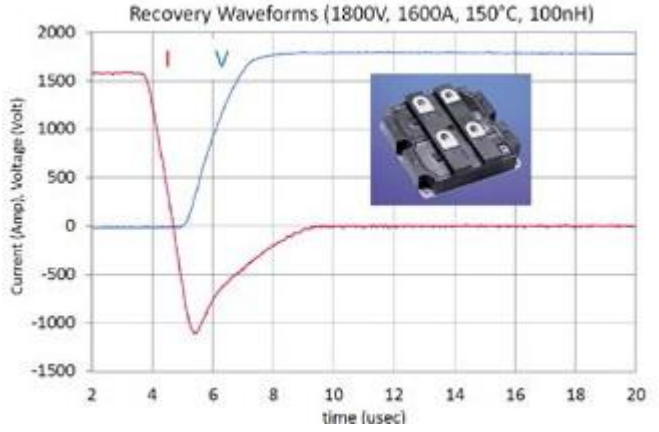

Figure 9: 3300V/1600A HiPak 1 ET-BIGT Diode mode reverse recovery waveforms at 150°C

After nearly two decades of HV-IGBT developments, the ET-BIGT chip platform has the potential to enable a new milestone by reaching double the output current carrying capability of HV-IGBT modules when compared to first generation devices.