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ABB Protective Relay School Webinar Series
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ABB Protective Relay School Webinar Series

Bus Protection Fundamentals
Jack Chang, RTM, Western CA
July 09, 2015

Power and productivity
for a better world™

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Presenter

Jack Chang

Jack Chang is the regional technical manager for ABB Inc. in the Substation Automation Products BU serving customers in western Canada and northern regions. He provides engineering, commissioning and troubleshooting support to customers applying ABB's high-voltage protective and automation devices. Prior to joining ABB, Jack worked as a substation P&C project engineer in two specialized consulting firms (now ABB and Quanta Services, respectively) and also as an engineering consultant to a public owned utility in their transmission expansion and upgrade projects. Jack is a registered professional engineer in the province of Alberta, Canada.

Learning objectives

- Types of bus configurations

- Current transformer characteristics and their effect on bus protection

- Types of bus protection schemes

- Modern Numerical Bus Protection Features

- Questions: jack.j.chang@ca.abb.com, 403-923-4028

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Why bus protection?

- Different configuration and design

- Usually very robust, high current faults

- Need to clear quickly

- A Delayed bus trip leads to:

  - Network instability pole slip of nearby generators

  - Possible system collapse

  - Bigger fault related damages & risk to human life or injury

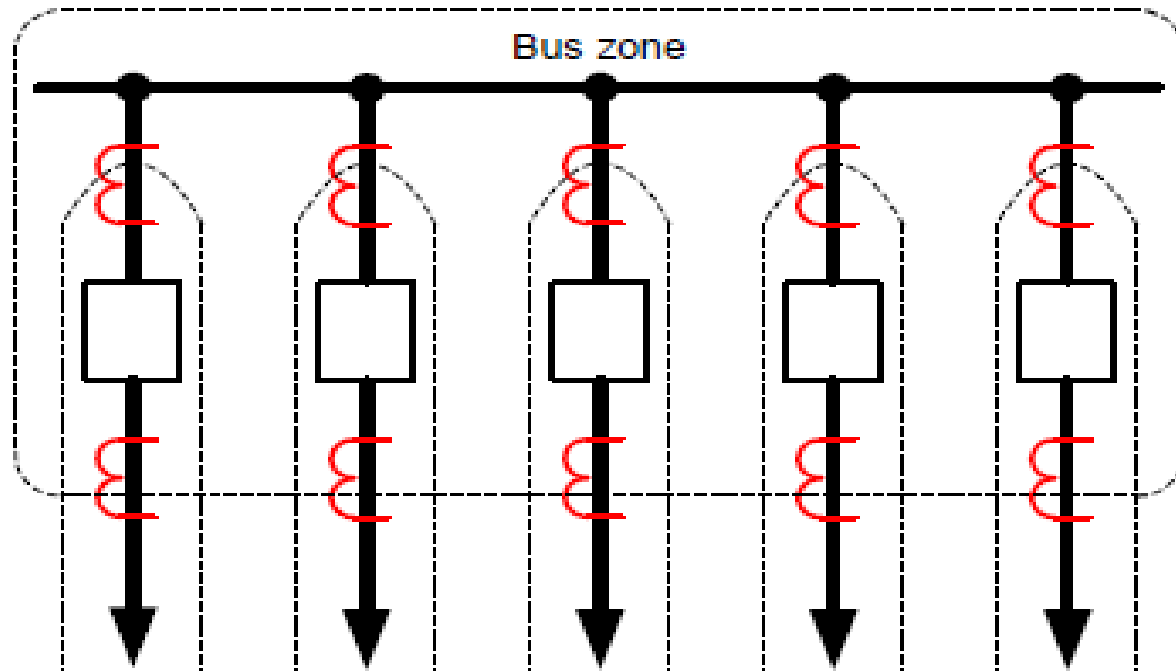 - Many bus faults caused during maintenance (eg. Arc flash)

Bus fault protection

- Easy to detect because of robust nature

- Easy to protect for internal faults (87B)

- Summation of currents not equal to zero for internal fault

- External faults can cause current transformer saturation which results in unwanted differential currents

- Infrequent, but must be cleared with high speed

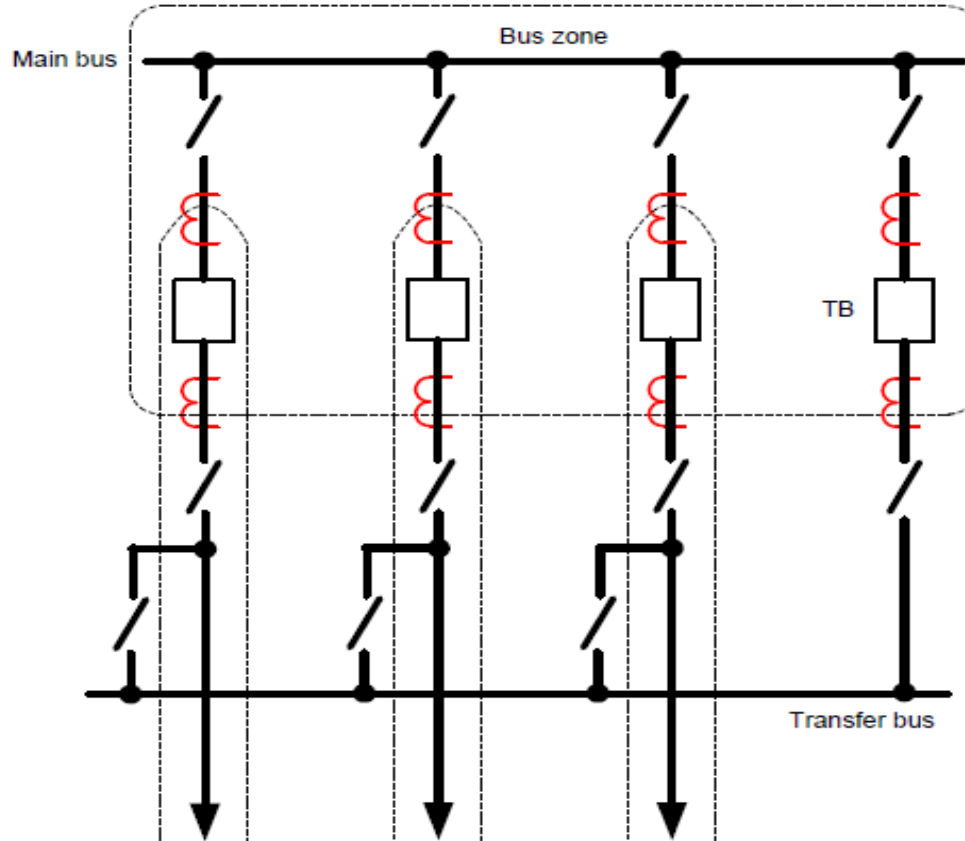 - Substation is well shielded

  - Protected environment

Bus configurations

- Single bus *

- Main and transfer bus

- Double bus, single breaker *

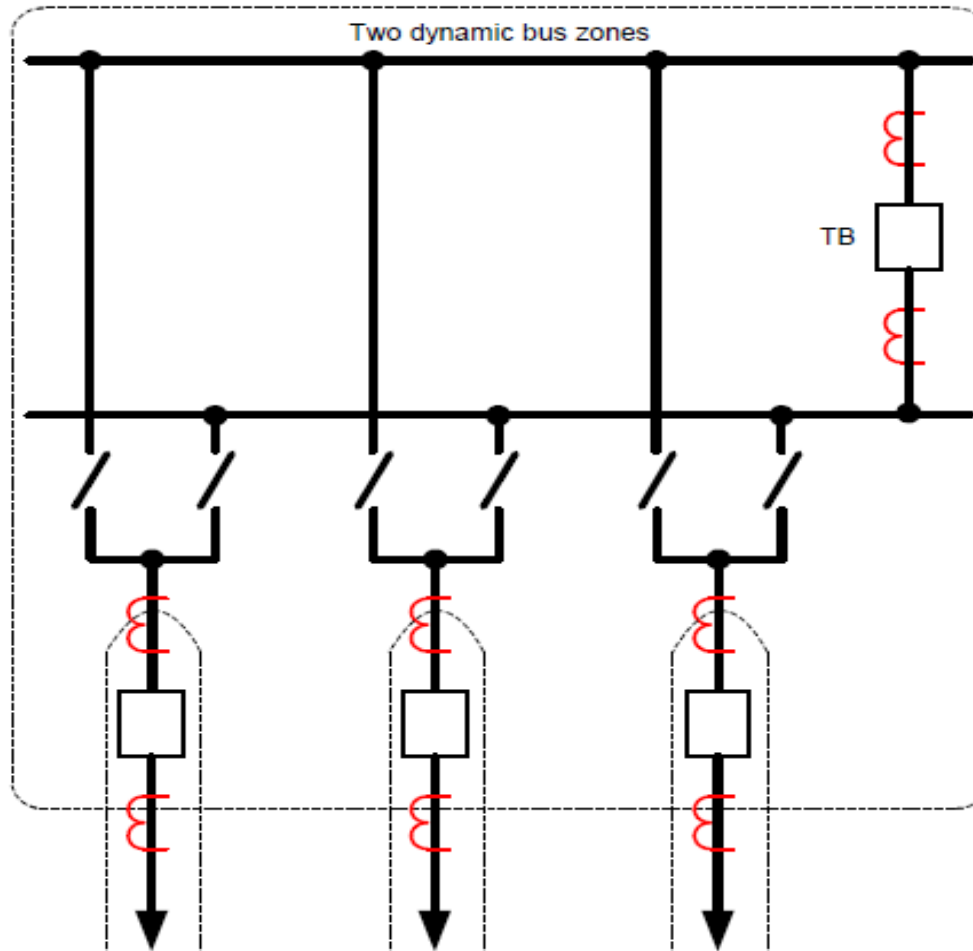- Double bus, double breaker

- Breaker and a half *
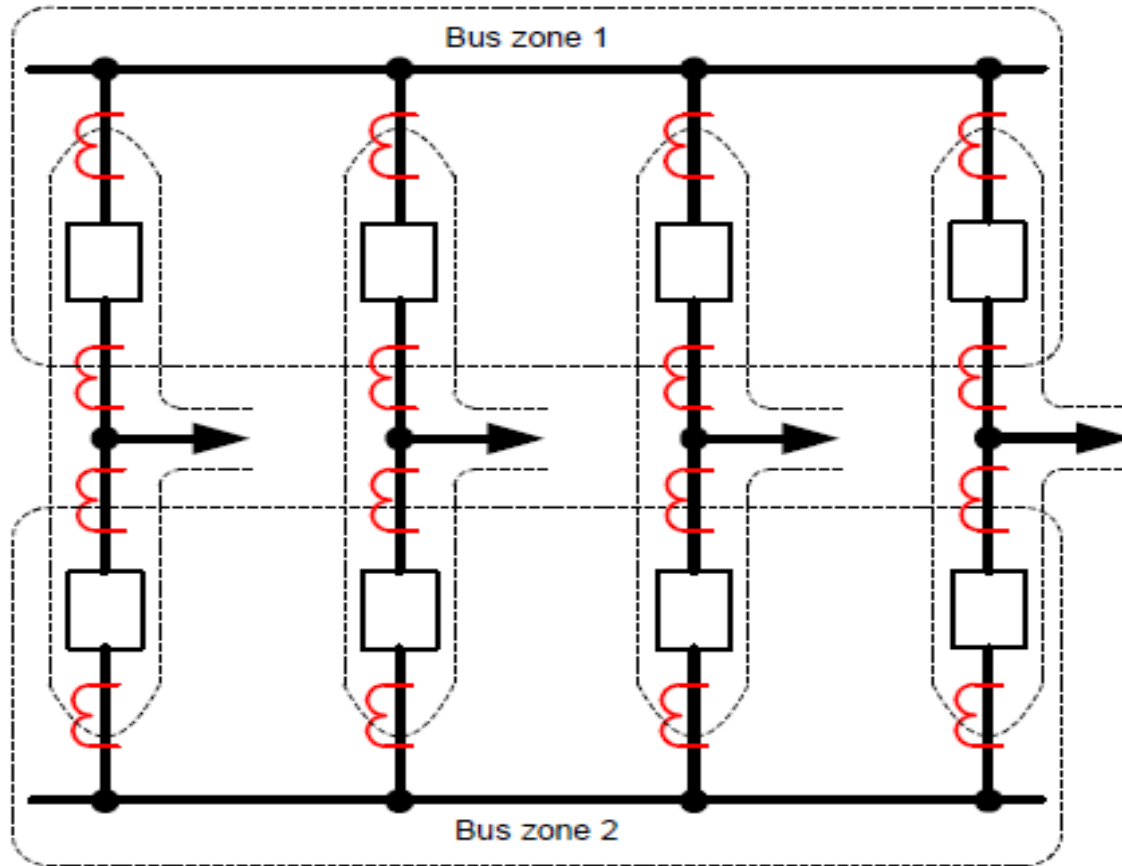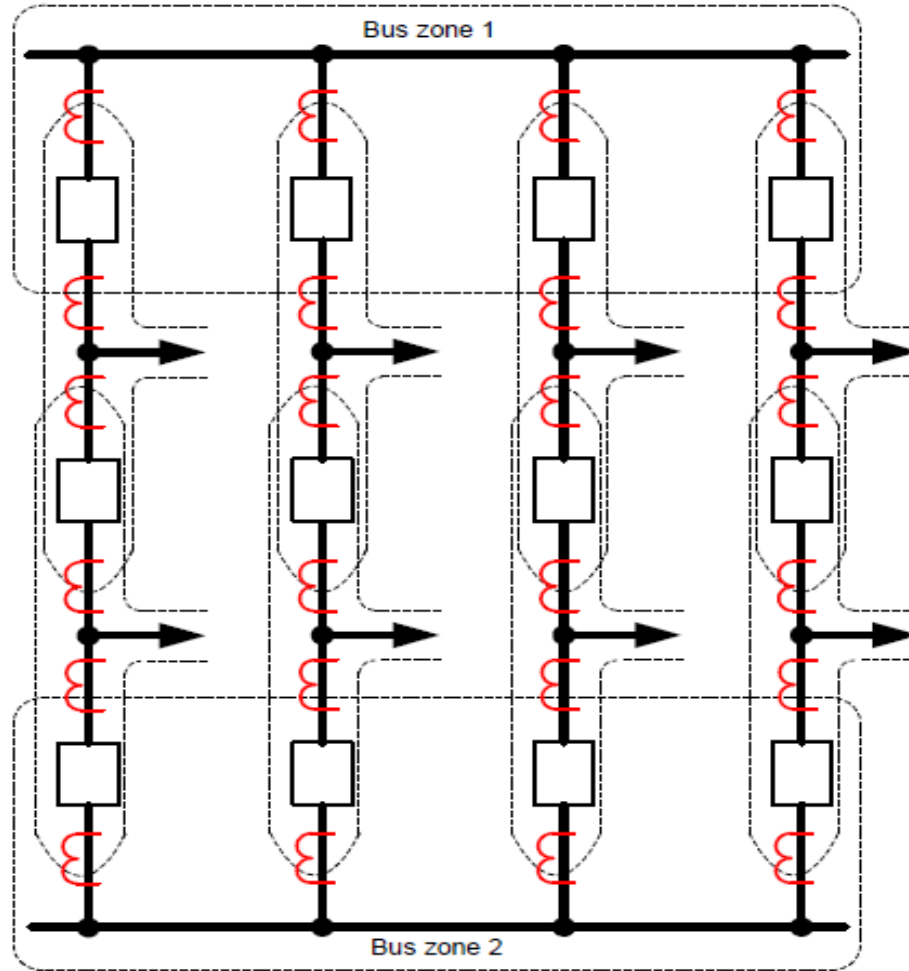
- Ring bus *

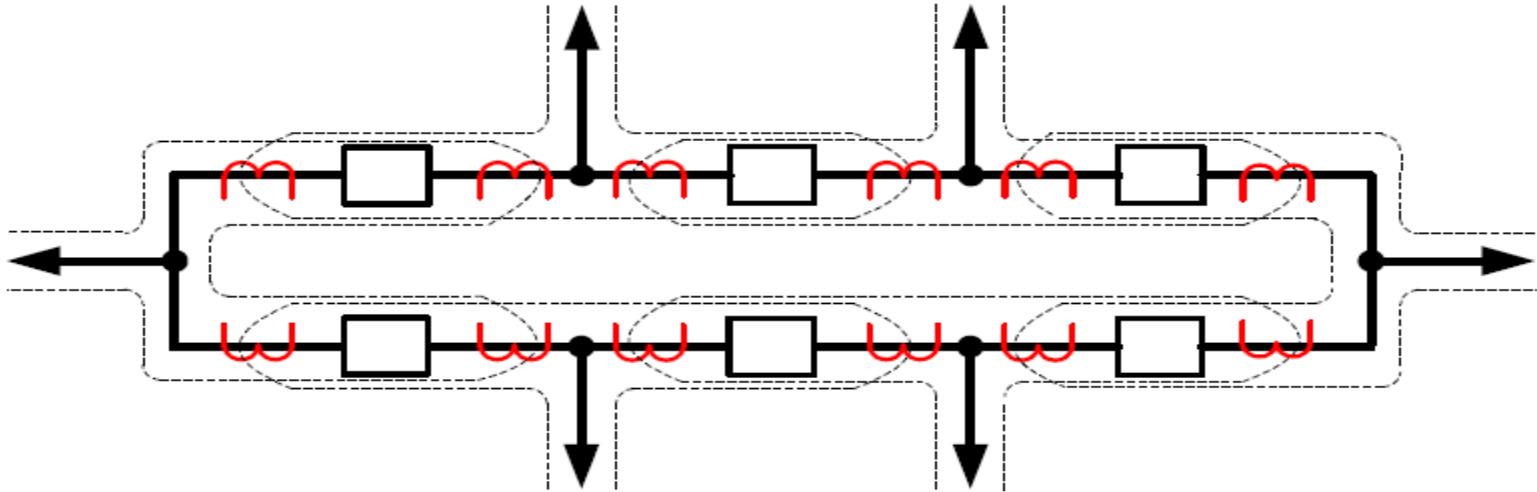# Single bus

Main and transfer bus

Double bus single breaker

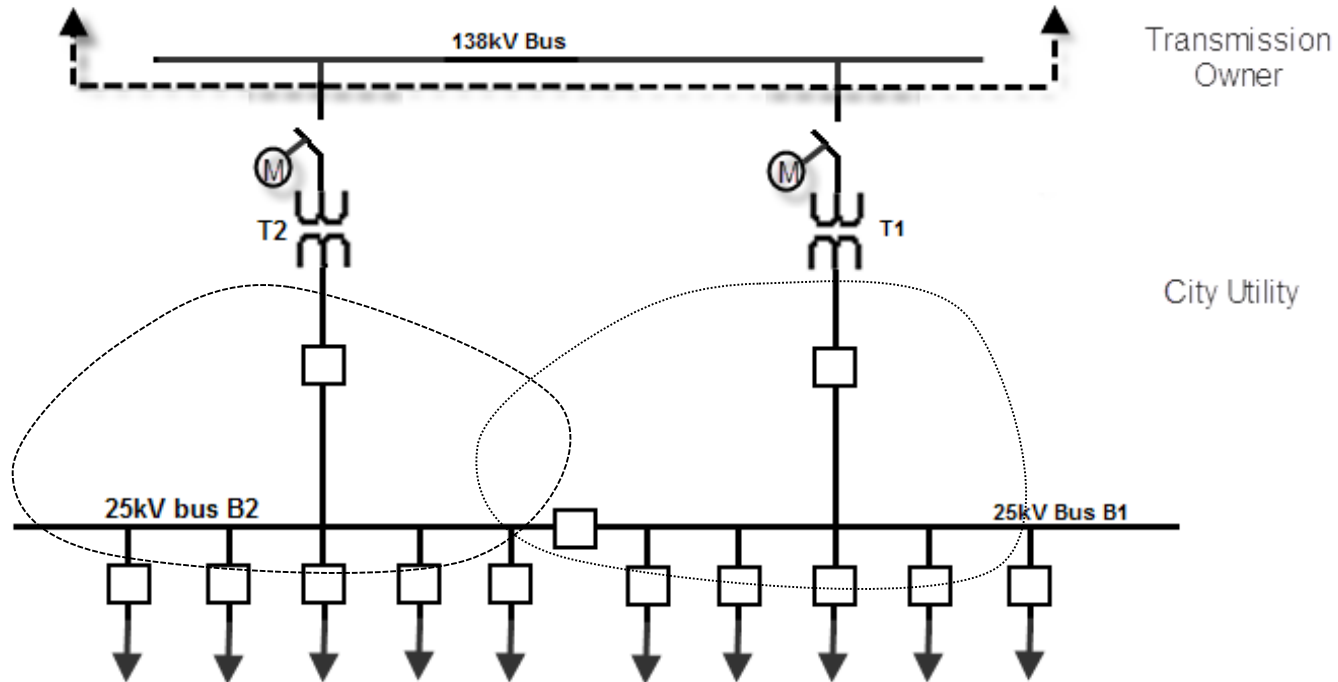# Double bus, double breaker

Bus zone 1

Bus zone 2
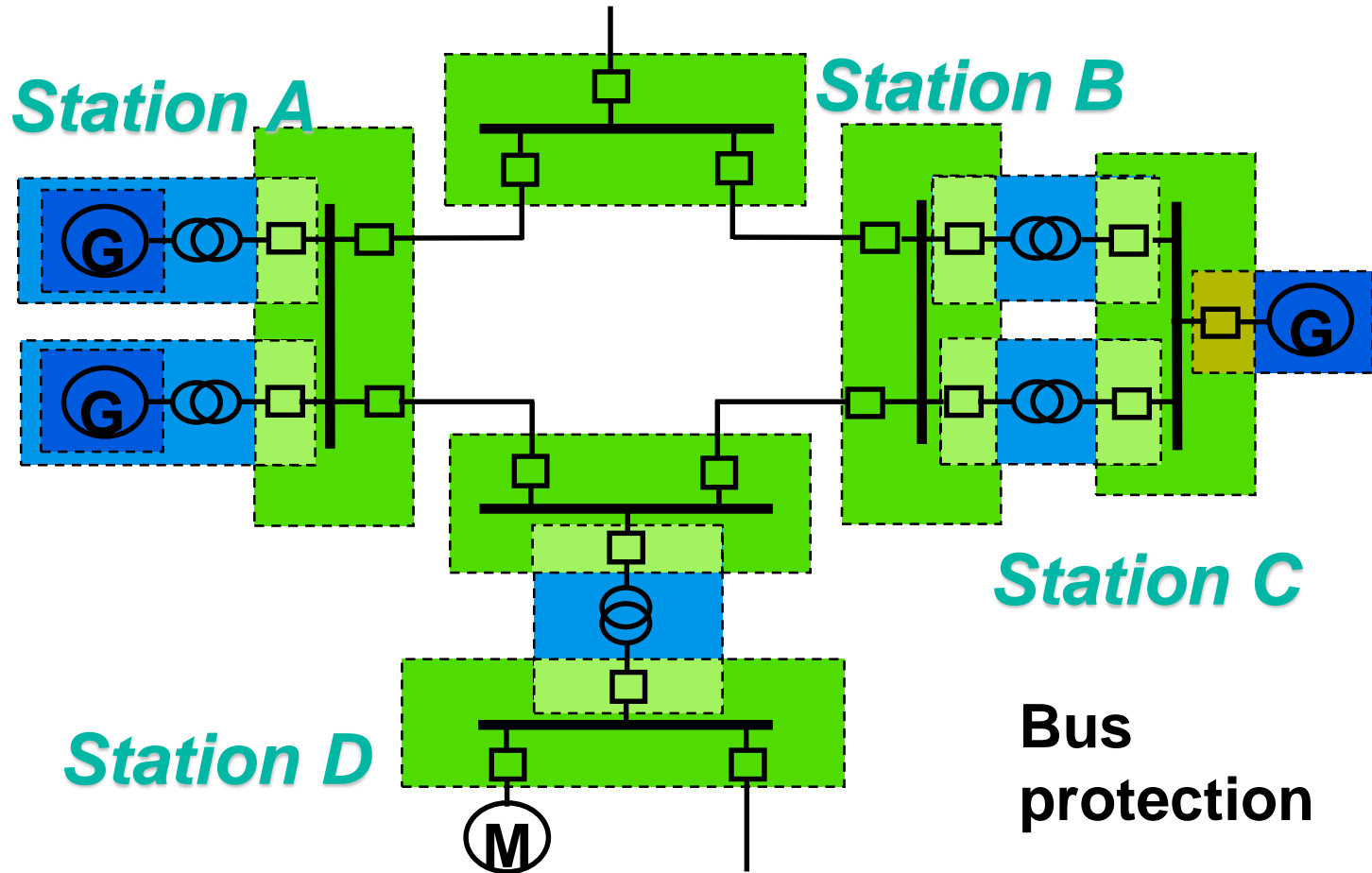
Breaker and one half

Ring bus

Main-Tie-Main
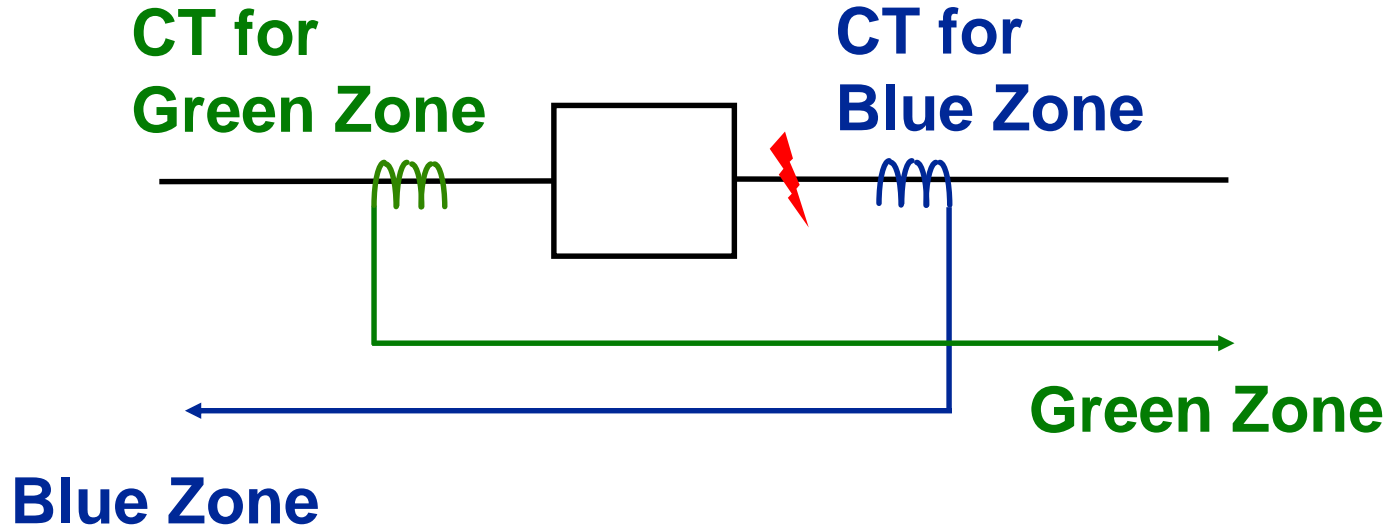
Some issues

- Availability of overlapping protection zones (CTs)

- Blind or end zone protection

- Will loads or sources be switched from one bus to the other

- Current transformer switching from one zone to another

- Open circuit current transformers

- CT Saturation

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Zones of protection

Station A

Station B

Station C

Station D

Bus protection

Zones of protection

CT for Green Zone

CT for Blue Zone

Green Zone

Blue Zone

Dead tank breaker, two CTs

Zones of protection

CT for Green Zone

CT for Blue Zone

Green Zone

Blue Zone
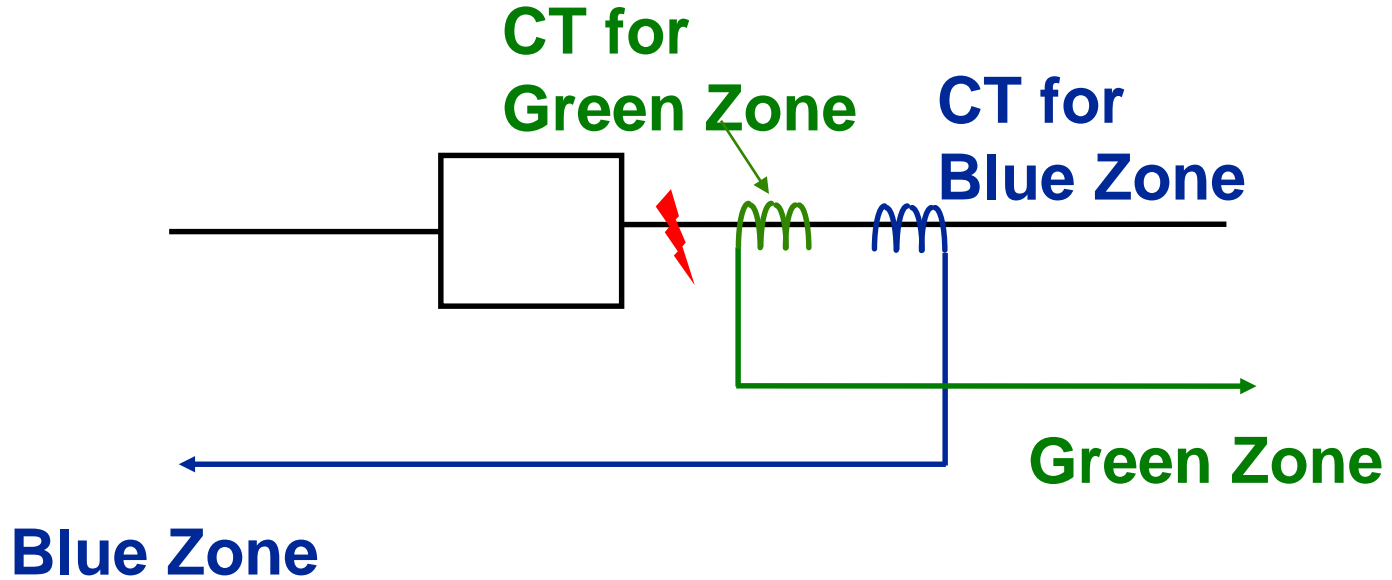
Live tank breaker, single CT

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Current transformer
Ratings of concern for bus protection

- Ratio: 200/5, 1200/5, …500/1

- Burden capability: VA burden

- Accuracy Class: C800, K200, T400

- Knee point, saturation voltage (can be derived from chart in C class CTs)

- CT availability

- IEEE Standard C57.13-1993 (R2003), IEEE Standard Requirements for Instrument Transformers

- IEEE Standard C37.110-1996, IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes

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ANSI current transformer accuracy class

- Example 1200/5 C800

- This current transformer will deliver 800 volts on its secondary when it is connected to a standard burden and 20 times rated current is flowing in the primary winding without exceeding 10% ratio error.
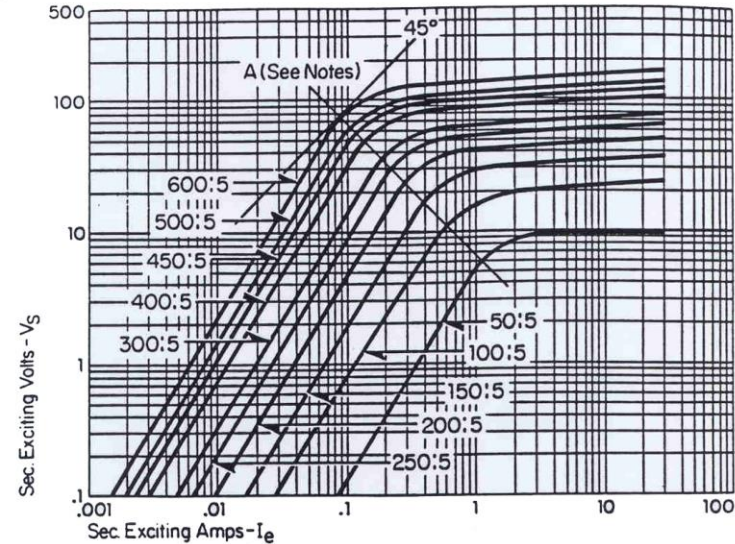
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ANSI accuracy class
Standard chart for class C current transformers
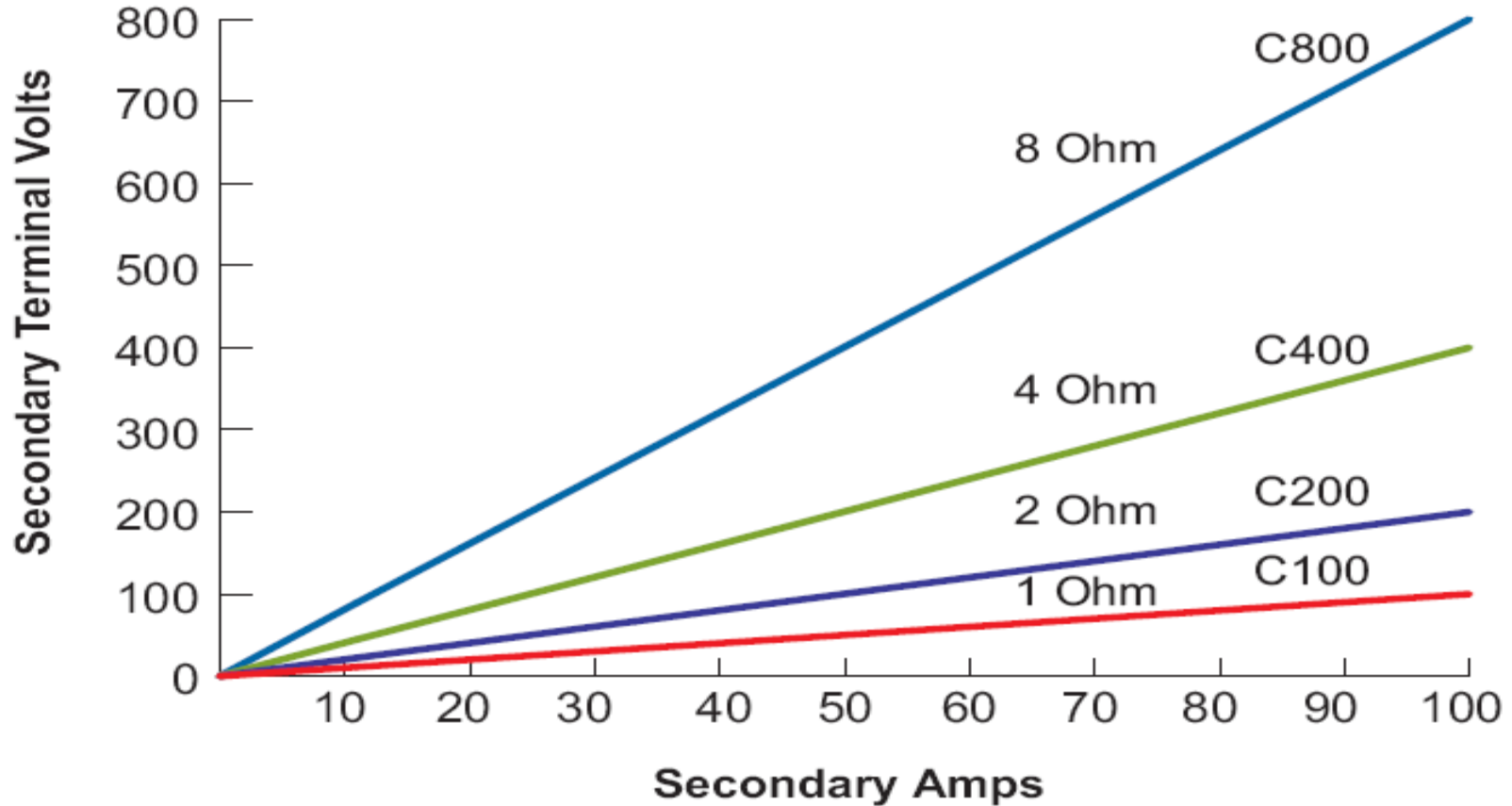
Knee point voltage

- Knee point
  - Log-log plot
  - Square decades
  - I.e. (.01,1) – (.1,10)
  - Tangent 45⁰ line (knee pt)

Current Ratio	Turn Ratio	Sec. Res. 1
50:5	10:1	.061
100:5	20:1	.082
150:5	30:1	.104
200:5	40:1	.125
250:5	50:1	.146
300:5	60:1	.168
400:5	80:1	.211
450:5	90:1	.230
500:5	100:1	.242
600:5	120:1	.296

Notes:

1) Above The Line, The Voltage for a Given Exciting Current Will Not be Less Than 95% of The Curve Value.

2) Below The Line, The Exciting Current for a Given Voltage Will Not Exceed The Curve Value by More Than 25%.

Differential measurement difficulties

- Three measuring conditions

    - normal load flow - no differential current

    - external fault - ideally no differential current

    - internal fault - high differential current

- CT saturation

    - causes false differential current for external faults

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CT saturation

- CT core may reach saturation flux density due to a combination of dc offset in the fault current, with possibility remnant flux (20-80%, no way to predict, but can be erased by demagenatizing)

- The output current suddenly changes from a proportional signal to zero

- DC saturation depends on

    - system time constant (X/R)- large close to generating stations

    - secondary burden

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CT saturation

- CT secondary model

  - a perfect current source (infinite impedance) in parallel with an exciting impedance branch that drives proportional current

- Exciting impedance is normally very high

- At saturation, exciting impedance drops to a very low value

  - the CT appears short-circuited

  - neither delivers nor resists current flow

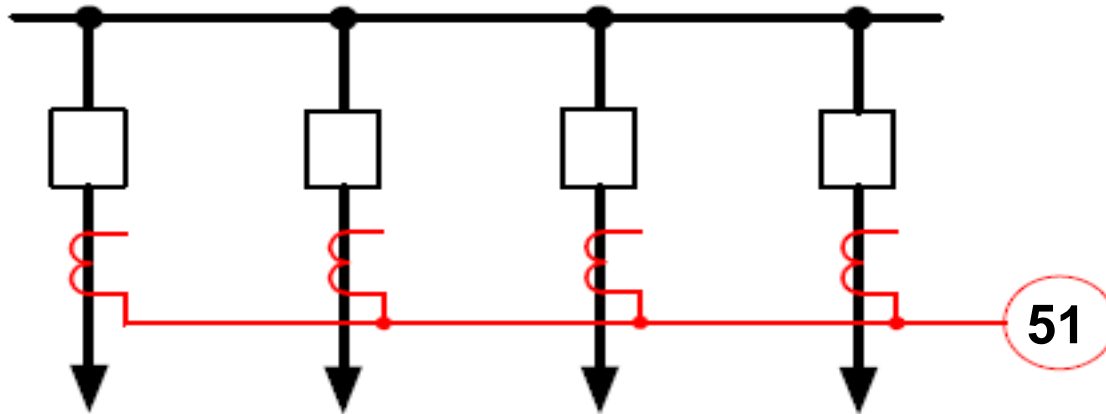- Time to saturation is important in low impedance bus protection

Issues effecting bus protection selection

- Bus arrangement
  - Fixed
  - Switchable
- Availability and characteristics of current transformers
- Performance requirements
  - Speed
  - Dependability
  - Security
  - Sensitivity (for high impedance grounded system)
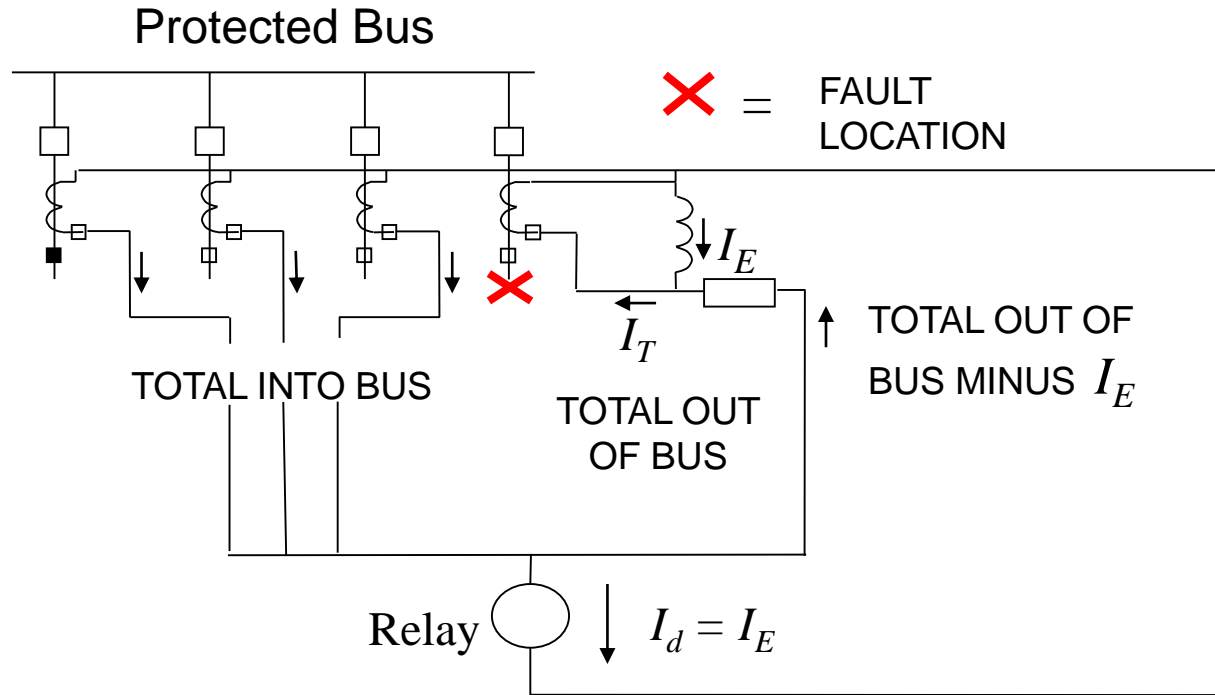
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Types of bus protection

- Differential

    - Differentially connected overcurrent

    - Percentage-restrained differential (low Z)

    - High impedance differential

    - Partial differential

- Zone interlocked scheme

- Back up schemes (eg. remote over-reaching zones)

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Differentially connected overcurrent relay

External fault case

Protected Bus

$$\textcolor{red}{\times} = \text{FAULT LOCATION}$$
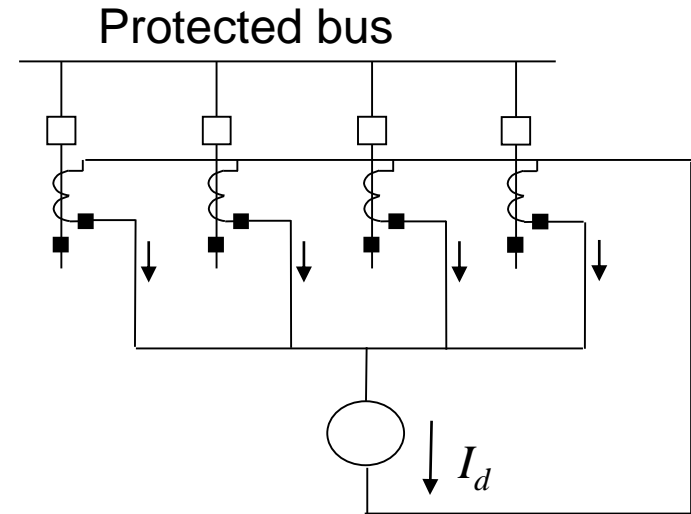
I_E

I_T

TOTAL OUT OF BUS MINUS I_E

TOTAL INTO BUS

TOTAL OUT OF BUS

Relay

$I_d = I_E$

Internal fault case

Protected Bus
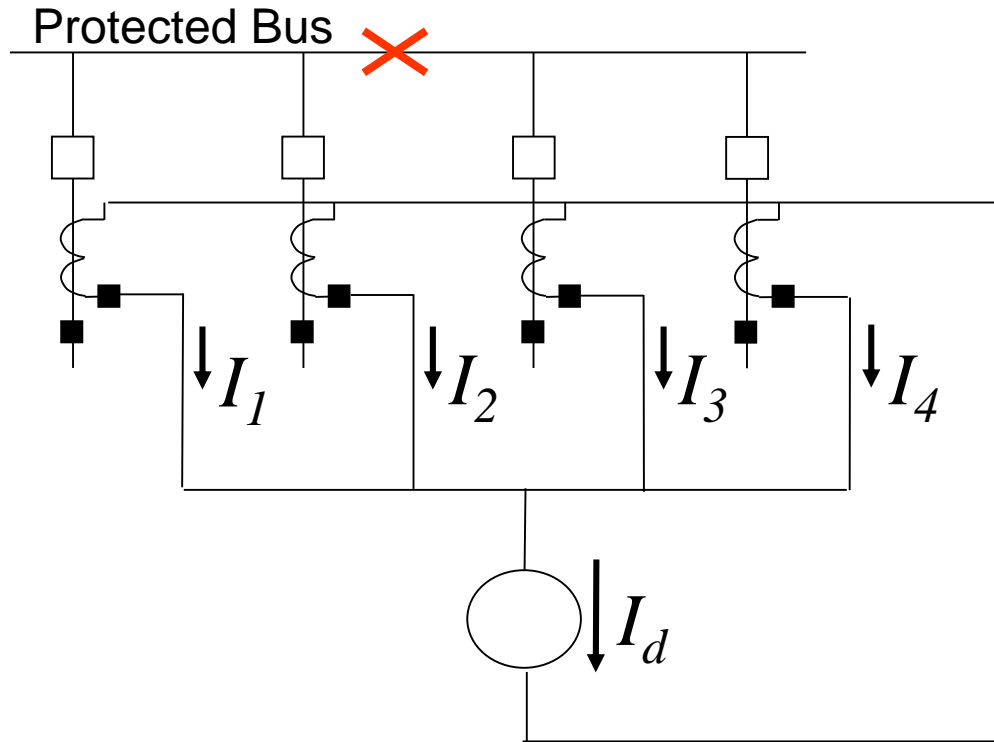
$$I_d = I_1 + I_2 + I_3 + I_4$$
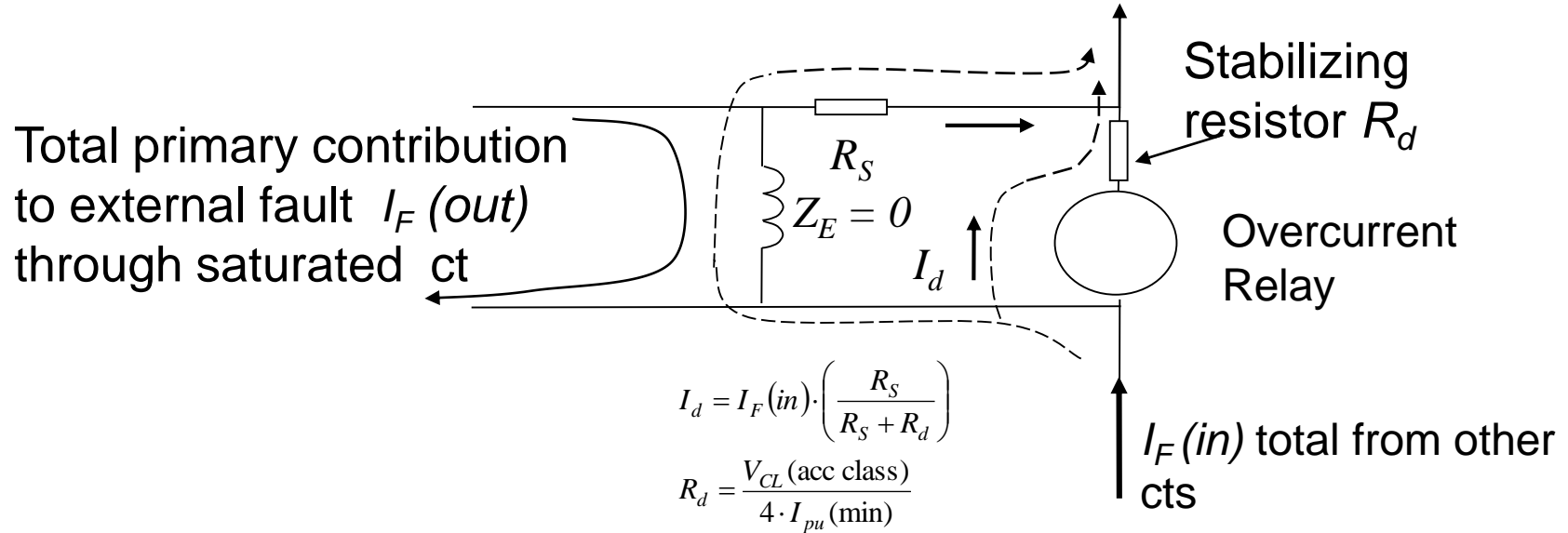
Overcurrent relay bus differential

- Application OK if:

    - Symmetrical CT secondary current less than 100

    - Burden less than rated

    - Typical pickup setting $I_{PU} > 10A$

    - Trip delay greater than 3 x primary time constant (L/R)

Protected bus

$\downarrow I_d$

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Resistor added to relay branch
External fault

Total primary contribution
to external fault I_F *(out)*
through saturated ct

Stabilizing
resistor R_d

R_S

$Z_E = 0$

I_d

Overcurrent
Relay

$$I_d = I_F(in) \cdot \left(\frac{R_S}{R_S + R_d} \right)$$

$$R_d = \frac{V_{CL}(\text{acc class})}{4 \cdot I_{pu}(\min)}$$

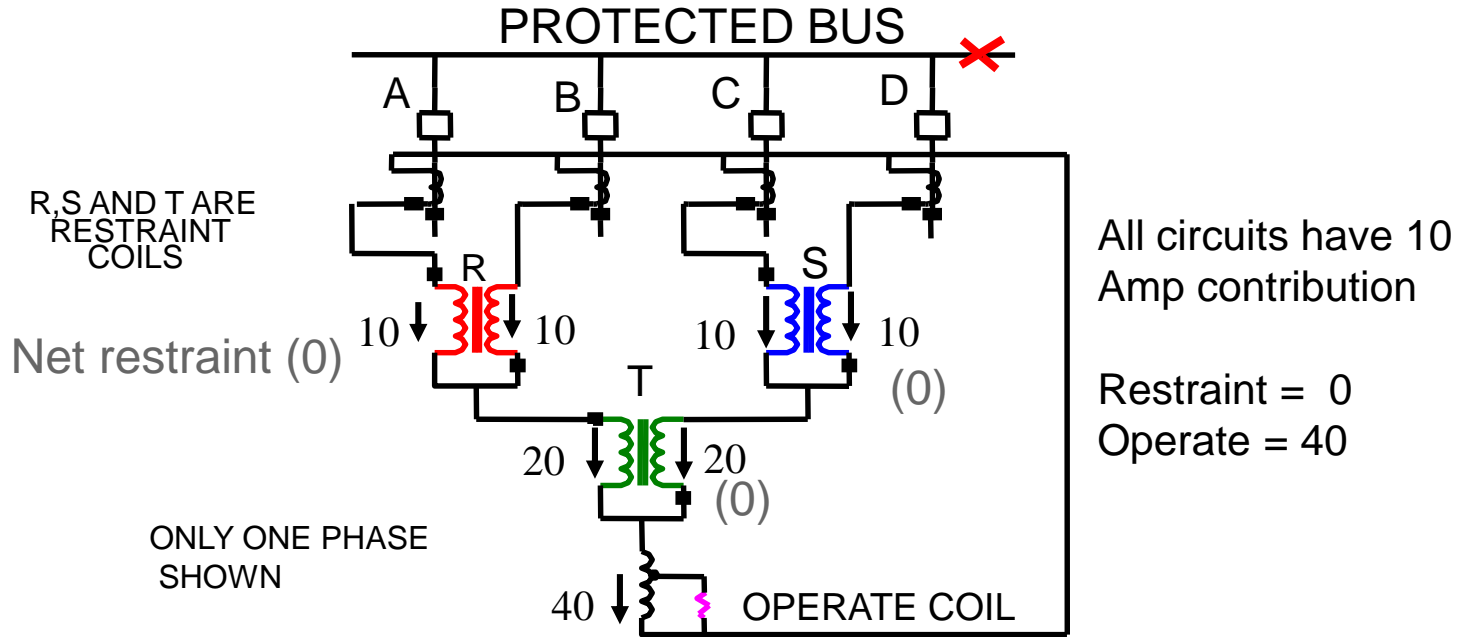I_F *(in)* total from other
cts

- Resistor reduces current in relay and increases current in R_S (secondary and lead)
- Increases sensitivity to internal faults

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Multiple restraint Percentage Differential (Legacy)

PROTECTED BUS

A   B   C   D

R,S AND T ARE
RESTRAINT
COILS

R

Net restraint (0)

10   10   10   30

S

(20)

T

20   20

(40)

ONLY ONE PHASE
SHOWN

0   OPERATE COIL

All circuits have 10
Amp contribution

Restraint = 60
Operate = 0
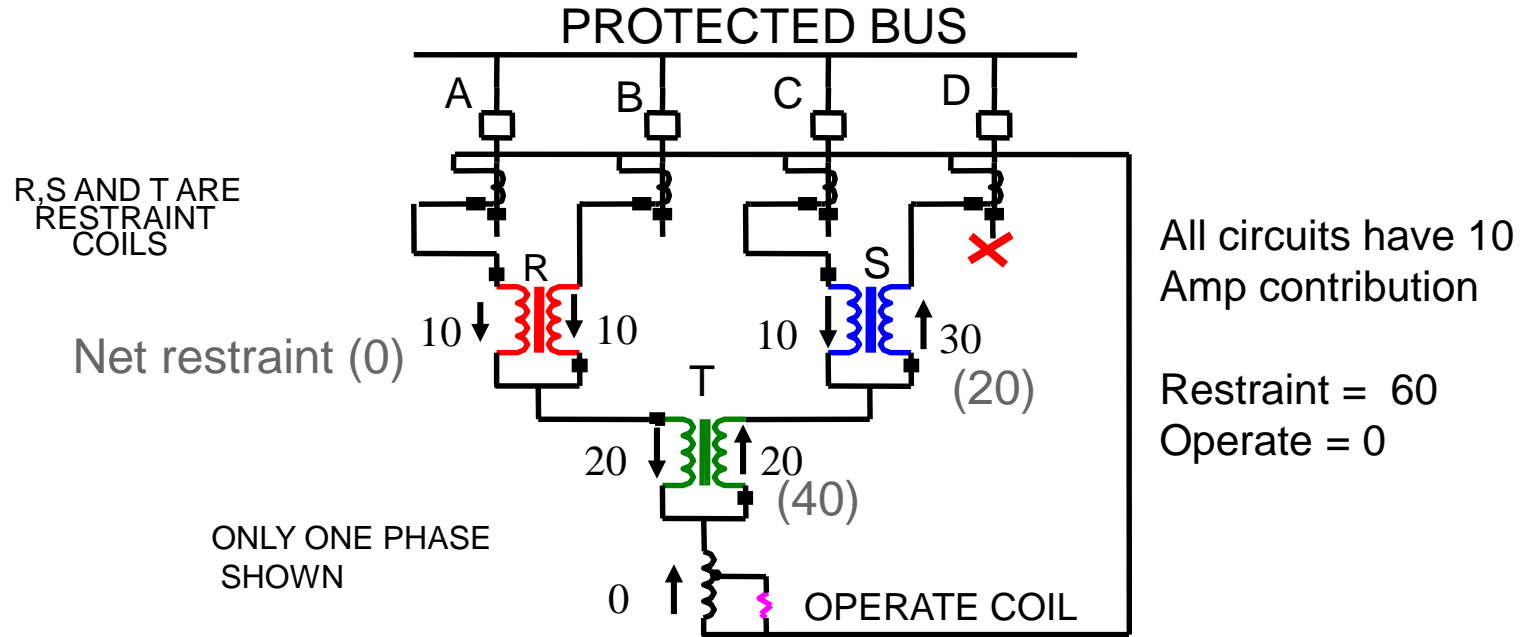
External fault example – 4 circuit connection

Multiple restraint Percentage Differential (Legacy)

PROTECTED BUS

A   B   C   D

R,S AND T ARE RESTRAINT COILS

R   S

Net restraint (0)

10 ↓ ↓ 10   10 ↓ ↓ 10

(0)

T

20 ↓ ↓ 20

(0)

ONLY ONE PHASE SHOWN

40 ↓   OPERATE COIL

All circuits have 10 Amp contribution
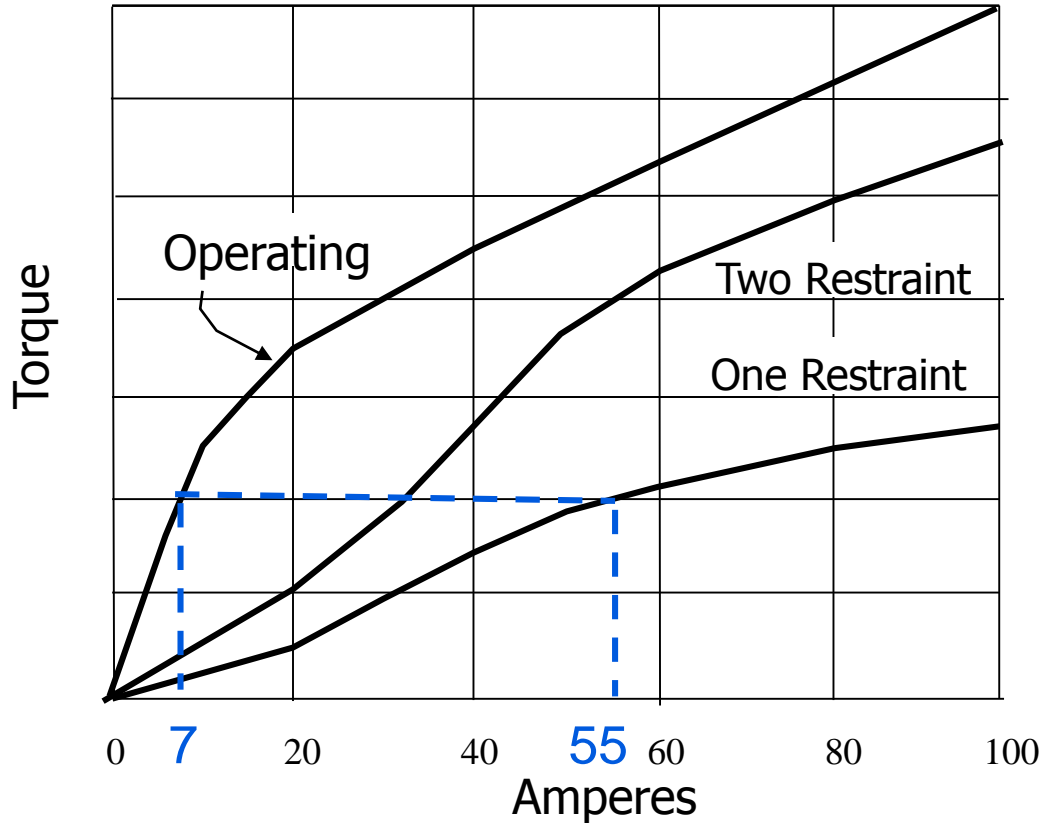
Restraint = 0
Operate = 40

Internal fault example – 4 circuit connection

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Torque for typical multi-restraint relay
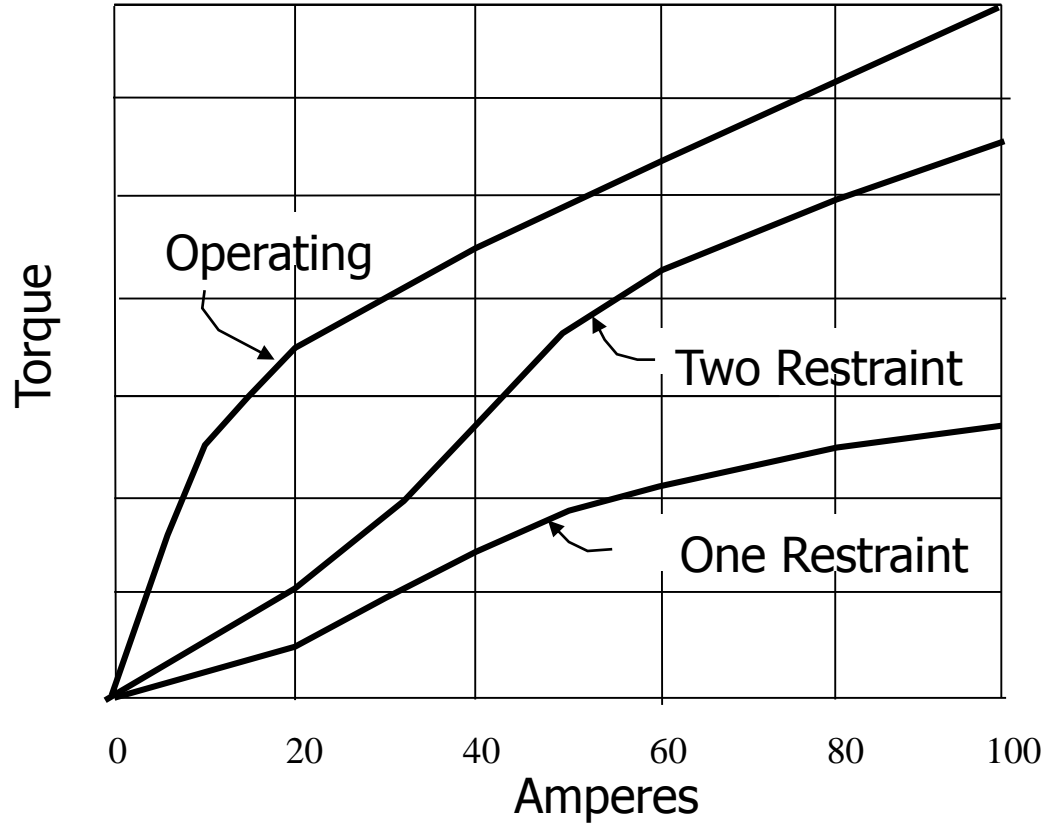
Torque for typical multi-restraint relay

55 A. of restraint overcomes 7 A of operating current with one restraint winding

Multi-restraint percentage differential

- Good sensitivity

- Good security

- Allows other relays on the same CT core

- Different CT ratios with Aux CTs.

- Slow compared to high impedance

- Number of feeders limited by restraint windings

- Each CT is wired to relay

- ## Not easily extendable

High impedance bus protection

- High resistor (R > 1500 ohm) in series with relay coil and a MOV to prevent over-voltages

- High voltage develops for internal faults. lower Voltage will develop on external faults under ct saturation

- Voltage unit must be set higher than the maximum junction point voltage for any external fault

- The lowest achievable sensitivity must verified for the application

- Proven reliability and very sensitive

- Operating times of less than one cycle for internal faults
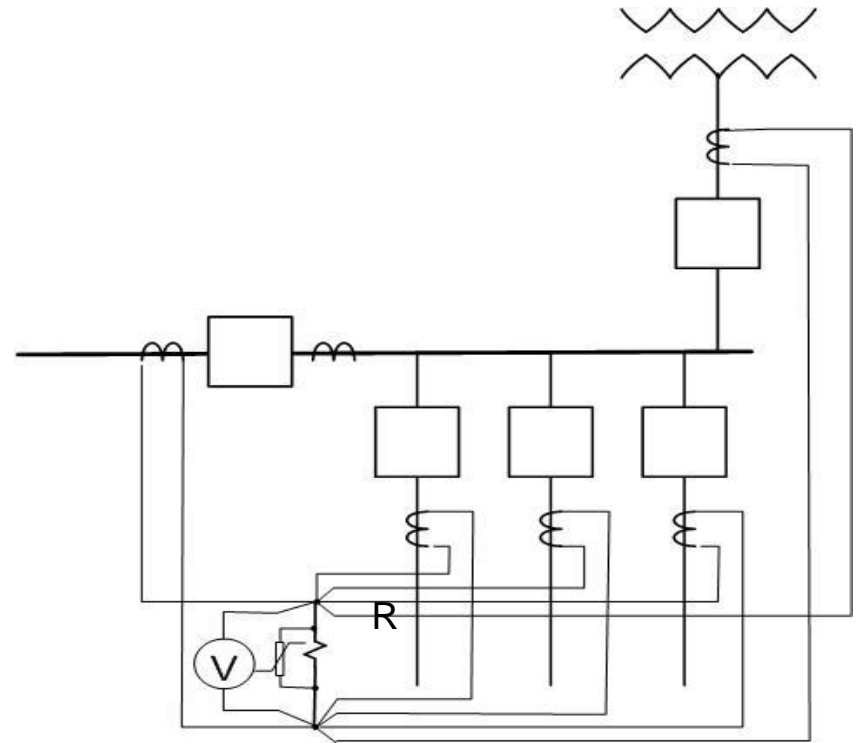
High impedance bus protection

EXILERNAL FAULT - *SECURITY*

Setting $V_R > (I_F / N)(R_L + R_S)$

K = margin factor
I_F = Max external fault current
R_S = Ct secondary resistance
R_L = Lead resistance to junction box
N = ct turns ratio

INTERNAL FAULT - *SENSITIVITY*
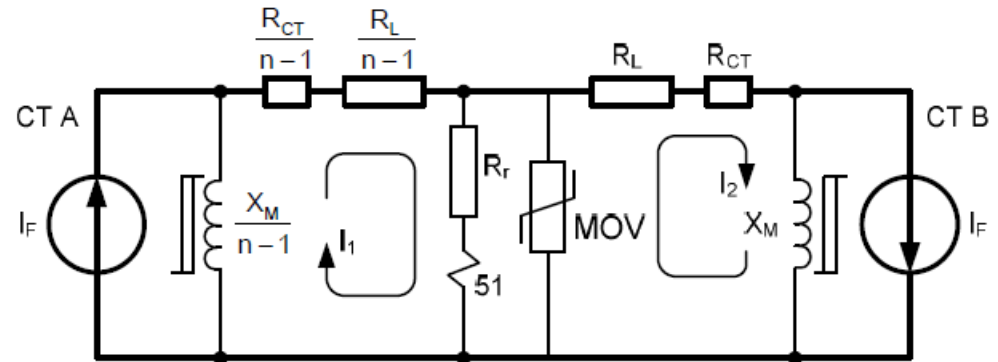
$I_{MIN} = (XI_E + I_R + I_V)N$

X = number of circuits
I_E = Ct exciting current at V_R
I_R = resistor current at V_R
I_V = Varistor current at V_R

R > 1500 W

High impedance bus protection
Criteria to be met

- Objective: Keep V_R and I_{min} low

    - Ct secondary loop resistance kept low

    - Impedance from junction point to relay is of no consequence so good practice to parallel the CTs as close to the CTs as possible.

    - Theoretically no limitations in the number of parallel CTs but sensitivity reduced

    - Setting VR higher that the CT knee point voltage (400V for C400 CTs) will produce errors when estimating CT exciting branch current, hence inaccurate sensitivity calculation.

- All cts should have the same ratio and magnetizing characteristics

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Differential comparator (Legacy, Static type) RADSS/REB103

AUX CTs

I_{OUT}

I_{DIFF}

I_{IN}

S_R

D_R

- Developed to lessen restrictions imposed by high impedance
- All CT secondary circuits connected via interposing cts
- Connection made using a special diode circuit producing rectified incoming, outgoing and differential currents
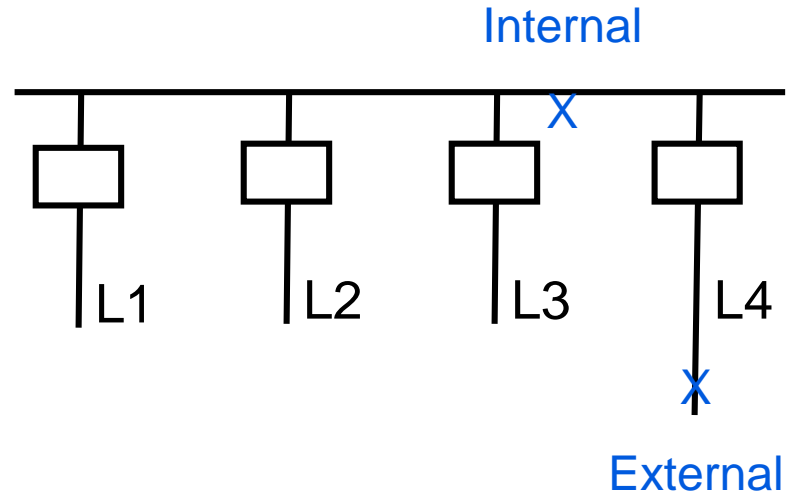
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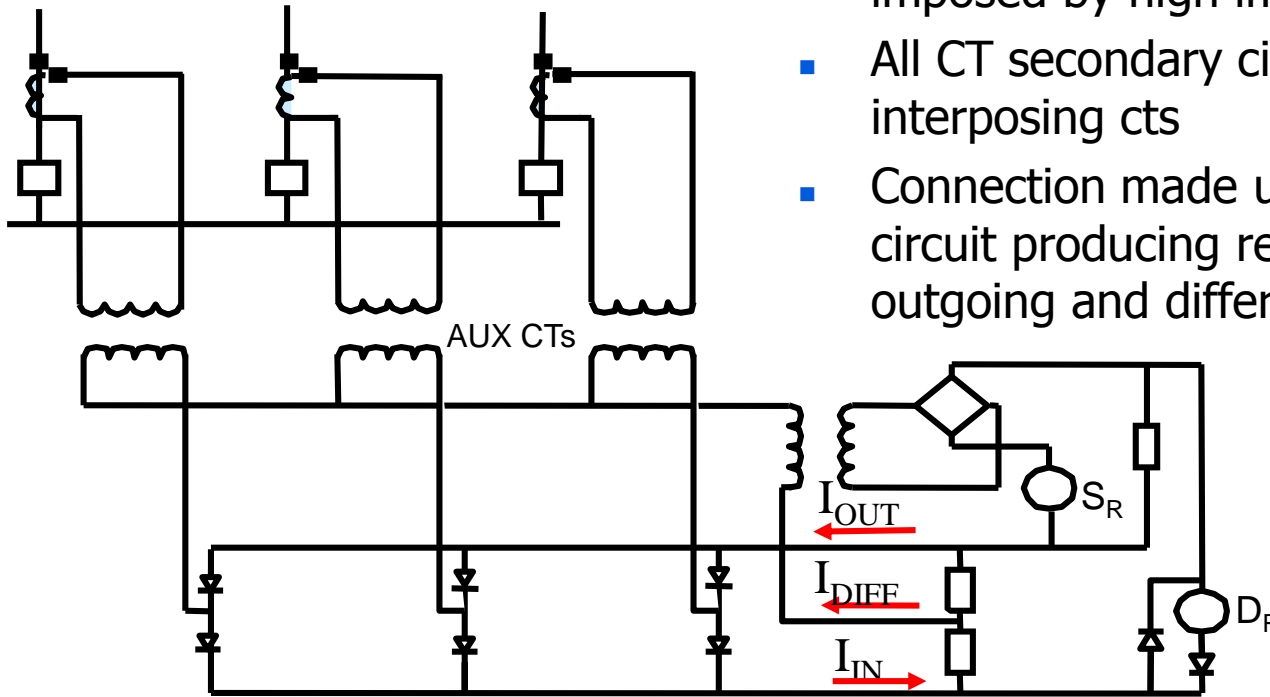
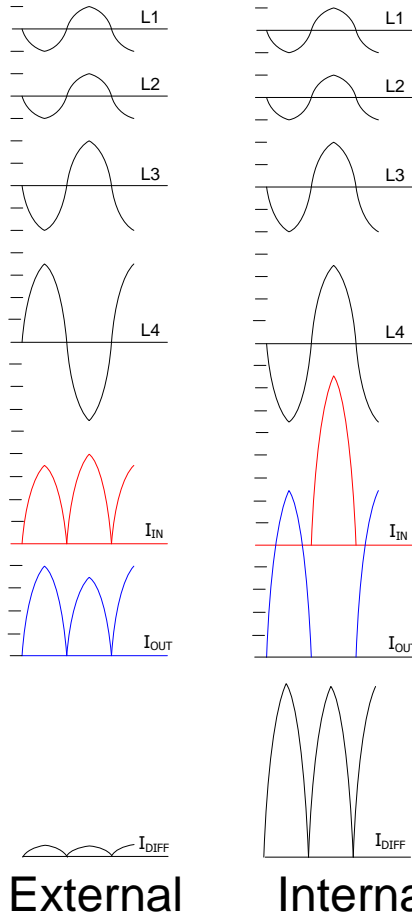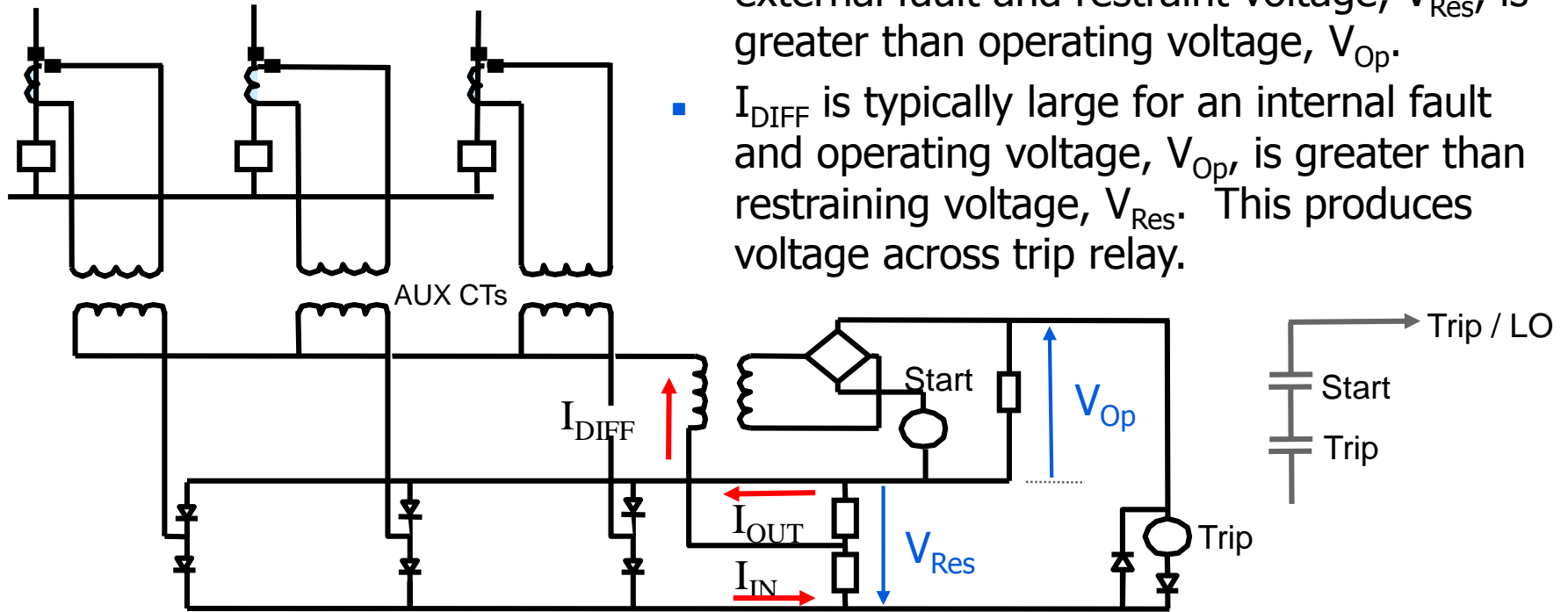# Differential comparator
Single phase connection
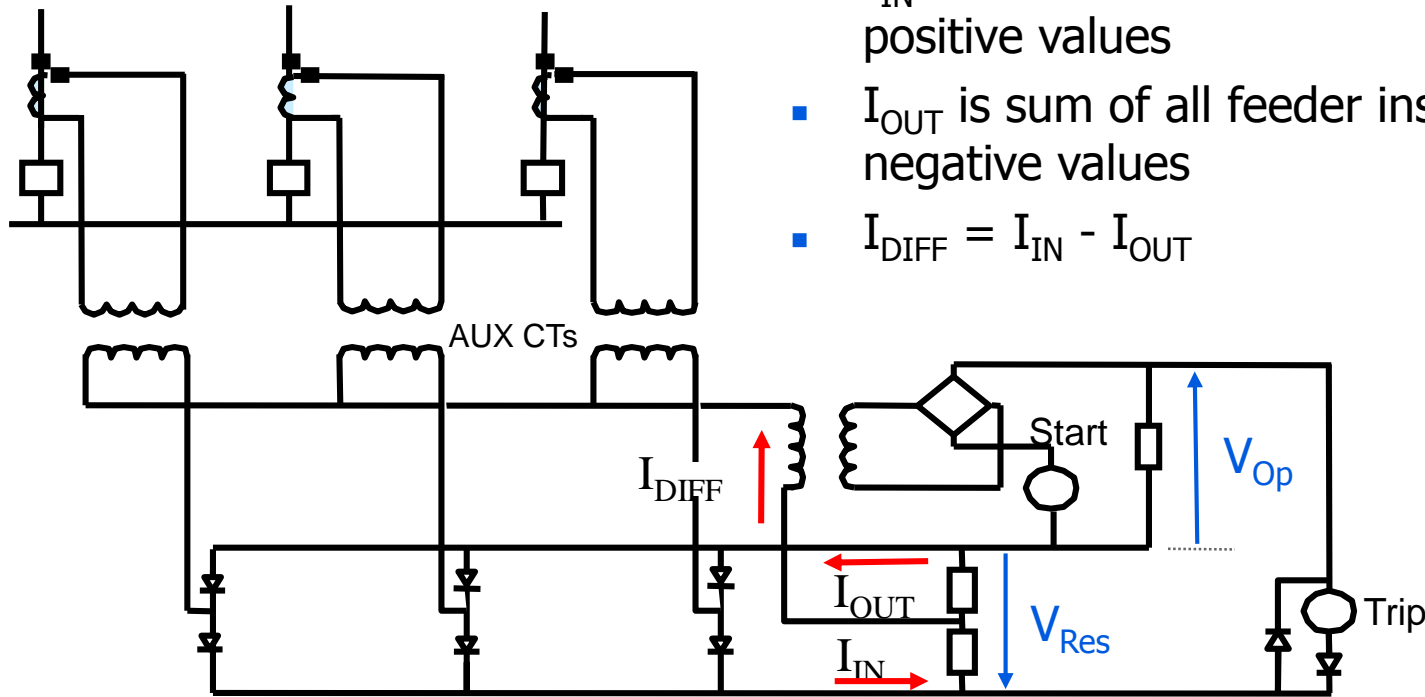
- I_{IN} is sum of all feeder instantaneous positive values

- I_{OUT} is sum of all feeder instantaneous negative values

- $I_{DIFF} = I_{IN} - I_{OUT}$

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Differential comparator

L1
L2
L3
L4
I_{IN}
I_{OUT}
I_{DIFF}

External

L1
L2
L3
L4
I_{IN}
I_{OUT}
I_{DIFF}

Internal

Internal

X

L1   L2   L3   L4

X

External

Differential comparator
Single phase connection

- I_{DIFF} is typically small (normally 0) for external fault and restraint voltage, V_{Res}, is greater than operating voltage, V_{Op}.

- I_{DIFF} is typically large for an internal fault and operating voltage, V_{Op}, is greater than restraining voltage, V_{Res}. This produces voltage across trip relay.

AUX CTs

I_{DIFF}

I_{OUT}

I_{IN}

Start

V_{Op}

V_{Res}

Trip

Trip / LO

Start

Trip

Differential comparator

- ## All measurement decisions based on three quantities

  - I_{DIFF} - difference of input current and output current ($I_{DIFF} = I_{IN} - I_{OUT}$)

  - I_{IN} - total input current

  - S - % differential setting

- $I_{DIFF} > S \times I_{IN}$

  - e.g. for setting S=50%, differential current $\geq$ 50% of incoming current before operation
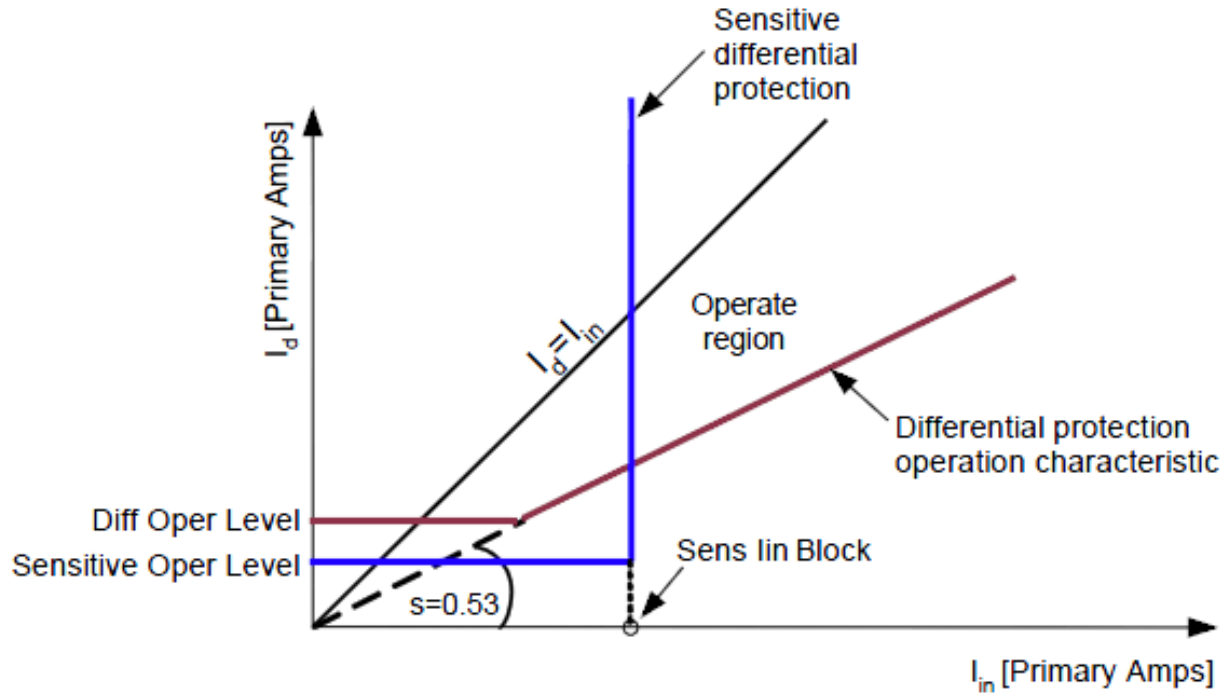
Differential comparator
Advantages over high impedance differential

- Lower ct requirements

- Allows much higher ct loop resistances

- Accommodate different CT ratios / auxiliary CTs

- Fast operating times for internal faults

  - Detects internal 1 - 3 ms
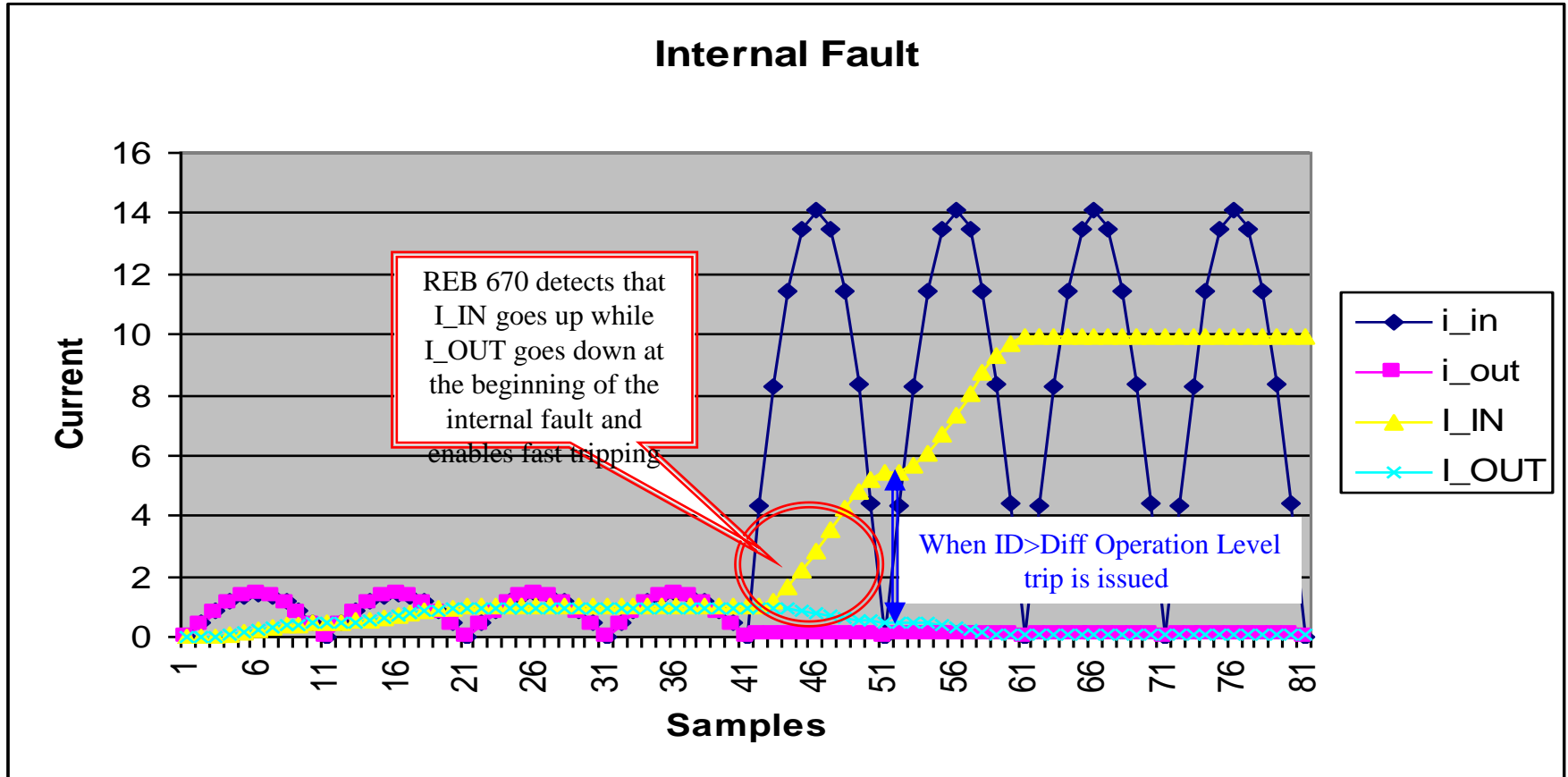
  - Before ct saturation

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Numerical differential comparator

- Analog input currents are instantaneously sampled and quantized to numerical number

- Similar technique to legacy differential comparator, but with measured sampled data

- Secondary circuit loop resistance no longer a critical factor

- Critical factor is time available to make the measurement, i.e. time to saturation. (only 3ms required to properly restrain for heavy external faults)

- Algorithms for Ct saturation Detection and CT state supervision

Differential comparator

Quick operation for internal fault

Internal Fault

REB 670 detects that I_IN goes up while I_OUT goes down at the beginning of the internal fault and enables fast tripping

When ID>Diff Operation Level trip is issued

Legend: i_in, i_out, I_IN, I_OUT

Axis labels: Current (y-axis), Samples (x-axis)

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Proper & secure restrain during external fault

External Fault

REB 670 detects this short interval when i_in=i_out (after every fault current zero crossing) and restrain properly during external fault

REB 670 detects that I_IN=I_OUT at the beginning of the external fault

Legend:
- i_in
- i_out
- I_IN
- I_OUT

Y-axis: Current (0, 2, 4, 6, 8, 10, 12, 14, 16)

X-axis: Samples (1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77, 81)
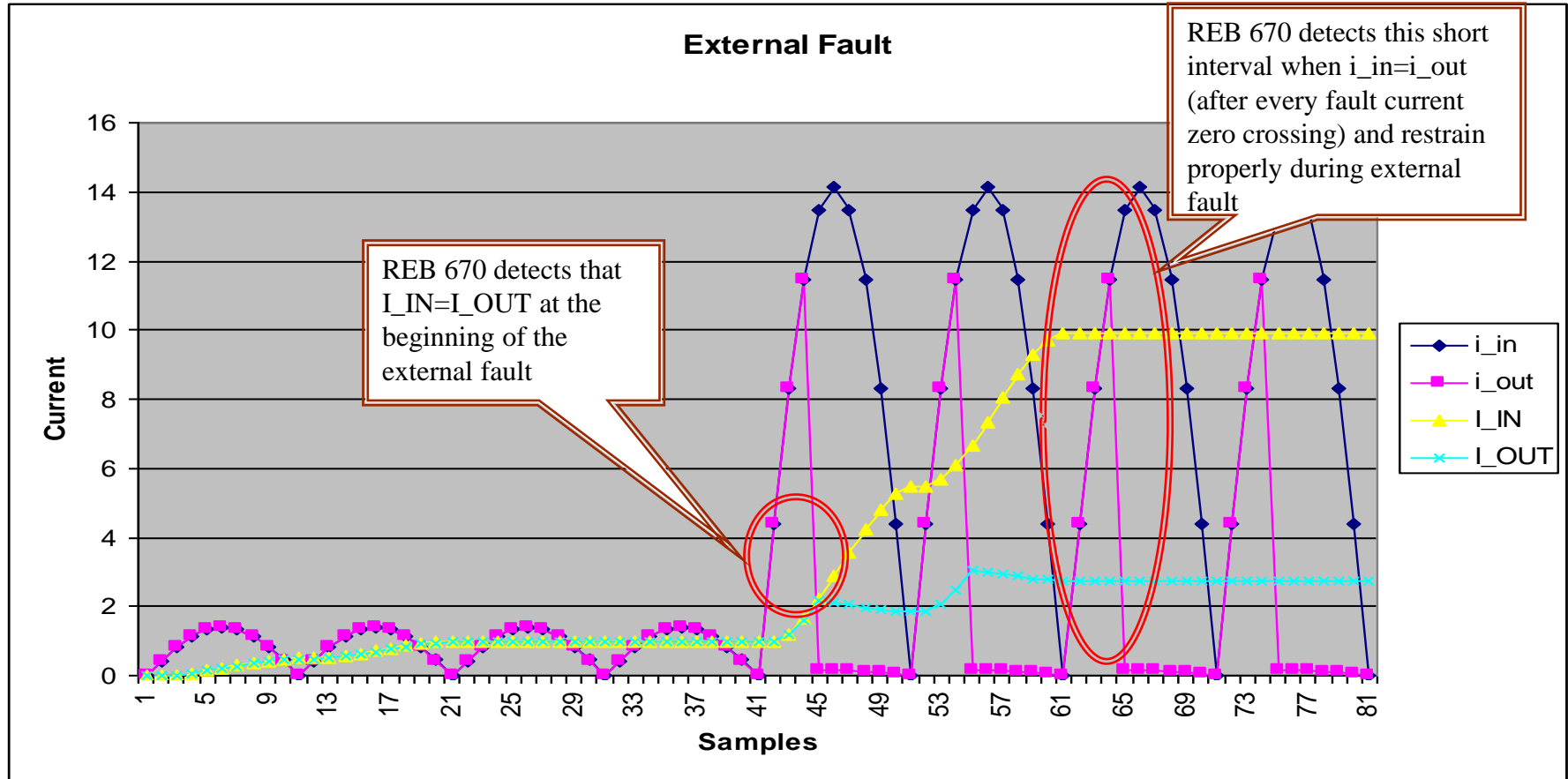
Fast open CT algorithm
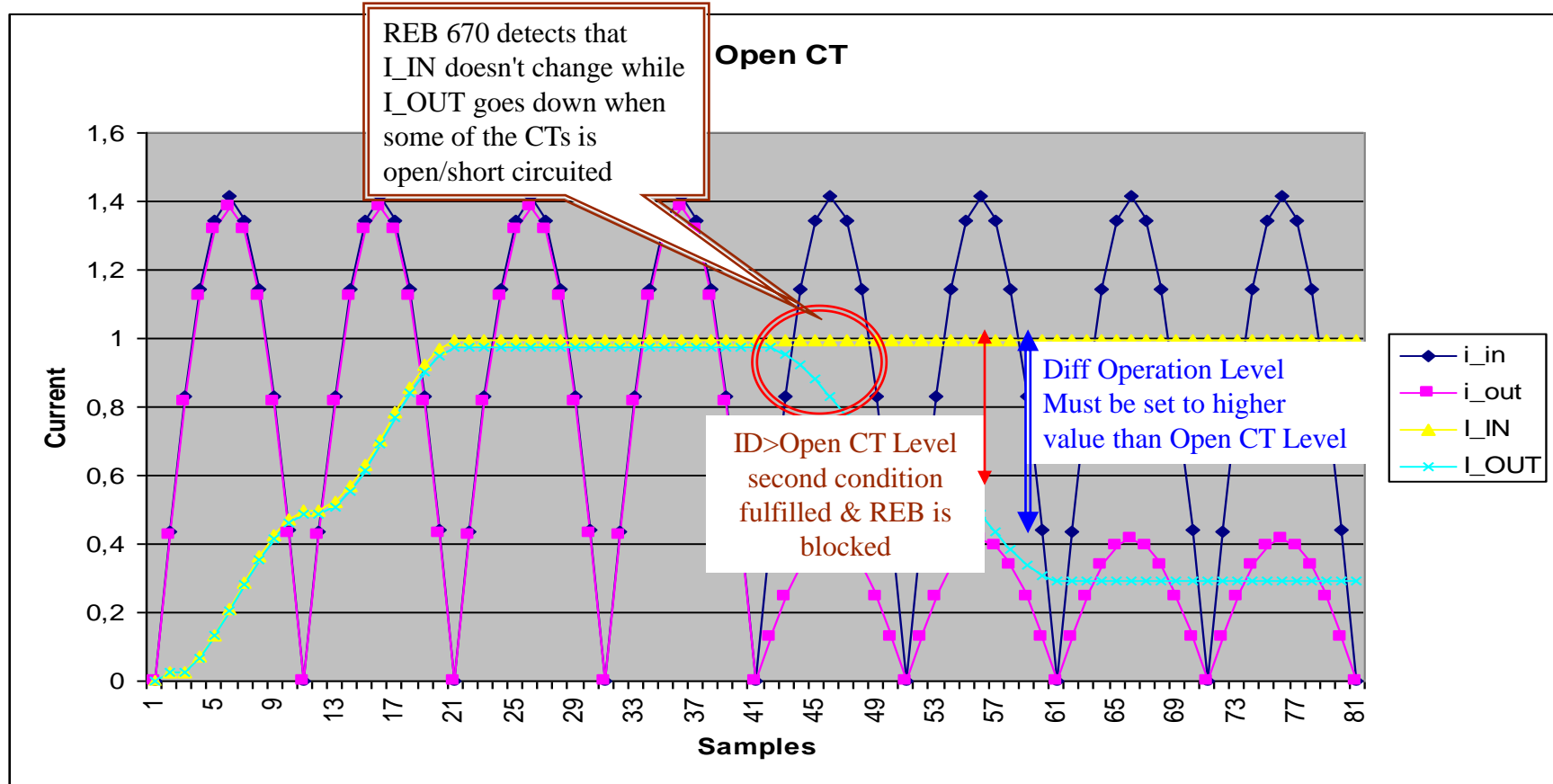
Other Features in Modern Numerical Bus IEDs

- Each device capable of connecting multiple bays (eg. CTs) in 3-ph or 1-ph design

- Multiple differential zones, dynamic bay switching, zone interconnection, and check zone logics

- External fault/CT saturation detection, open CT detection algorithms

- Blind zone protection (see next 2 slides)

- End zone protection (see next 2 slides)

- Backup protection (eg. 50/51, 50BF) for each connected bay

- Modern substation automation communication (DNP 3.0, IEC61850)

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Blind zone detection for bus coupler bays

- Blind zone between live tank CT and breaker

- Fault strikes in the blind zone

- Tie bkr normally closed: ZA operates but Zone B restrains -> the fault is persisting

- Tie bkr normally open: ZA operates unnecessarily and ZB restrains

- Solution: connect BKR NC (open) status to the bay to remove the tie CT from ZA, ZB (software)

- ZA will then restrain and ZB operates properly for the blind zone fault
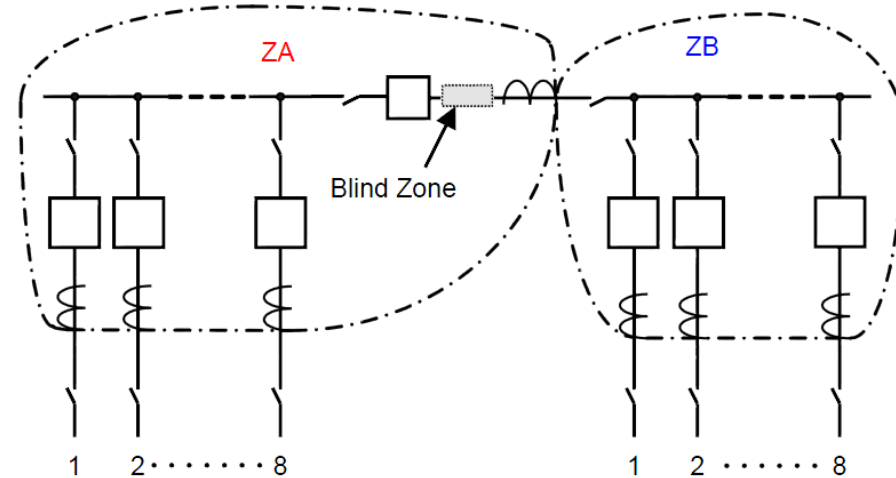
Blind zone detection for feeder bays

- Regions not overlapped by both red and blue boundaries are blind zones

- CTs are used for both feeder and bus protection measurement (live tank CTs)

- Common in HV 1-1/2 stations

- For 3. measuring CT can be removed (BBP) to avoid over-tripping on open pos. Fast OC set up to DTT (open pos)

- For 4. measuring CT can be removed (BBP) to force tripping on open pos (feeder protection operates first)


where:
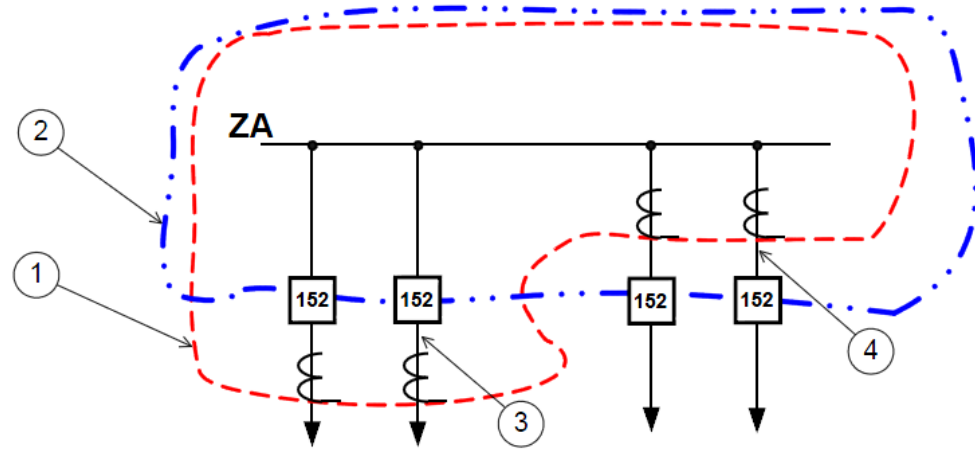
1   is Busbar Protection measuring boundary determined by feeder CT locations

2   is Busbar Protection internal fault clearing boundary determined by feeder CB locations

3   is End fault region for feeders as shown in figure 36/B

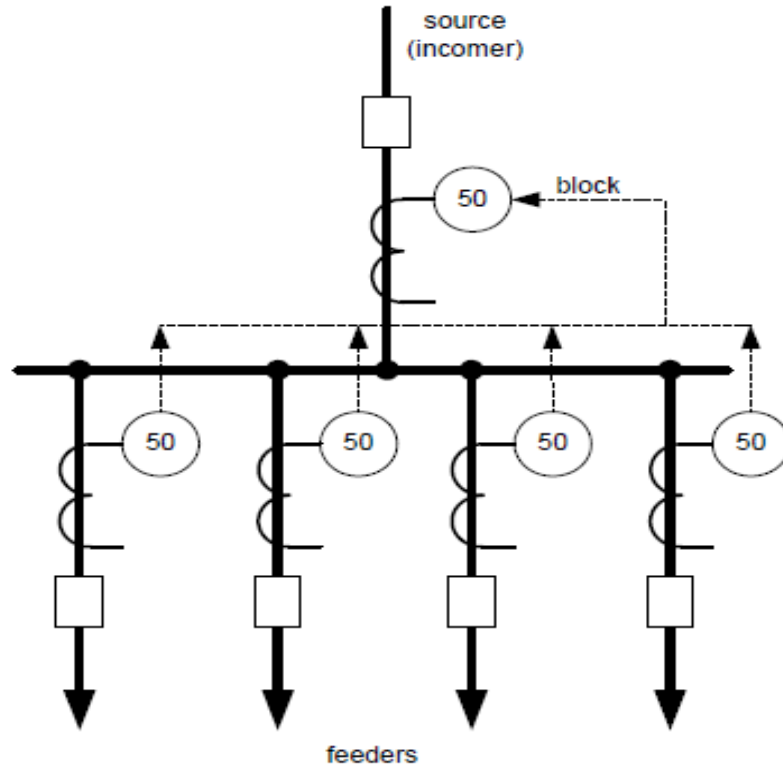4   is End fault region for feeders as shown in figure 36/C

Other distribution (MV) bus protection methods
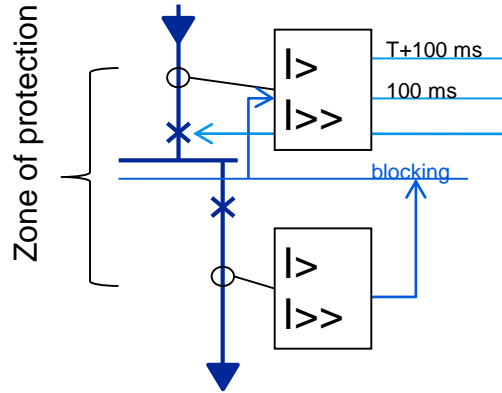
- Partial differential

- Blocking on feeder fault

Partial differential
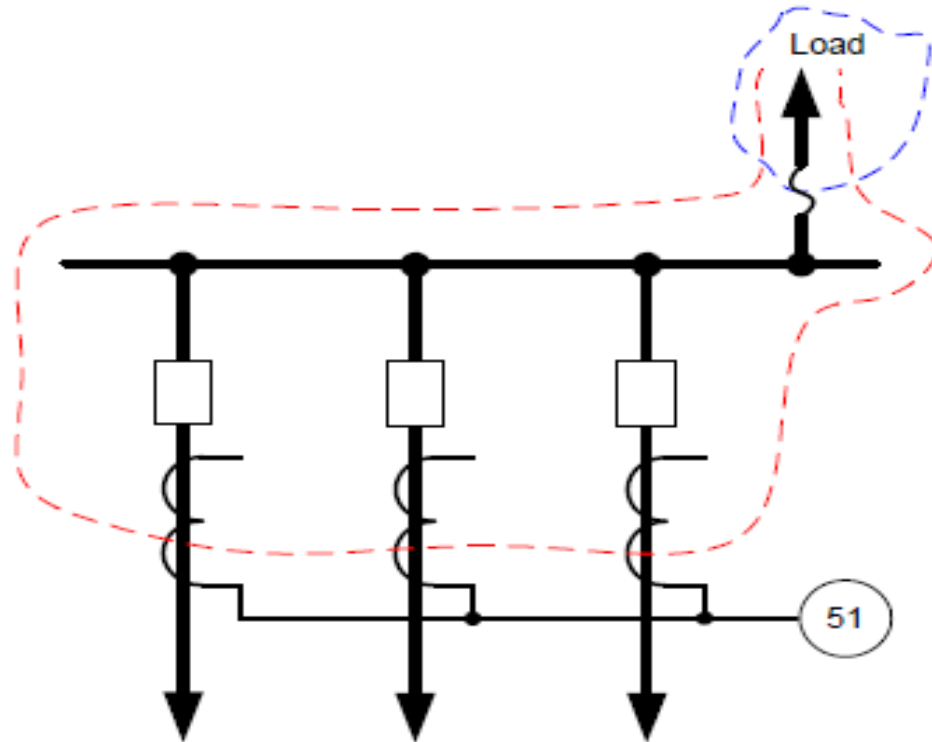
Blocking scheme

Conventional Blocking Scheme

Zone of protection

I> T+100 ms
I>> 100 ms

blocking

I>
I>>

Delay setting with inst. O/C protection (conventional approach)

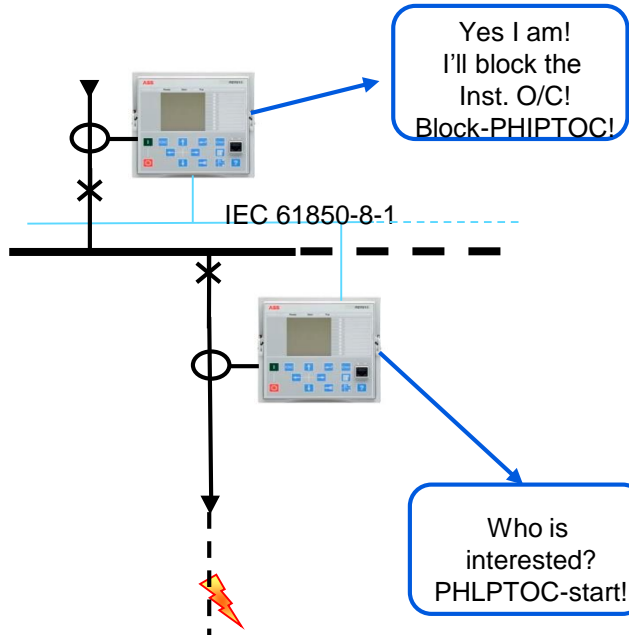|	
Safety marginal, e.g. delay in operation due to CT saturation.	**20…40 ms**
O/C protection start delay + output relay's delay	**<40 ms**
Start delay with receiving relay + retarding time for the blocking signal *)	**<40 ms**
ALL TOGETHER	**100…120 ms**

- Traditional busbar protection based on upstream blocking

  - Dedicated hard-wire signal paths needed

  - Signal path delay needs to be considered, input and output delay + auxiliary relays

  - Changes in the protection scheme may require re-wiring

- Typical needed delay in incoming relay is over 100 ms

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Blocking Scheme with IEC-61850 GOOSE

Delay setting with inst. O/C protection (REF615 GOOSE approach)	
Safety marginal, e.g. delay in operation due to CT saturation.	**20…40 ms**
O/C protection start delay	**20 ms**
Retardation time of inst. O/C stage blocking	**5 ms**
GOOSE delay (Type 1A, Class P1)	**<10 ms**
ALL TOGETHER	**55…75 ms**

Bus protection comparison chart

	COST	EASE OF USE	SENSI-TIVITY	DEPEND ABILITY	SECURITY	FLEXI-BILITY	SPEED
SIMPLE OVER-CURRENT	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
MULTIPLE RESTRAINT	MED	POOR	BEST	GOOD	GOOD	POOR	GOOD
HIGH IMPEDANCE	MED	GOOD	GOOD	GOOD	BEST	GOOD	FAST
PERCENTAGE RESTRAINED DIFFERENTIAL	HIGH	BEST	GOOD	GOOD	BEST	BEST	BEST
PARTIAL DIFFERENTIAL	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
BLOCKING	MED	GOOD	POOR	GOOD	GOOD	GOOD	FAST

Questions?
Recommended reading

- ANSI C37.234 Guide for Protective Relay Applications to Power system Buses

Thank you for your participation

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