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ABB Protective Relay School Webinar Series

Bus Protection Fundamentals Jack Chang, RTM, Western CA October 1, 2013



Presenter



Jack Chang

Jack Chang is the regional technical manager for ABB Inc. in the Substation Automation Products BU serving customers in western Canada and northern regions. He provides engineering, commissioning and troubleshooting support to customers applying ABB's high-voltage protective and automation devices. Prior to joining ABB, Jack worked as a substation P&C project engineer in two specialized consulting firms (now ABB and Quanta Services, respectively) and also as an engineering consultant to a public owned utility in their transmission expansion and upgrade projects. Jack is a registered professional engineer in the province of Alberta, Canada.



Learning objectives

- Types of bus configurations
- Current transformer characteristics and their effect on bus protection
- Types of bus protection schemes
- Modern Numerical Bus Protection Features

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Why bus protection?

- Different configuration and design
- Usually very robust, high current faults
- Need to clear quickly
- A Delayed bus trip leads to:
 - Network instability pole slip of nearby generators
 - Possible system collapse
 - Bigger fault related damages & risk to human life or injury
 - Many bus faults caused during maintenance (eg. Arc flash)



Bus fault protection

- Easy to detect because of robust nature
- Easy to protect for internal faults (87B)
- Summation of currents not equal to zero for internal fault
- External faults can cause current transformer saturation which results in unwanted differential currents
- Infrequent, but must be cleared with high speed
 - Substation is well shielded
 - Protected environment

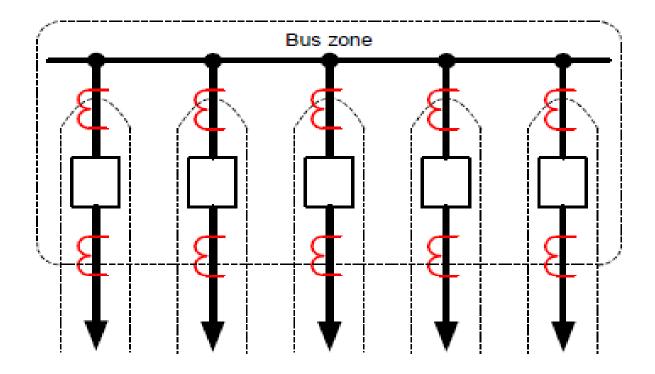


Bus configurations

- Single bus *
- Main and transfer bus
- Double bus, single breaker *
- Double bus, double breaker
- Breaker and a half *
- Ring bus *

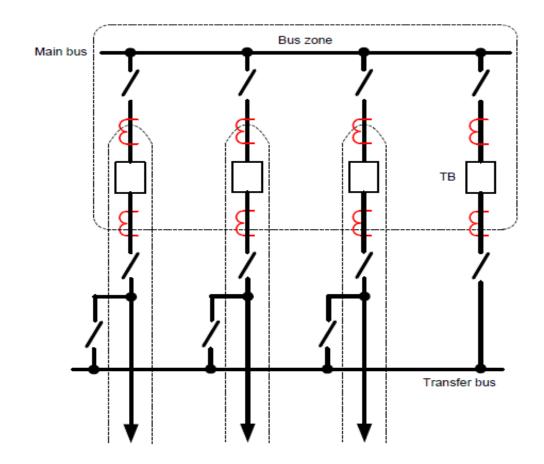


Single bus



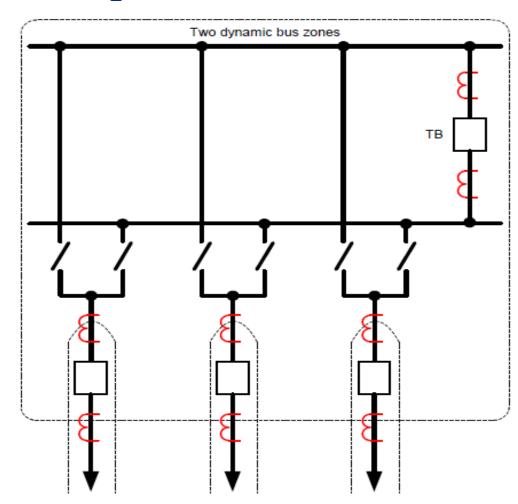


Main and transfer bus



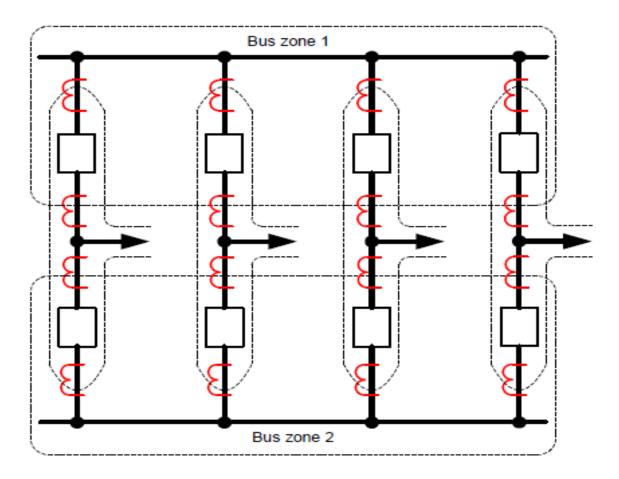


Double bus single breaker



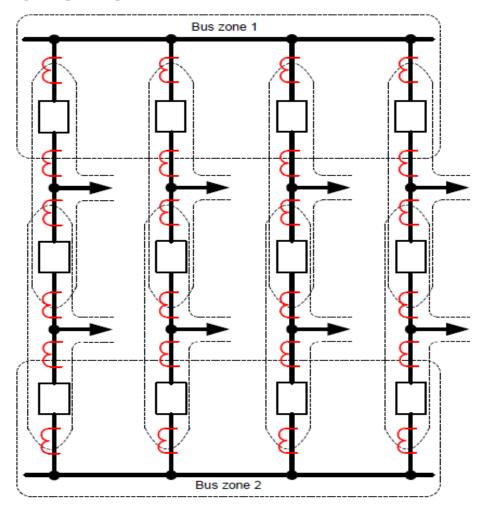


Double bus, double breaker



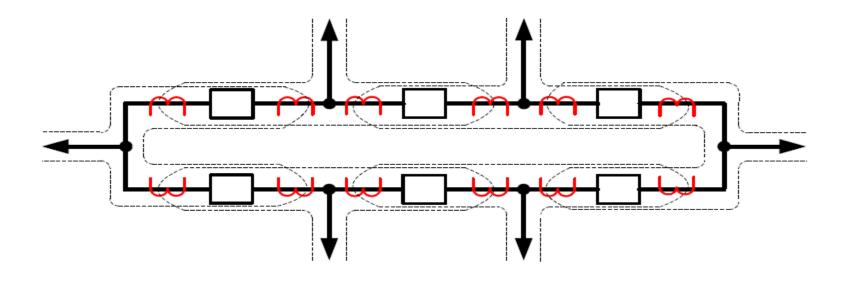


Breaker and one half



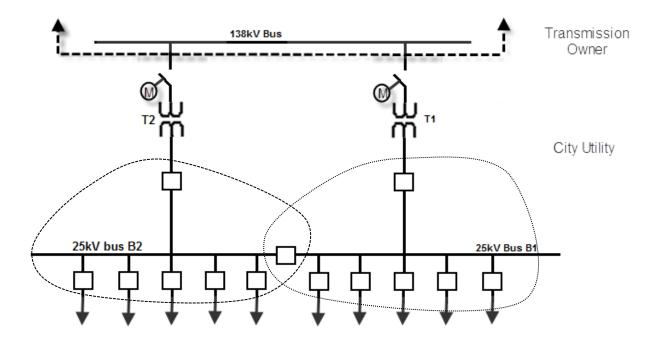


Ring bus





Main-Tie-Main



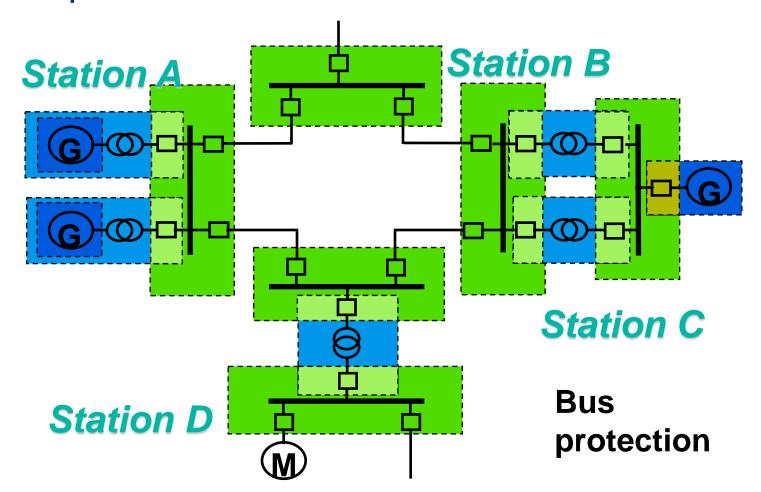


Some issues

- Availability of overlapping protection zones (CTs)
- Blind or end zone protection
- Will loads or sources be switched from one bus to the other
- Current transformer switching from one zone to another
- Open circuit current transformers
- CT Saturation

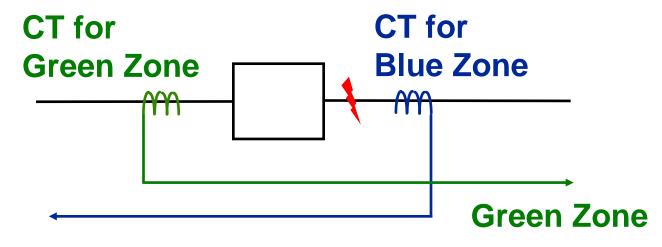


Zones of protection





Zones of protection

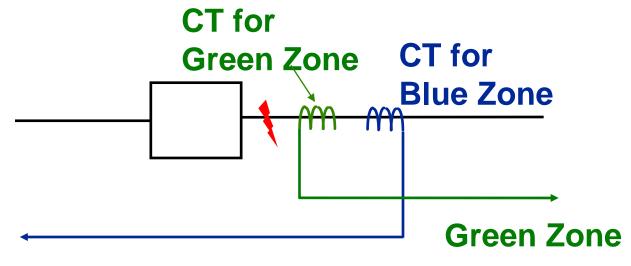


Blue Zone

Dead tank breaker, two CTs



Zones of protection



Blue Zone

Live tank breaker, single CT



Current transformer Ratings of concern for bus protection

- Ratio: 200/5, 1200/5, ...500/1
- Burden capability: VA burden
- Accuracy Class: C800, K200, T400
- Knee point, saturation voltage (can be derived from chart in C class CTs)
- CT availability
- IEEE Standard C57.13-1993 (R2003), IEEE Standard Requirements for Instrument Transformers
- IEEE Standard C37.110-1996, IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes

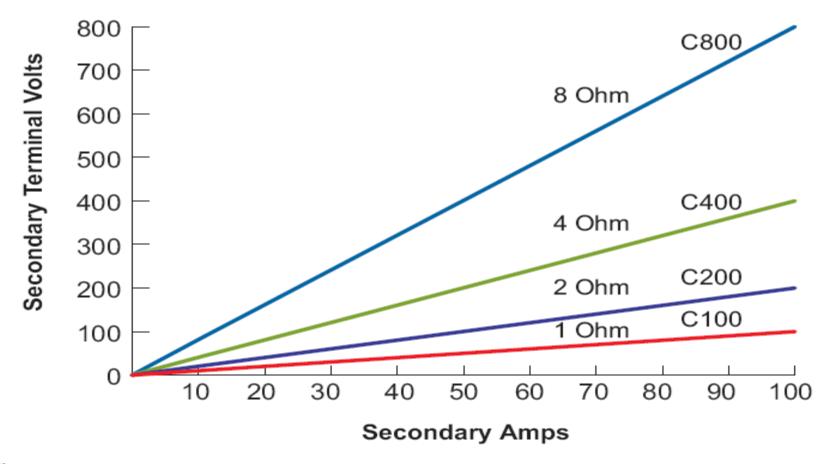


ANSI current transformer accuracy class

- Example 1200/5 C800
- This current transformer will deliver 800 volts on its secondary when it is connected to a standard burden and 20 times rated current is flowing in the primary winding without exceeding 10% ratio error.



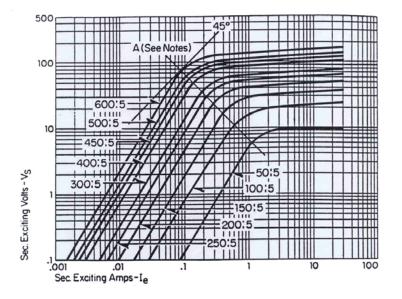
ANSI accuracy class Standard chart for class C current transformers





Knee point voltage

- Knee point
 - Log-log plot
 - Square decades
 - I.e. (.01,1) (.1,10)
 - Tangent 45° line (knee pt)



Current	Turn	Sec.
Ratio	Ratio	Res. 1
50:5	10:1	.061
100:5	20:1	.082
150:5	30:1	.104
200:5	40:1	.125
250:5	50:1	.146
300:5	60:1	.168
400:5	80:1	.211
450:5	90:1	.230
500:5	100:1	.242
600:5	120:1	.296

Notes:

- Above The Line, The Voltage for a Given Exciting Current Will Not be Less Than 95% of The Curve Value.
- Below The Line, The Exciting Current for a Given Voltage Will Not Exceed The Curve Value by More Than 25%.



Differential measurement difficulties

- Three measuring conditions
 - normal load flow no differential current
 - external fault ideally no differential current
 - internal fault high differential current
- CT saturation
 - causes false differential current for external faults



CT saturation

- CT core may reach saturation flux density due to a combination of dc offset in the fault current, with possibility remnant flux (20-80%, no way to predict, but can be erased by demagenatizing)
- The output current suddenly changes from a proportional signal to zero
- DC saturation depends on
 - system time constant (X/R)- large close to generating stations
 - secondary burden



CT saturation

- CT secondary model
 - a perfect current source (infinite impedance) in parallel with an exciting impedance branch that drives proportional current
- Exciting impedance is normally very high
- At saturation, exciting impedance drops to a very low value
 - the CT appears short-circuited
 - neither delivers nor resists current flow
- Time to saturation is important in low impedance bus protection



Issues effecting bus protection selection

- Bus arrangement
 - Fixed
 - Switchable
- Availability and characteristics of current transformers
- Performance requirements
 - Speed
 - Dependability
 - Security
 - Sensitivity (for high impedance grounded system)

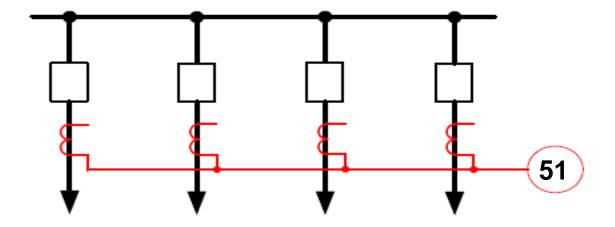


Types of bus protection

- Differential
 - Differentially connected overcurrent
 - Percentage-restrained differential (low Z)
 - High impedance differential
 - Partial differential
- Zone interlocked scheme
- Back up schemes (eg. remote over-reaching zones)

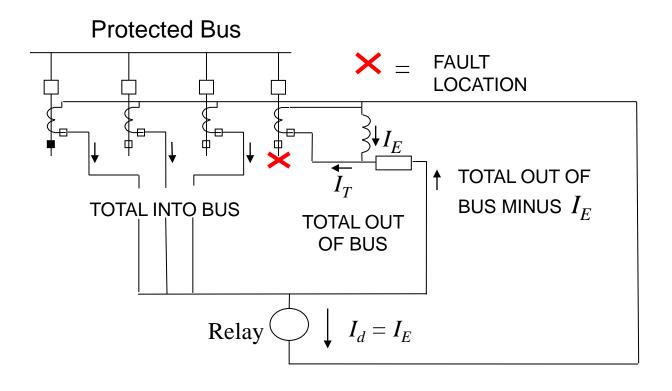


Differentially connected overcurrent relay



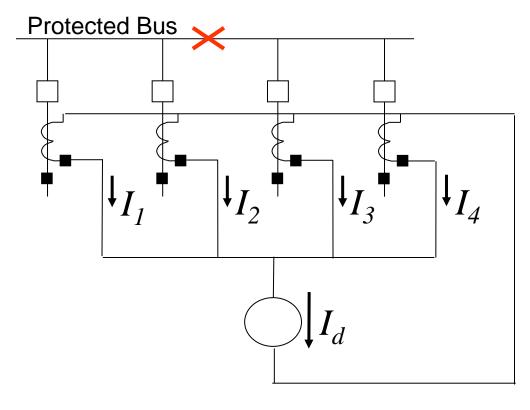


External fault case





Internal fault case

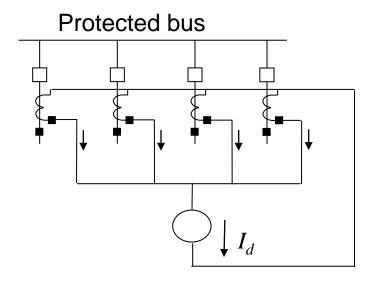


$$I_d = I_1 + I_2 + I_3 + I_4$$



Overcurrent relay bus differential

- Application OK if:
 - Symmetrical CT secondary current less than 100
 - Burden less than rated
 - Typical pickup setting I_{PU} > 10A
 - Trip delay greater than 3 x primary time constant (L/R)





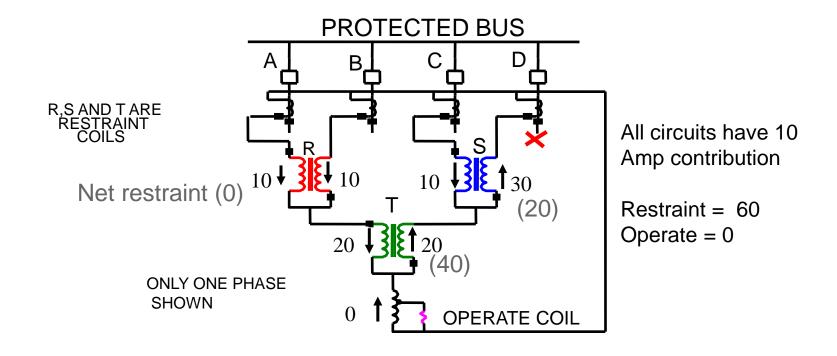
Resistor added to relay branch External fault

Total primary contribution to external fault I_F (out) through saturated ct $I_d = I_F(in) \cdot \left(\frac{R_S}{R_S + R_d}\right)$ $I_d = I_F(in) \cdot \left(\frac{R_S}{R_S + R_d}\right)$ I_F (in) total from other cts

- Resistor reduces current in relay and increases current in R_s (secondary and lead)
- Increases sensitivity to internal faults



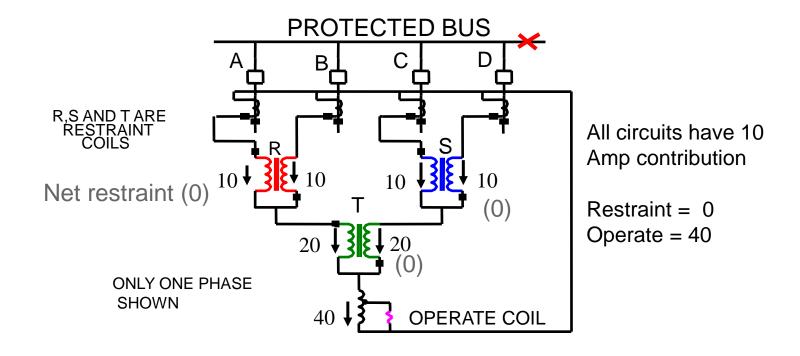
Multiple restraint Percentage Differential (Legacy)



External fault example – 4 circuit connection



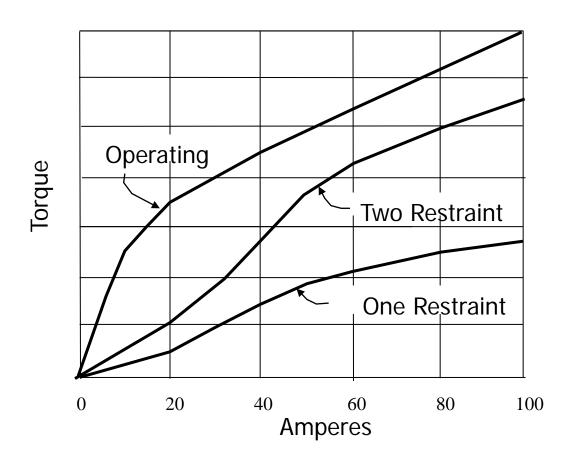
Multiple restraint Percentage Differential (Legacy)



Internal fault example – 4 circuit connection

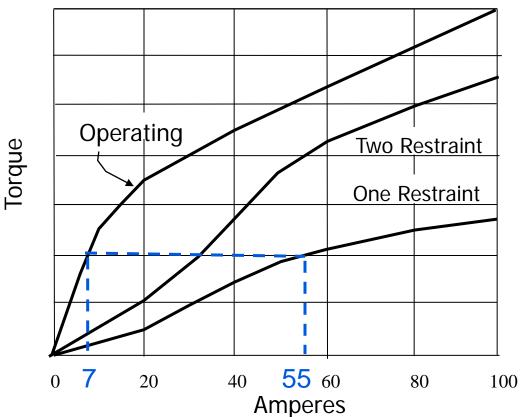


Torque for typical multi-restraint relay





Torque for typical multi-restraint relay



55 A. of restraint overcomes 7 A of operating current with one restraint winding



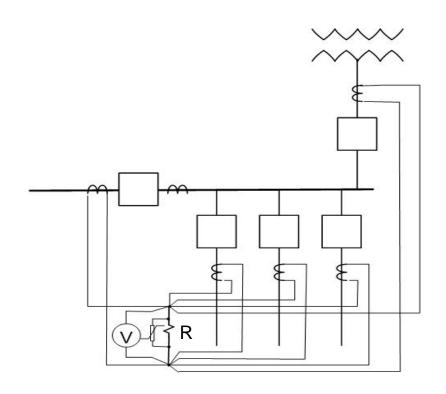
Multi-restraint percentage differential

- Good sensitivity
- Good security
- Allows other relays on the same CT core
- Different CT ratios with Aux CTs.
- Slow compared to high impedance
- Number of feeders limited by restraint windings
- Each CT is wired to relay
- Not easily extendable



High impedance bus protection

- High resistor (R > 1500 ohm) in series with relay coil and a MOV to prevent over-voltages
- High voltage develops for internal faults. lower Voltage will develop on external faults where with ct saturation
- Voltage unit must be set higher than the maximum junction point voltage for any external fault
- The lowest achievable sensitivity must verified for the application
- Proven reliability and very sensitive
- Operating times of less than one cycle for internal faults





High impedance bus protection

EXTERNAL FAULT - SECURITY Setting $V_R > (I_F / N) (R_L + R_S)$

K = margin factor

 $I_F = Max$ external fault current

 R_S = Ct secondary resistance

 R_L = Lead resistance to junction box

N = ct turns ratio

INTERNAL FAULT - SENSITIVITY

 $I_{M I N} = (XI_E + I_R + I_V) N$

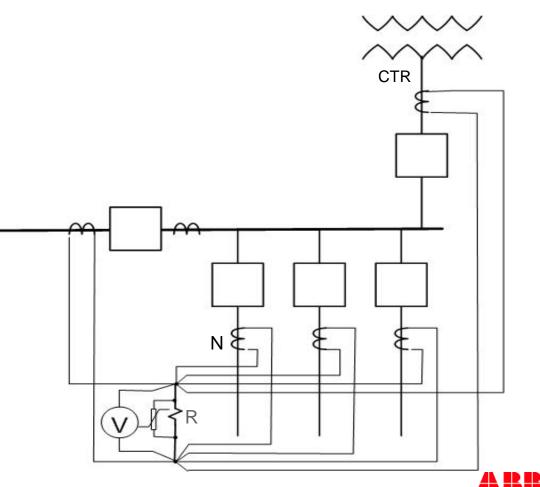
X = number of circuits

 I_F = Ct exciting current at V_R

 I_R = resistor current at V_R

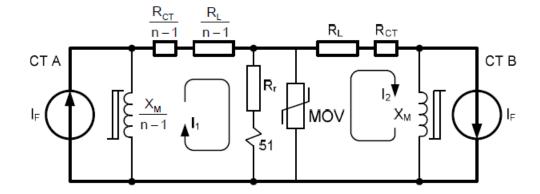
 I_V = Varistor current at V_R

R > 1500 W



High impedance bus protection Criteria to be met

- Objective: Keep V_R and I_{min} low
 - Ct secondary loop resistance kept low
 - Impedance from junction point to relay is of no consequence so good practice to parallel the CTs as close to the CTs as possible.
 - Theoretically no limitations in the number of parallel CTs but sensitivity reduced.
- All cts should have the same ratio and magnetizing characteristics



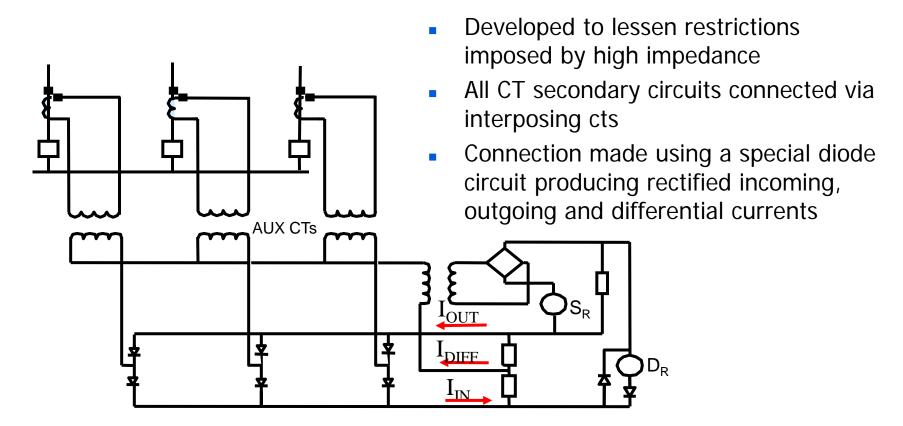


High impedance bus protection Criteria to be met

- Tapped CT's may be interconnected with fixed ratio ct's if attention is given to the autotransformer effect and the overvoltage protective characteristics of the relay
- A voltage setting higher than the lowest of all of the relaying accuracy class voltages of the CT's used in the scheme (400 V for a C400 CT). I_E obtained from the excitation character contains large errors
- Voltage setting can be lowered by reducing CT lead resistance

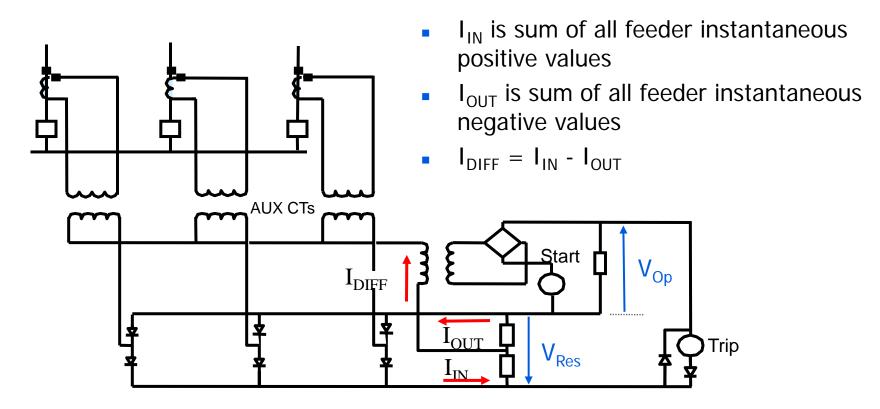


Differential comparator (Legacy, Static type) RADSS/REB103



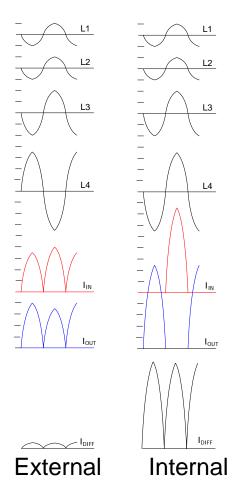


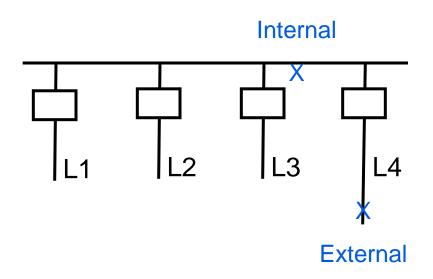
Differential comparator Single phase connection





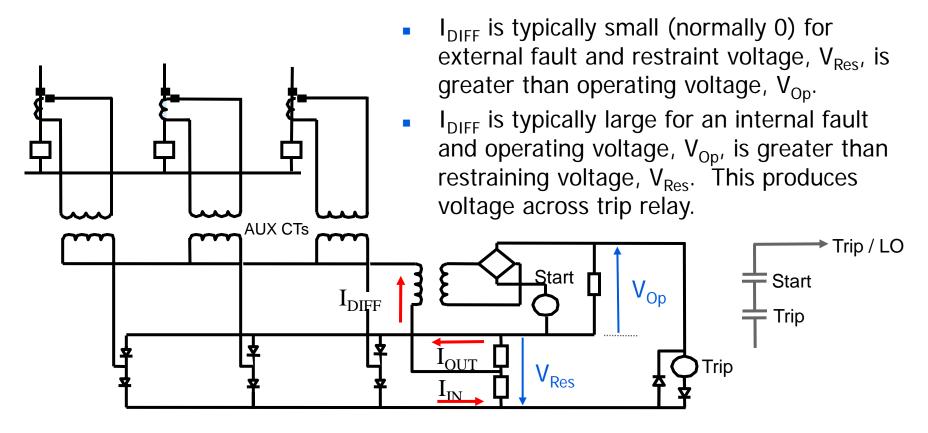
Differential comparator







Differential comparator Single phase connection





Differential comparator

- All measurement decisions based on three quantities
 - I_{DIFF} difference of input current and output current (I_{DIFF} = I_{IN} - I_{OUT})
 - I_{IN} total input current
 - S % differential setting
- $I_{DIFF} > S \times I_{IN}$
 - e.g. for setting S=50%, differential current ≥
 50% of incoming current before operation



Differential comparator Advantages over high impedance differential

- Lower ct requirements
- Allows much higher ct loop resistances
- Accommodate different CT ratios / auxiliary CTs
- Fast operating times for internal faults
 - Detects internal 1 3 ms
 - Before ct saturation

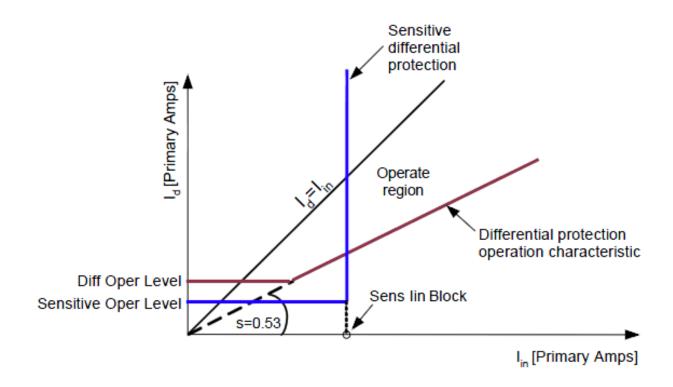


Numerical differential comparator

- Analog input currents are instantaneously sampled and quantized to numerical number
- Similar technique to legacy differential comparator, but with measured sampled data
- Secondary circuit loop resistance no longer a critical factor
- Critical factor is time available to make the measurement, i.e. time to saturation. (only 3ms required to properly restrain for heavy external faults)
- Algorithms for Ct saturation Detection and CT state supervision

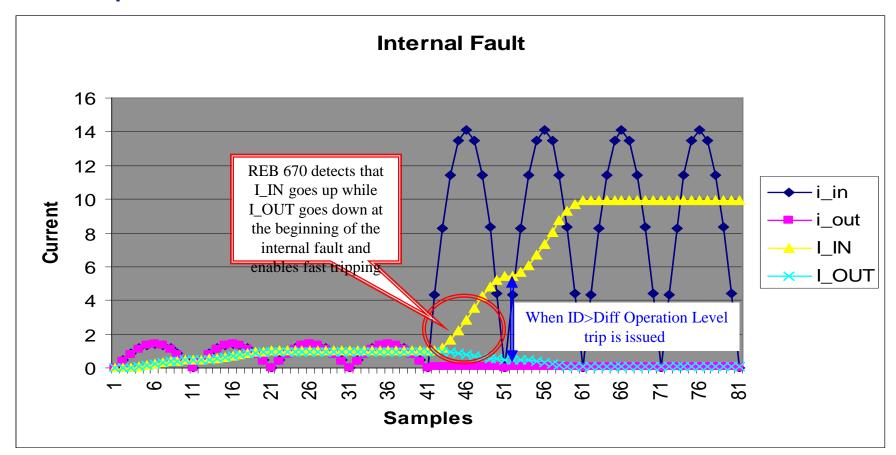


Differential comparator



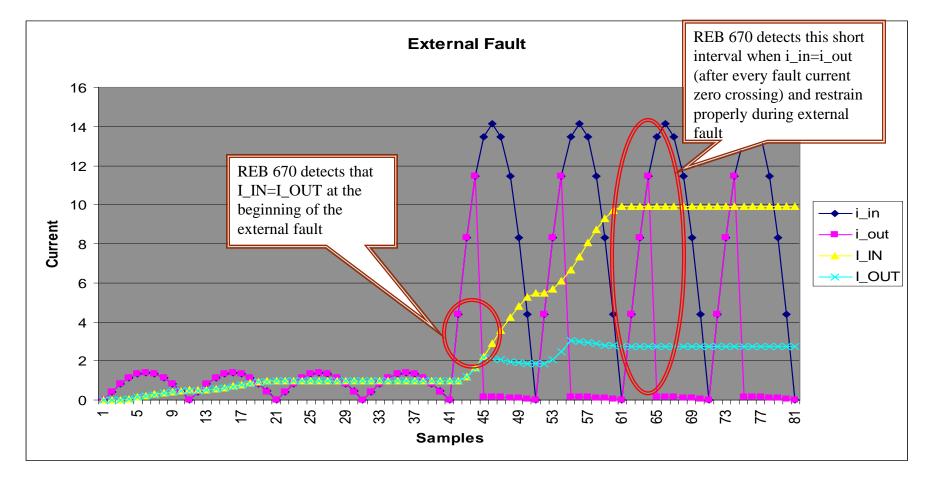


Quick operation for internal fault



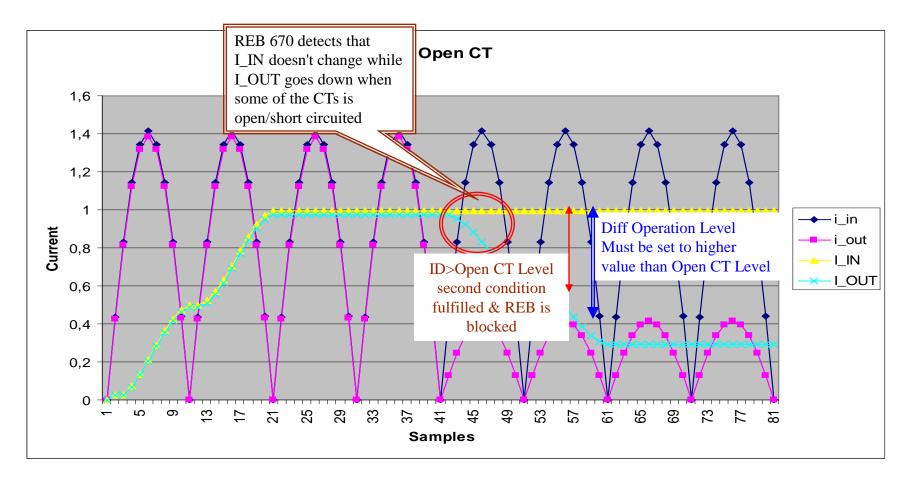


Proper & secure restrain during external fault





Fast open CT algorithm





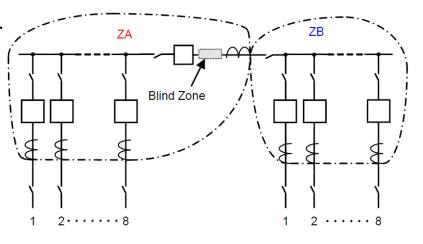
Other Features in Modern Numerical Bus IEDs

- Each device capable of connecting multiple bays (eg. CTs) in 3ph or 1-ph design
- Multiple differential zones, dynamic bay switching, zone interconnection, and check zone logics
- External fault/CT saturation detection, open CT detection algorithms
- Blind zone protection (see next 2 slides)
- End zone protection (see next 2 slides)
- Backup protection (eg. 50/51, 50BF) for each connected bay
- Modern substation automation communication (DNP 3.0, IEC61850)



Blind zone detection

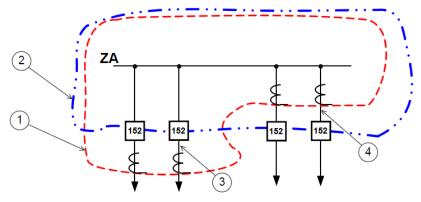
- Blind zone between live tank CT and breaker
- A fault in the blind zone makes operation in ZA unnecessary (tie breaker normally open)
- ZB cannot detect the fault
- Solution: connect BKR NC (open) status to the bay to remove this CT from ZA, ZB (software)
- Remove CT dynamically can force operation of ZB





End Zone Protection

- Regions not overlapped by both red and blue boundaries are blind zones
- CTs are used for both feeder and bus protection measurement (live tank CTs)
- Common in HV 1-1/2 stations
- Requires local backup (eg. BF) to trigger DTT for 3
- Requires remote back up (eg. zone 2) to open local breaker and disconnect the CT to clear bus zone for 4



where:

- is Busbar Protection measuring boundary determined by feeder CT locations
- 2 is Busbar Protection internal fault clearing boundary determined by feeder CB locations
- is End fault region for feeders as shown in figure 36/B
- 4 is End fault region for feeders as shown in figure 36/C

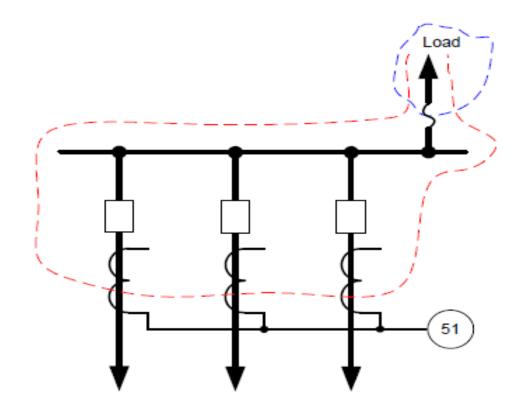


Other distribution (MV) bus protection methods

- Partial differential
- Blocking on feeder fault

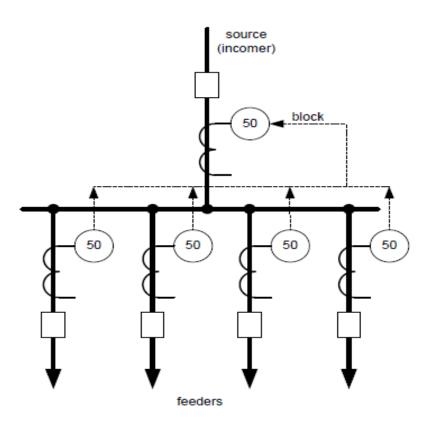


Partial differential



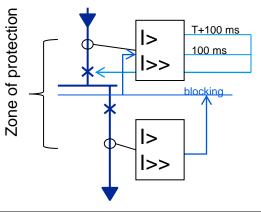


Blocking scheme





Conventional Blocking Scheme



Delay setting with inst. O/C protection (conventional approach)	
Safety marginal, e.g. delay in operation due to CT saturation.	2040 ms
O/C protection start delay + output relay's delay	<40 ms
Start delay with receiving relay + retarding time for the blocking signal *)	<40 ms

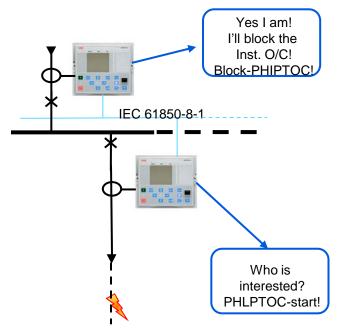
100...120 ms

- Traditional busbar protection based on upstream blocking
 - Dedicated hard-wire signal paths needed
 - Signal path delay needs to be considered, input and output delay + auxiliary relays
 - Changes in the protection scheme may require rewiring
- Typical needed delay in incoming relay is over 100 ms



ALL TOGETHER

Blocking Scheme with IEC-61850 GOOSE



Delay setting with inst. O/C protection (REF615 GOOSE approach)	
Safety marginal, e.g. delay in operation due to CT saturation.	2040 ms
O/C protection start delay	20 ms
Retardation time of inst. O/C stage blocking	5 ms
GOOSE delay (Type 1A, Class P1)	<10 ms
ALL TOGETHER	5575 ms



Bus protection comparison chart

	COST	EASE OF USE	SENSI- TIVITY	DEPEND ABILITY	SECURITY	FLEXI- BILITY	SPEED
SIMPLE OVER- CURRENT	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
MULTIPLE RESTRAINT	MED	POOR	BEST	GOOD	GOOD	POOR	GOOD
HIGH IMPEDANCE	MED	GOOD	GOOD	GOOD	BEST	GOOD	FAST
PERCENTAGE RESTRAINED DIFFERENTIAL	HIGH	BEST	GOOD	GOOD	BEST	BEST	BEST
PARTIAL DIFFERENTIAL	LOW	GOOD	POOR	GOOD	GOOD	GOOD	POOR
BLOCKING	MED	GOOD	POOR	GOOD	GOOD	GOOD	FAST



Questions? Recommended reading

 ANSI C37.234 Guide for Protective Relay Applications to Power system Buses



Relion® REB650/670 Advanced Busbar Protection Reliable protection and control of busbars



One IED for a wide range of high impedance differential protection applications



REB670 State of the art protection for medium to extra high voltage levels

- Selective, reliable and fast fault clearance for all types of internal phase-to-phase and phase-to-ground faults in solidly earthed or low-impedance earthed power systems
- Significant savings in configuration and commissioning with efficient system integration and optimum "off-the-shelf" solutions and settings
- Do more with less the advanced logic and multipurpose functionality allow you to customize protection schemes for multiple zones with a single IED
- Maximize flexibility and performance with powerful application and communication capabilities that allow you to integrate these IEDs into new or retrofit substation automation systems or use them as stand-alone multifunctional units



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