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ISPS, September 2010, Prague, Czech Republic

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Abstract

An advanced Reverse Conducting (RC) IGBT concept referred to as the **Bi-mode Insulated Gate Transistor (BIGT)** has been previously documented mainly for high voltage devices rated at 3300V. In this paper, we report on the progress made to implement the new technology for lower voltage classes rated below 2000V which would require complex thin wafer processing for the design realization. The paper covers mainly the process challenges met to introduce the BIGT into the lower voltage class and present the latest test results of the first thin wafer 1700V/150A prototype BIGT in both IGBT and diode mode of operation.

Keywords: BIGT, Thin Wafer.

INTRODUCTION

The traditional goal for a Reverse Conducting (RC) transistor having an integral diode is to obtain higher power for a given footprint package area by eliminating the need for a separate anti-parallel diode [1]. This approach has been demonstrated experimentally in recent years for medium voltage IGBTs (600V-1200V) mainly operating at low currents and/or soft switching conditions [2][3]. A 3300V RC-IGBT concept was presented [4] to demonstrate the feasibility of such technology for higher voltage devices. A new advanced reverse conducting IGBT device concept referred to as the **Bi-mode Insulated Gate Transistor (BIGT)** was also presented [5] which mainly targets to fully replace the state-of-the-art two-chip IGBT/Diode approach with a single BIGT chip. This is achieved for hard switching applications while also being capable of improving on the over-all performance especially under hard switching conditions with low losses, soft switching characteristics and high SOA. The high voltage BIGT development has resulted in a clear breakthrough in device performance by adopting an advanced shorted collector backside layout design, optimum doping profiles and controlled lifetime reduction for enabling optimal operation in both IGBT mode and diode mode. In this paper, we demonstrate the BIGT technology for the first time on the medium to lower voltage classes where thin wafer processing is required for optimum loss performance.

The BIGT Concept

The BIGT consists of a hybrid structure integrating an IGBT and an RC-IGBT into a single chip as shown in figure (1).

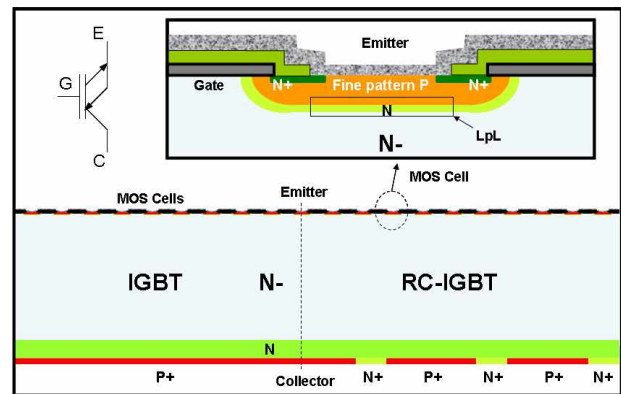


Fig. 1 BIGT basic structure

The main target of this combination is to eliminate snap-back behavior at low temperatures in the BIGT transistor on-state mode by ensuring that hole injection occurs at low voltages and currents from the P-type collector region in the IGBT section of the BIGT. The backside layout design and dimensioning of the IGBT region is also optimized to

- 1- Provide smooth transition into full chip conduction as the RC-IGBT section will also provide holes at higher currents.
- 2- Maximize and independently optimize the RC-IGBT area for diode conduction.
- 3- Ensure that the BIGT utilizes the whole chip during transistor conduction for providing the same technology curve as for a state-of-the-art IGBT chip.
- 4- Minimize any current non-uniformities especially during switching due to the integrated structure.

The BIGT concept has resulted in a better trade-off between the above mentioned parameters compared to the standard RC-IGBT design.

BIGT Thin wafer Processing

The introduction of the required structures, implants and anneals for thick high voltage BIGTs (>200um) is relatively straightforward and can be implemented at different stages during device processing. This provides a flexible approach for optimizing the different device parameters in the complex BIGT design. The main process parameters include the P-type and N-type regions dimensioning, dopants implantation doses and activation for providing the required injection efficiencies needed for optimum performance.

For the realization of lower voltage BIGTs on thin wafer (<200um) technologies, many process challenges must first be met. The main reason is due to the fact that the backside processing must be carried out after completing the front-side emitter and termination processes and thinning the wafer to its final intended thickness. This in turn provides many handling and thermal budget limitation for further processing.

For such a process, the device front side termination/passivation and (emitter) MOS structure/metallization processes are completed on a relatively thick wafer. Following this, the device is then grinded and polished to its intended final thickness. In a normal IGBT, only a backside anode P-type implant and subsequent metallization and thermal anneal is carried out for the anode activation and metal sintering. This anneal is normally limited to temperatures below 500°C for not affecting the front side metallization.

For the BIGT, extra processing steps immediately after thinning are required to define the backside in order to introduce the shorted anode structure containing both P-type and N-type regions. The shorted anode results in weaker anode injection efficiency and higher on-state losses in the IGBT mode. Hence higher temperatures are required for the P-type activation. On the other hand, the N-type regions would also require sufficient activation to establish a good ohmic contact for the diode mode operation. Furthermore, it is beneficial to attempt to decouple the two regions for optimum definition of dopant activation.

To achieve the above requirements, two special processes were implemented. The first process consist a defined high dose P-type boron implantation on the full backside before structuring. This is followed by applying the mask for defining the shorted N-type regions in the RC-IGBT part of the BIGT. A very shallow etch process through the mask is implemented to remove the boron implant layer followed by the N-type Phosphorous implant. In this way, both implants will not suffer from any compensation

effects, which is critical for such thin pn-junctions. A SEM cross-section of the BIGT backside is shown in figure (2) to visualize the resulting structure.

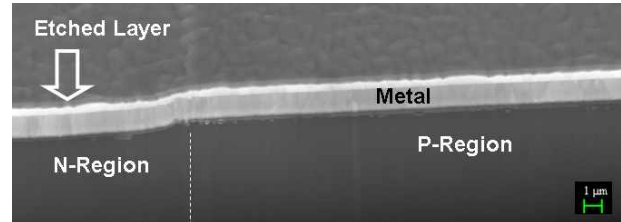


Fig. 2 SEM cross-section of the BIGT backside.

The backside is then exposed to high energy laser anneal for the dual activation of both the P-type and N-type regions to the required levels. The laser -anneal process enables finely defined high temperatures for very short times (100s of nanoseconds) at the silicon surface without exposing the wafer frontside. To demonstrate the activation effect, figure (3) shows the doping concentration profiles of a boron implant activated using both a low temperature sinter process (<450°C) and a high energy laser anneal.

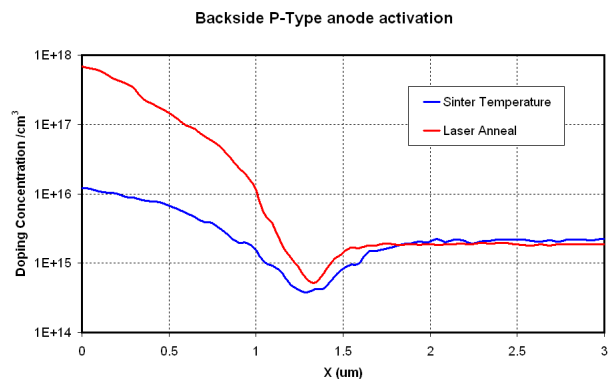


Fig. 3 Backside thermal activation of P-type layer.

The first 1700V prototype samples with a final thickness of 190um have been produced to demonstrate the feasibility of such processes for thin wafer technology BIGT.

1700V / 150A BIGT Prototypes

A 1700V/150A BIGT chip (13.6mm x 13.6mm) was manufactured based on a Soft-Punch-Through (SPT) buffer design and Enhanced Planar (EP-IGBT) concept [6]. The EP technology having NO highly doped and deep P+ well regions while exhibiting a compensation effect due to the additional enhancement N-layer (figure.1 top) have provided the BIGT with a fine pattern p-well profile

which ensures low injection efficiency for optimum diode performance. In addition, a Local p-well Lifetime (LpL) control technique utilizing a self-aligned and well defined large particle implantation ensures improved diode recovery without influencing the transistor loss trade-offs and leakage current levels. Finally a local lifetime control layer using proton implantation is added for further reducing the diode mode losses. This would normally result in a slight increase in the IGBT mode on-state losses.

Using high energy pulse laser annealing and low temperature sintering for varying of the anode P-type doping, three BIGT design were provided for the IGBT mode technology curve (V_{ce} vs. E_{off}) as shown in figure (4). Point (C) represents the sintered version while point (A) and (B) represent two laser anneal energies. The laser anneal provides a wide activation range for an optimum device loss trade-off design.

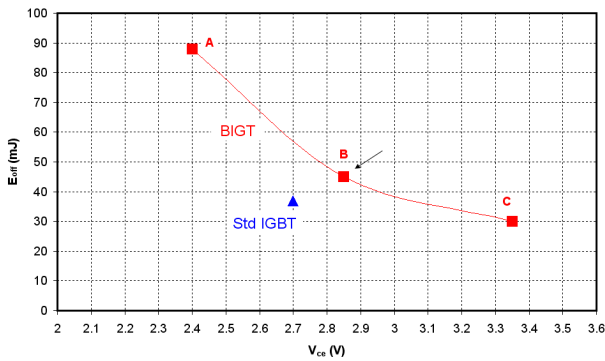


Fig. 4 1700V BIGT technology curve (900V, 150A, 125°C)

The device exhibits a slightly higher loss technology curve compared to an equivalent standard IGBT (without backside structuring) due to the added proton irradiation. The effect of the introduced N-type shorts on the technology curve is clear resulting in the need for higher activation to operate the device in a low on-state technology point close to the standard IGBT. Therefore, device (B) will be the focus for the electrical test in the following sections.

1700V / 150A BIGT Electrical Performance

First, the forward characteristics of design (B) of the BIGT in both IGBT (solid line) and Diode mode (dotted line) are shown in figure (5). At 150A and 125°C, the $V_{ce(sat)}$ of the IGBT mode is around 2.85V and the V_F in diode mode is 2.65V. Further optimization will still be required to further enhance the on-state curves in both modes of operation at lower current and temperatures due for smoother transition into full chip conduction.

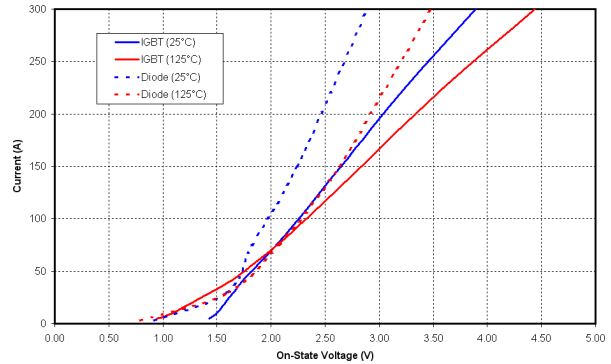


Fig. 5 1700V BIGT (design B) on-state characteristics at 25°C and 125°C.

The switching characteristics are also presented here for the 1700V BIGT design (B) version. The nominal turn-off and turn-on waveforms are shown in figures (6) and (7) respectively. The nominal test conditions were set to 150A, 900V at 125°C. The diode reverse recovery mode of the BIGT is clearly seen mirrored in the current waveform during turn-on. The switching losses under nominal conditions are around 45mJ during turn-off and 80mJ during turn-on.

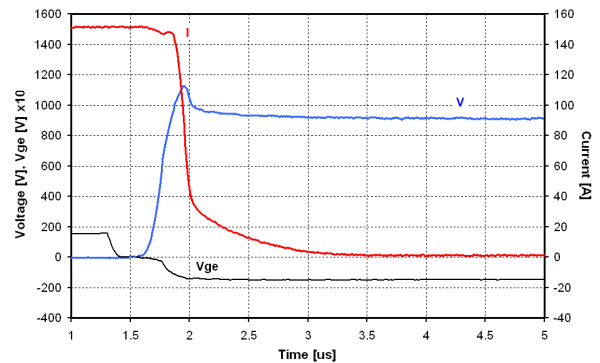


Fig. 6 1700V BIGT (design B) nominal turn-off (900V, 150A, 125°C).

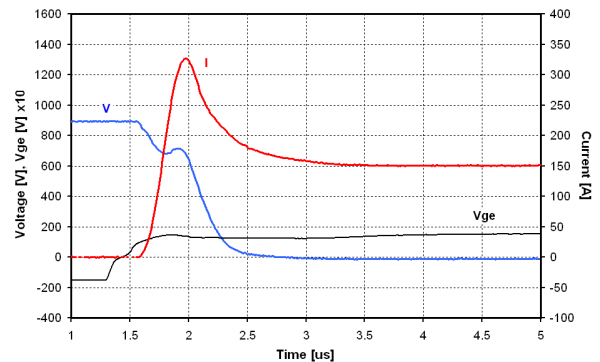


Fig. 7 1700V BIGT (design B) nominal turn-on (900V, 150A, 125°C).

The turn-off SOA of the BIGT under extreme conditions is shown in figure (8) at 125°C, 1450V and 750A and a stray inductance of 160nH. This current level represents 5 times the nominal current for demonstrating the robust performance of the 1700V BIGT chip. Immunity to strong dynamic avalanche is also observed due to the rugged IGBT cell structure. The device is also able to withstand a very high overshoot voltage of 1850V which exceeds the 1700v device rating.

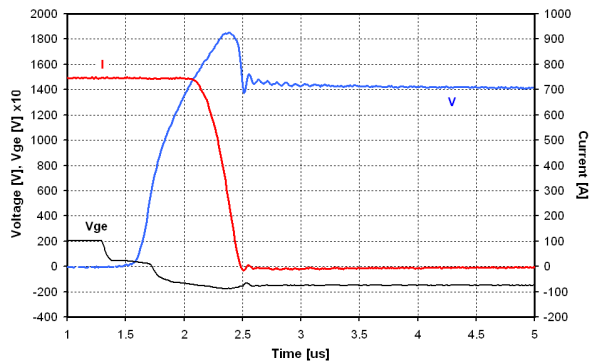


Fig. 8 1700V BIGT (design B) turn-off SOA (1450V, 750A, 125°C)

Finally, the short circuit performance of the BIGT at 1300V and 125°C is shown in figure (9). The device was subjected at 125°C to a 10usec pulse at 1400V. The short circuit current level is close to 4 times the nominal value having a controllable and smooth current waveform for the whole duration.

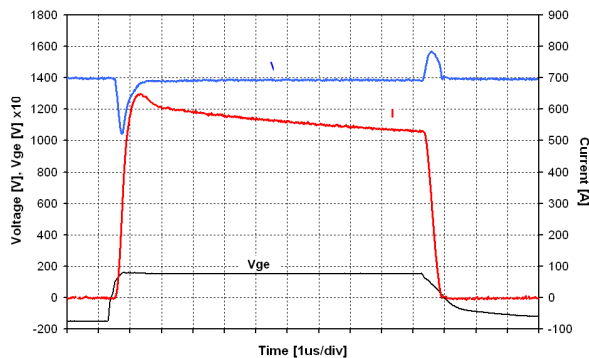


Fig. 9 1700V BIGT (design B) Short Circuit (1400V, 125°C).

The BIGT Impact on Future Applications

As discussed previously, the main aim of the BIGT technology is to provide higher power density than conventional devices for future applications. An expected 30% increase in power density is expected depending on the device design and application requirements.

Furthermore, due to the fact that the IGBT and Diode operational modes share the same silicon area, there are no more inactive periods for the silicon and thus temperature ripples are reduced. Therefore, the BIGT has the potential to minimize the ongoing reliability concerns for classical IGBT modules exhibiting a relatively limited ΔT temperature cycling capability due to the low output frequency. Fig. 10 illustrates the expected thermal cycling pattern in a BIGT application where no inactive periods are present per IGBT/Diode compared to the standard approach. This will lead to better thermal utilization of the module and eventually improved reliability performance due to a better thermal cycling capability. This feature will also enable a more reliable chip operation at higher junction temperatures.

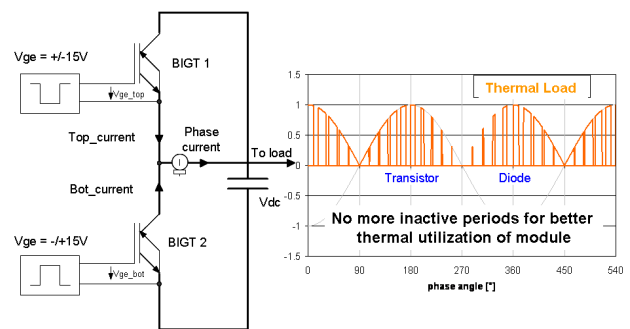


Fig. 10: BIGT thermal load cycling in PWM applications.

CONCLUSIONS

The BIGT concept on thin wafer technology has been introduced and experimentally demonstrated. Electrical data at chip level for a 1700V/150A BIGT prototype were also presented showing that the BIGT concept can provide exceptional electrical performance and has the potential of achieving higher power densities in future applications.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the help of R. Jabrani, W. Janisch, E. Faggiano, E. Nanser and K. Ruef for device processing and analysis.

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