Thin Silicon Wafer Device Concept

with Advanced Laser Annealing and Sintering Process

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Abstract

A new anode/cathode design and process concept for thin wafer based silicon devices is proposed to achieve the goal of providing improved control for activating the injecting layer and forming a good ohmic contact. The concept is based on laser annealing in a melting regime of a p-type anode layer covered with a thin titanium layer with high melting temperature and high laser light absorption. The improved activation control of a boron anode layer is demonstrated on the Soft Punch Through IGBT with a nominal breakdown voltage of 1700 V. Furthermore, the silicidation of the titanium absorbing layer, which is necessary for achieving a low $V_{CE\,ON}$, is discussed in terms of optimization of the device electrical parameters.

Keywords: silicon, diode, IGBT, laser annealing, laser sintering.

INTRODUCTION

The IGBT evolved over the past 20 years from epitaxial based Punch-Through (PT) type structures into Non-Punch-Through (NPT) structures [1]. The NPT devices offered a wide range of advantages in terms of the switching capability and current sharing of the chips which enabled the employment of a large number of paralleled IGBT chips into high current modules. Nevertheless, due to the relatively thicker base region designs required for the NPT concept, devices suffered from higher static and dynamic losses. The introduction of the thinner Soft-Punch-Through (SPT) or Field-Stop (FS) concepts brought about major improvement in terms of reduced overall losses [2]. Similar structures were also employed in the latest diode designs.

However, the SPT/FS concepts require complex processes especially for 600V, 1200V and 1700V rated devices when the wafer is very thin (< 200um) for forming the backside layers including the anode and buffer regions. In many cases the process temperature is limited to below 500°C due to the completion of the front side processes on a thicker material which include the emitter metallization and the device passivation. This restricts the capability to control the activation levels of the anode layer and for forming good silicon/metal ohmic contacts after the thinning process is completed. Therefore, for such devices, the losses optimization is being limited for achieving improved static and dynamic performance for a given application and operating frequency.

In recent years, such challenges are met with advanced laser thermal annealing (LTA) processes [3] for fine control of activation of the anode and buffer of the IGBT without affecting the front side of the wafer. Nevertheless, a number of issues remain challenging for this approach including higher energy density levels delivered by the laser beam which remains difficult and also produce silicon surface defects, plus the formation of good ohmic contacts after activation and metal deposition [4]. In addition, the process is limiting for implementing structured backside designs as required in modern concepts such as the BIGT (Bi-mode IGBT) and FCE (Field Charge Extraction) diode concepts. This paper describes a new process for the activation of the p-type anode and sintering of the contact stack for a thin wafer IGBT by using the LTA for improved process capability and device performance when compared to prior art.

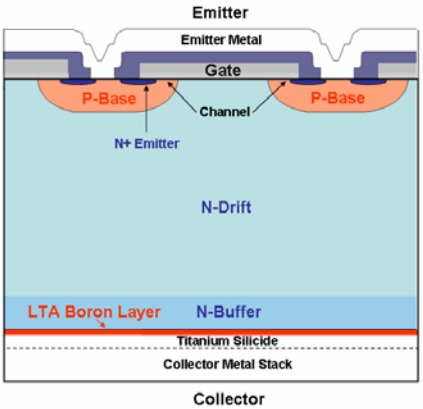

Fig. 1. Schematic cross-section of the IGBT (not to scale).

The advantage of the LTA technology is that it significantly limits the induced thermal budget to the surface of very thin devices [4] [5] [6]. The fact, that the activation cannot be applied at the same time over the whole wafer is overcome by performing the LTA in a melting regime while stepping the single laser shot over

the whole wafer surface. With this approach, the necessary overlapping of neighboring areas exposed to the laser shots does not impact the required homogeneity of dopant activation [4].

However, for a higher dopant activation, which is needed for a lower $V_{CE\,ON}$ of IGBTs, higher LTA energy densities are needed (> 3 J/cm^2). At such densities, both the size of surface defects and the stability of the laser tool become a limiting factor. Also the increased beam reflection from the molten silicon surface causes the saturation of dopant activation with energy density and the $V_{CE\,ON}$ cannot be further improved. To overcome this problem, a thin titanium layer, which absorbs the laser light better than silicon, is deposited at the surface before the LTA process. The achieved improvements in dopant activation and subsequent lowering of $V_{CE\,ON}$ including process optimization are presented below.

EXPERIMENTAL

In today`s low voltage IGBTs with ratings below 2 kV, the device backside is implanted after thinning for forming the p-type layer followed by multi metal depositions. Finally a sinter process is carried out below 500°C in a conventional furnace to activate the anode and form a good ohmic contact. This process, which is named as “Prior Art” in Tab.2, is limiting for achieving good control of the p-type anode activation [7] [8].

The new process for achieving a greatly improved activation of the IGBT anode (typically boron) is shown in Tab.2 at right. The LTA step is performed after a thin layer (≤ 100 nm) of Ti is deposited on the p-type silicon surface (Tab.2, step #4, right). This step is missing in the classical approach (left). Depending on the energy density of the LTA process, the titanium layer undergoes the process of silicidation in order to provide a good ohmic contact. As the resulting layer of titanium disilicide $TiSi_2$ can be left as a part of the contact stack, it does not complicate the already delicate thin wafer process.

The device under test is a planar IGBT with an SPT buffer rated at a breakdown voltage of 1700 V and nominal current of 75 A [2][7][8]. After the front-side processing of the IGBT termination and emitter cell / MOS part, the wafers are grinded and etched to a well defined final thickness for the backside boron implantation to be performed (Tab.2). In the novel devices (Tab.2 right), the Ti layer of various thicknesses is sputter deposited following the boron implantation. The high energy UV laser system with $\lambda = 308$ nm, energy densities up to 5 J/cm^2 and pulse durations below 200 ns is used for the LTA of the boron layer and the silicidation of the Ti layer. The metal stack is then deposited (Al, Ti, Ni, Ag) and sintered in a classical way in a sintering furnace.

The Ti layer is chosen due to the fact that the Ti in principle absorbs the laser beam (heat) much more than the melted silicon surface, hence a better activation of boron is achieved with lower laser energy densities. Furthermore, the Ti provides about 300 ^oC higher melting point than silicon. It is important since the very short laser pulses (for example 200ns) with high energy density (≈2 J/cm2) will bring the Si into the melting regime, but without a substantial vapor pressure to create vapor bubbles in silicon. There are further good reasons for the usage of titanium:

1. The titanium is capable of providing a good contact silicide layers with silicon.
2. The silicidation process is not sensitive on the existing native oxide at a silicon surface.
3. The reaction between aluminum and titanium silicide does not lead to the formation of inter-metallics of aluminum, which would otherwise affect the electrical characteristics and the stability of the silicide [9].

The last item means that there is no cause for concern about the integration of the titanium absorbing layer into the standard metal stack (Al, Ti, Ni, Ag).

A. Prior art	**B. New process**
1. Front side (MOS part) processing	
2. Device thinning	
3. Boron implantation optionally with N-buffer implantation	
Not applied	4. Titanium deposition sputter (t ≤ 100 nm)
Not applied	5. Laser Annealing (LTA) & Laser sintering for $TiSi_2$ from Fig.1
6. Metal stack deposition	
7. Sintering	

Tab. 2. Classical (left) and new (right) process flows.

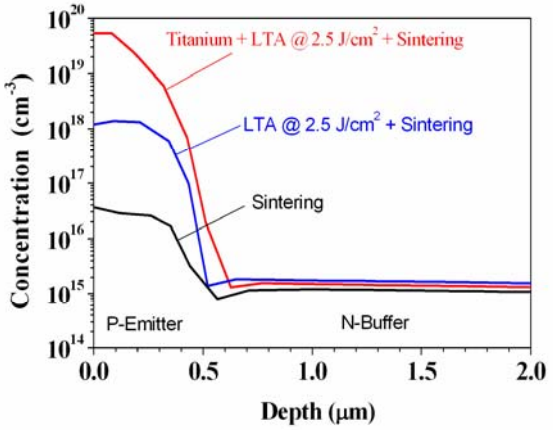

Fig. 2. Doping profiles for classical activation by during Sintering, activation by LTA and LTA using Titanium absorber layer (measured by Spreading Resistance technique).

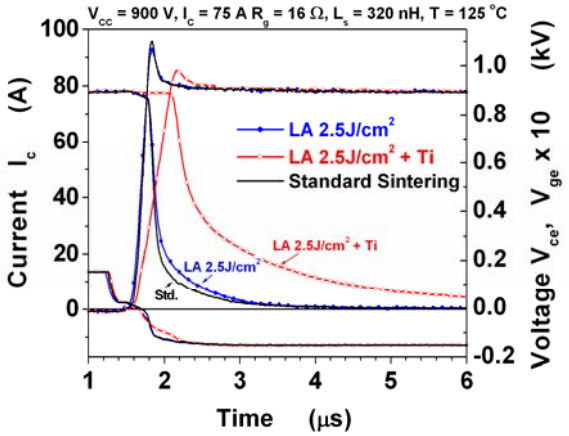

Fig. 3. 1700V IGBT turn-off (900V, 75A, 125°C) for devices with doping profiles from Fig.2 tested at nominal conditions. Notice that the standard LTA process provides devices with parameters not far away from that of the standard sintering activation.

RESULTS AND DISCUSSION

Fig.2 shows that the activation level of boron can be increased about 50 times for the laser energy density of 2.5 J/cm^2, if the Ti absorbing layer is used. While the LTA improve the boron activation about 20 times over that of the classical furnace sintering, the improvement of the boron activation due to the LTA with the Ti absorber is about three orders of magnitude. This gives a significantly increased operation space for the IGBT design, where one can use also lower energy densities. However, it must be done with care, because there is a limit from which the silicidation stops to give an optimal titanium silicide.

The switching IGBT turn-off waveforms are presented in Fig.3 showing the higher turn-off charge of the IGBT with the proposed new process, which provides higher injection levels when compared to state-of-the-art. This is also clearly illustrated in the technology curve shown in Fig.4 together with the reduction of the $V_{CE\ ON}$ by 20% against the standard LTA process with the Ti absorber for the energy density of 2.5 J/cm^2.

For the novel device, the thickness of the Ti layer after sputtering (t_{Ti}) is shown as a parameter in order to emphasize its importance for device electrical parameters. Fig.4 shows that a thinner titanium layer brings a lower $V_{CE\ ON}$ than the thicker one. This effect can be explained by a lower consumption of the silicon by the titanium when a thinner titanium layer is used for the laser sintering (silicidation). For example, the 100 nm titanium layer consumes during the silicidation process approximately 220 nm of silicon, which is already a significant portion of the boron layer.

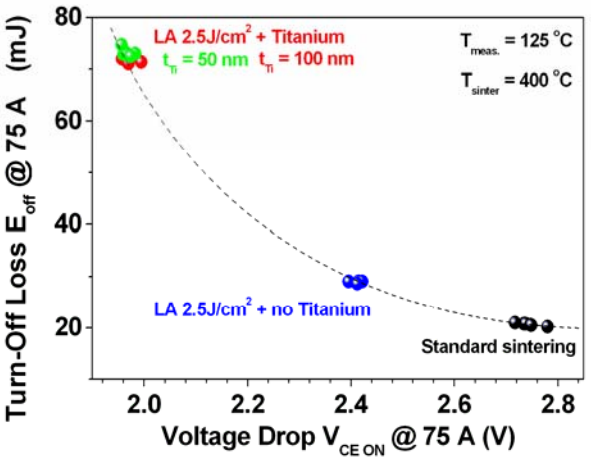

Fig. 4. Technology curve E_{OFF} vs. $V_{CE\ ON}$ for 1700V IGBTs from Figs.2 and 3 tested at nominal conditions.

The reduction of the titanium thickness has been found to bring not only a better activation of the boron layer, but also a lower density of protrusions of titanium under the original silicon surface (see Fig.5) and hence a lower leakage current of resulting devices. On the other hand, the existence of protrusions has been found to be important for the achievement of the low $V_{CE\ ON}$. The devices without protrusions, which resulted from the LTA at energy densities at 1 J/cm^2 and lower, have shown the values of $V_{CE\ ON}$ higher than that of the standard process. This means that the protrusions, which are the product of constitutional supercooling during the solidification process of the LTA [10], are needed to obtain the superior values of the $V_{CE\ ON}$ shown in Fig.4.

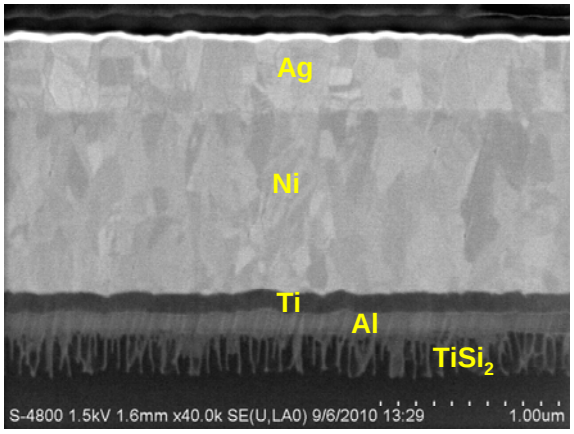

Fig. 5. SEM cross-section of the novel device laser annealed with 50 nm thick Ti absorber using the laser energy density of 2 J/cm^2. The protrusions of the titanium disilicide are extending from the aluminum layer

The behavior of the $TiSi_2$ at the periphery between the metal stack and silicon bulk is analogous to the case of homogeneous layer presented above.

The new process can also be employed for improved activation of n-type cathode layers for diode. In addition, it can be used to structure the backside of thin wafer devices as needed for implementing the FCE diode concept or reverse conducting IGBTs. This is achieved while providing different activation levels using the same laser energy density for optimizing the performance [11].

CONCLUSIONS

A new process concept for silicon power devices fabricated at thin wafers was presented for fabricated thin wafer IGBTs. The concept is based on laser thermal annealing of a p-type anode layer of an IGBT covered with a thin titanium layer for increased absorption of the ultraviolet laser light. The controlled activation of the anode was achieved while forming at the same time a good ohmic contact by means of laser sintering. The influence of the thickness of the titanium layer on device electrical parameters was also shown.

The improvement of the ON-state voltage drop $V_{CE\ ON}$ of the 1700 V IGBT was achieved, which is not possible by other means without a deleterious effect on the MOS part of the IGBT.

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