Paralleling of modules or paralleling of inverters becomes necessary, if a desired inverter rating or output current can not be achieved with a single IGBT module as switch.
From an economic point of view paralleling of modules is in many cases the solution of choice. On the other hand it is a technical challenging task to ensure proper current sharing between the parallel connected modules.
This application note shades light on the technical measures which help to ensure a homogenous current sharing within the parallel connected power modules. Homogenous current sharing is also the key to maintain high ruggedness of the whole converter and it allows an optimal utilisation of the power modules with minimal de-rating.
1 Introduction
In an ideal case the current capability of IGBT modules scales with the number of modules connected in parallel. Due to a never completely matched impedance of each module connection and due to parameter variations between the different modules a perfect current sharing is not realistic. In addition unequal cooling of the semiconductor devices can lead to further current imbalance in and between the modules since the semiconductor on-state and switching characteristics are temperature dependent. This application note deals with the influence parameters for static and dynamic current sharing and shows the impact on current imbalance between the parallel connected modules and consequential influence on the junction temperature.

2 Static current sharing
The static current sharing is influenced mainly by the difference of the connection resistance and the on-state characteristics of the parallel connected modules.

2.1 Influence of the module parameter spread
Figure 2 shows the IGBT-on state voltage distribution of a production time of roughly one year for one product. The median $V_{CEsat}$ of the population is at 5.4 V and the standard deviation is 0.065 V. In order to statistically evaluate the current sharing of two parallel connected modules $V_{CEsat}$ of roughly 4000 measured modules was randomly grouped into a total of 200 pairs. Figure 3 shows the probability plot of the $V_{CEsat}$ difference of the paralleled IGBT modules. The random grouping of the modules out of the population shown in Figure 2, yields in a median $V_{CEsat}$ difference of 65 mV and a maximum difference of 265 mV.

More important than the voltage difference, is the resulting current imbalance between the paralleled modules.

In order to calculate the current in the modules a linear approximation of $V_{CEsat}$ versus $I_C$ was assumed between nominal current (600 A) and 1/3 of the nominal current (see also Figure 1).

$$ V_{CEsat}(I_C) = V_{TO} + I_C \cdot r_{CE} $$

Eqn. 1

As a simplification the threshold on-state voltage ($V_{TO}$) at zero amps was set to 2.5 V. This is quite close to the reality since most of the process variations influence more the resistive part of the characteristics and only minor the $V_{TO}$. Evaluating only the current imbalance due to the module variation, (assuming the worst case of zero connection resistance) both paralleled modules must see the same voltage drop. Running two paralleled modules at twice the nominal rating of a single module will cause a common voltage drop of the average $V_{CEsat}$ of the two modules at its nominal current (in the example 600 A per module). Thus the resulting module current in each module can be calculated.
based on its on-resistance \( r_{CE(n)} \):

\[
I_{C(n)} = \frac{V_{CEsat(1)} + V_{CEsat(2)} - V_{f0(n)}}{2} \frac{1}{r_{CE(n)}}
\]

Eqn. 2

The current imbalance between the paired modules from Figure 3 is expressed as the maximum collector current minus the average current, divided by the average current (in this example 600 A). The probability plot of the current imbalance of two paralleled modules is shown in Figure 4. The median current imbalance is 1.1 % and the maximum observed current imbalance was 4.5 %.

The current sharing shown in Figure 4 is what can be expected if modules from a large production period (one year) are randomly grouped in to pairs, excluding the influence of possible inhomogeneous cooling and connection resistance. A further improvement in static current sharing can be achieved if the modules for parallel connection are specifically selected based on its on-state voltage \( V_{CEsat} \) or if modules from the same production lot (narrower parameter spread) are used. Figure 5 shows the current imbalance as a function of the on-state voltage difference.

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Figure 6 shows the on-state characteristics for 25 and 125 °C of a 6500 V 600 A IGBT. Obviously if one module would be operated at 25 °C and the other module at 125 °C, the cooler module would take a much larger share of the total current. Though thanks to the positive temperature coefficient the current sharing in reality would improve since the higher current in the cold module would cause a higher temperature and vice versa for the hotter module. So in short time the current sharing would stabilise. Nevertheless homogenous cooling with the same in-let temperature of the cooling medium for both module heat-sinks is crucial. Especially for the diode operation mode, since the diode on-state characteristic does not offer necessarily a positive temperature coefficient over the full current and temperature range. Last but not least also the gate voltage supplied by the gate-unit has an influence on the on-state characteristic of the IGBT. It is thus important that the gate-voltages are narrowly matched for all parallel connected IGBTs or that the same gate-voltage supply is used.

### 3 Dynamic current sharing

Dynamic current sharing depends largely on the external power circuit design. Especially during the turn-on process different emitter impedance values to the common point of the commutation loop have a strong influence since the gate-voltages of the paralleled IGBTs are directly affected if a common gate-driver for all modules is used. If individual gate drivers are used, proper matching and narrow parameter spread between the drivers is crucial.

#### 3.1 Common Gate-Drive

Figure 7 shows a simplified schematic of a parallel connection of two IGBT modules with a common Gate-Unit and with slightly different connection inductance values which resemble a not ideal but realistic difference to the virtual common connection point for this consideration. Through this configuration a loop between the
auxiliary emitter connections and the common emitter point is unavoidable.

\[
V_{GE} = V_{GU} - V_{ZE} - V_{ZG}
\]

Figure 7: Simplified schematic of a parallel connection

Especially during turn-on this has a significant influence on the dynamic current sharing. Assuming an identical initial turn-on \( \frac{dI_c}{dt} \) we get a proportional voltage drop across the stray inductance between the auxiliary emitter potential and the common point (marked as earth symbol in Figure 7):

\[
v_{L_E(n)} = \frac{dI_c}{dt} \cdot L_{SE(n)}
\]

Eqn. 3

This unequal potential of the two auxiliary emitters forces a current through the auxiliary emitter connection to the gate-unit. Consequently we get a voltage drop across the impedance of this connection \( (Z_e) \) which changes the effective gate voltage as shown in Figure 7. In the example the gate voltage for the left IGBT with lower emitter inductance will be lifted and the gate voltages for the right IGBT will be damped. Thus the left IGBT takes most of the initial current and thus also produces significantly higher turn-on losses. Figure 8 shows a simulated turn-on behaviour with two 3300 V / 1200 A IGBTs and unequal connection as shown in Figure 7. Obviously the current mismatch is quite significant which causes roughly 20 … 25 % higher turn-on losses for the left switch compared to the expected losses with ideal current sharing.

Needless to say that this severe current mismatch is far from being ideal, thus the current and losses mis-match needs to be translated into a proper de-rating if the design of the power circuit can not be improved.

Interestingly the effect on turn-off is nearly invisible since the gate-voltage has practically no influence on the turn-off current characteristics and the theoretical influence on the collector voltage is irrelevant since the voltages are forced to be identical by definition. Figure 9 shows a turn-off event. The influence of the unequal \( L_{SE} \) on \( V_{GE} \) is clearly visible, but it has negligible influence on the collector current and thus the overall characteristics.

Figure 8: IGBT turn-on with unequal emitter inductance

Figure 9: IGBT turn-off with unequal emitter inductance

3.2 Common Gate-Driver with common mode chokes

A patented method from ABB to rectify unequal connection impedance values is the use of so called common mode chokes. The common mode chokes nearly don’t influence the gate-emit-
ter impedance, but damp common mode voltage jumps caused by the voltage drop across $L_{\text{aux}}$.

Figure 10: Parallel connection with common mode chokes

In Figure 10 a simplified schematic of a parallel connection with common mode chokes in the gate is shown. Since the common mode chokes decouple the gate-unit from the IGBT emitter it is important to tap one emitter with a resistance ($R_E \sim 100 \, \text{m\Omega}$) to the gate-unit in order to facilitate a proper $V_{\text{CEsat}}$ measurement for the desaturation detection.

Figure 11 shows the turn-on switching with the same non-ideal conditions for the connection impedance as shown in Figure 8 but this time with the use of common mode chokes ($L_{pr} = L_{sec} = 120 \, \mu$H). The current mismatch and thus as well the turn-on losses mismatch are minimised and no more relevant. The graph also shows the voltage rejection across the common mode choke ($V_{\text{cm}}$). Consequently nearly no current flows in the auxiliary emitter.

The common mode chokes should be designed with minimal differential inductance and resistance and should be able to handle the gate-current load.

$$I_{G,\text{rms}} = \sqrt{\frac{(V_{\text{Gon}} + V_{\text{Goff}}) \cdot Q_{\text{ge}} \cdot f_{\text{sw}}}{R_G}}$$

Figure 11b: Turn-on with common mode chokes

3.3 Individual Gate-Driven

Another way to avoid loop currents in the auxiliary emitter is to use an individual gate-unit for each IGBT. Provided the drivers are perfectly matched (equal $V_{\text{GE}}$ and timing), the result would be pretty much the same as shown in Figure 11 resulting in good current sharing. However it needs to be considered that as other components, drivers suffer from parameter variations in the timing as well as the gate voltage.

Figure 12 and Figure 13 show the turn-on and turn-off with 100 ns delay between the gates from IGBT1 to IGBT2. As a result we get a significant dynamic current mismatch in terms of amplitude and delay. Thus the turn-on and the turn-off losses deviate up to 15 .. 20 % from the expected switching losses with ideal current sharing. In addition the turn-off current is 40 % above the average turn-off current. It is a must to consider this in the SOA derating of the paralleled IGBT modules.

Figure 12: Turn-on with 100 ns timing mismatch
In Figure 14 and Figure 15 the turn-on respective the turn-off switching with 0.5 V difference in $V_{GE}$ are shown. Even if $V_{GE}$ seems to have less influence in dynamic current sharing it needs to be considered, especially for the turn-on losses ($E_{on}$), where the mismatch of this example is still 5 .. 10 %.

### 3.4 Stray Inductance and Clamping

For reliable device operation it is crucial, that the peak voltage even during switching always stays below the maximum rated device voltage. Especially if high current modules are parallel connected, this can become a challenge for the power electronics engineer. The equation below shows the relation of the peak voltage and the switching speed ($\frac{di}{dt}$) and the stray inductance ($L_i$):

$$V_{CE_{\text{Em}}} = |\frac{di_v}{dt}| \cdot (L_{\text{dc}} + L_{\text{s}}) + V_{DC} \quad \text{Eqn. 5}$$

For parallel connection it is a realistic assumption that the total switching speed scales with the number of paralleled devices ($n$):

$$\frac{di_v}{dt_{\text{tot}}} = \frac{di}{dt} \cdot n \quad \text{Eqn. 6}$$

Thus in order to keep $V_{CE_{\text{Em}}}$ of the paralleled modules at a similar level of a single module, the stray inductance must be significantly reduced, since $\frac{di_v}{dt}$ for the IGBT turn-off can practically not be influenced by the $R_{\text{Goff}}$. Especially for high-current modules it is a huge effort to design a power circuit with the required low stray inductance. In this case active clamping can be the solution of choice:

Figure 16 shows the principle of an active clamp for one IGBT. It is crucial that the active clamp acts on all paralleled IGBTs. If only one IGBT in the parallel connection has an active clamp circuit, the turn-off current is shared unequal and is concentrated to the IGBT with the clamp. In addition each module in the parallel connection must have its own gate-clamp (fast Zener suppressor diodes between gate- and emitter and as well as a Schottky diode to the $+15$ V supply) and gate-resistor. Advanced active clamping with feedback to the final amplifier stage of the gate-unit (indicated with dashed lines) is strongly recommended in order to avoid overload to the suppressor diodes.
3.5 Phase connection
Additional current balancing between paralleled modules can be achieved with the introduction of additional impedance in the phase connection, which decouples the single modules (Figure 17).

This solution though has the disadvantage that the converter needs to supply the additional reactive power consumed by the inductors. An even better alternative to the single phase inductors is to magnetic couple the phase currents with chokes that can be built with ferrite cores (Figure 18). In this case the inductance has only an effect on the current difference between the paralleled phase-legs.

3.6 Influence of the junction Temperature
The junction temperature has a significant influence on the switching characteristics and thus the dynamic current sharing. Especially during turn-off it is crucial to ensure, that all modules are operated within its safe operating area. In order to investigate the dynamic current sharing, special measurements carried out on 3300 V / 1200 A SPT modules with by purpose varied junction temperatures have been carried out [2]. The test was done with a total stray inductance of 100 nH (200 nH/module) and with the use of common mode chokes (Figure 10) in order to minimize the influence of the power circuit.
In order to achieve an equal current sharing between paralleled modules homogenous cooling is crucial in order to maintain a close matching of the junction temperatures of the individual modules and to avoid possible thermal runaway. Additionally a very symmetric construction of the power circuit with identical connection impedance values for each module is an absolute must.

Table 1: Impact parameters on current-sharing

In addition the module parameter spread can be reduced by a suitable device selection with the parameters $V_{CEsat}$/V and $V_F$.

As Table 1 shows a current imbalance of up to 50 % in the turn-off current in case of switching delays caused by the gate-unit. In such a case the maximum turn-off current must be reduced by 50 % in order to stay inside the SOA.

Table 1: Impact parameters on current-sharing

Table:  Impact parameters on current-sharing

<table>
<thead>
<tr>
<th>Influence</th>
<th>mismatch %</th>
<th>Parameter</th>
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<td>Static</td>
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<tr>
<td>$V_{CEsat}$/V selected (100 mV)</td>
<td>1.5 .. 2</td>
<td>$I_c/I_F$</td>
</tr>
<tr>
<td>$V_{CEsat}$/V un-selected</td>
<td>2 .. 5</td>
<td>$I_c/I_F$</td>
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<tr>
<td>Connection Impedance $L_C$</td>
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<td>$E_{on}$</td>
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<tr>
<td>Gate-driver $K_d$ – 100 ns</td>
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<td>$E_{on}$</td>
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<tr>
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<td>$I_{on}$</td>
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Table:  Impact parameters on current-sharing

4.1 De-rating

The de-rating of modules in parallel connection should be done based on two kinds of considerations:

**Safe-Operating-Area**

The modules must always be operated within the safe operating area (SOA). The main topic to look at, are the switching currents. Table 1 for instance shows a current imbalance of up to 50 % in the turn-off current in case of switching delays caused by the gate-unit. In such a case the maximum turn-off current must be reduced by 50 % in order to stay inside the SOA.

**Thermal de-rating**

Not homogenous current sharing causes higher losses in the module that takes more current. Consequently this needs to be considered in case of parallel operation. For the on-state losses the current mismatch can be expressed by multiplying the on-state losses with the factor for the current imbalance (e.g. $D = 1.05$ for 5 % current mismatch).

$$P_{STAT} = (V_{r0} + r_{ce} \cdot I_c) \cdot I_c \cdot D$$

Eqn. 7

The same is true for the switching losses. If the losses mismatch is known it has to be considered for the total switching losses.
\[ E_{\text{req}}(I_C) = E_{\text{on}}(I_C) \cdot D_{\text{on}} + E_{\text{off}}(I_C) \cdot D_{\text{off}} \]

Eqn. 8

Figure 21 shows the output current of two paralleled and fully utilised 6500 V 600 A modules operated at its maximum junction temperatures. The solid line represents the achievable output current without any de-rating in inverter operation. The dashed lines show the reduced output current due to de-rating caused by module parameter variations. No de-rating due to the circuit parameters is considered, thus a perfect symmetrical power circuit is assumed. For the selected modules a delta \( V_{\text{CEsat}}/V_F \) of 100 mV (corresponding to 2% current static current imbalance) and dynamic switching loss mismatch of 2.5% (\( E_{\text{on}} + E_{\text{off}} \)) are assumed. For the randomly picked unselected modules a static current imbalance of 5% and a dynamic losses mismatch of 5% are assumed. This yields in a switching frequency dependent output current de-rating of 1.5 .. 2.5% for the selected module and 3.5 .. 5% for the unselected module. The switching frequency dependency comes from the fact that the dynamic losses mismatch gets dominant at higher switching frequencies. This has to be especially considered for dynamic current mismatch due to unsymmetrical power circuit connection or timing variations of the gate-drivers, which is not included in Figure 21.

5 References

6 Revision history

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