Packaging Technology Platform for Next Generation High Power IGBT Modules

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Abstract

To enable smaller and more cost efficient inverter designs, new power modules are designed for low losses, reliable operation at high temperature, high current and high switching frequencies. The IGBT module design presented in this paper features large silicon active area for low on-state losses, good internal temperature distribution, high current conductor leads with well-designed electro-magnetic behaviour and highly reliable joining techniques. Simulation results as well as experimental results from prototypes are presented.

1. Introduction

IGBT power modules are widely used in industry and traction applications. The purpose of the power module is to achieve high current rating by parallelizing semiconductor chips [1]. The power module package provides the mechanical protection and electrical insulation for the chips, it allows to remove the heat via the base plate to a cooler and it connects the chips via the bond wires and conductor leads to the bus bar (Figure 1).

Especially in traction applications the load of the power module is not constant. The modules in a locomotive's inverter drive undergo a thermal cycle while the train is driving from one station to the next. This typically leads to degradation of the interconnections within the module and subsequently to a wear out failure [4]. The module prototype presented in this paper uses low temperature bonding and ultrasonic welding as interconnection technologies. Both joining technologies are highly resistant to mechanical fatigue and thus higher module life time under same load can be expected. Or in order to get most out of a power module is used under harsher loads while the same life time is achieved.

In order to make use of the above improvements also the current carrying capability in general is improved by having more silicon area within the module, having a lowered terminal resistance and an optimized stray inductance.

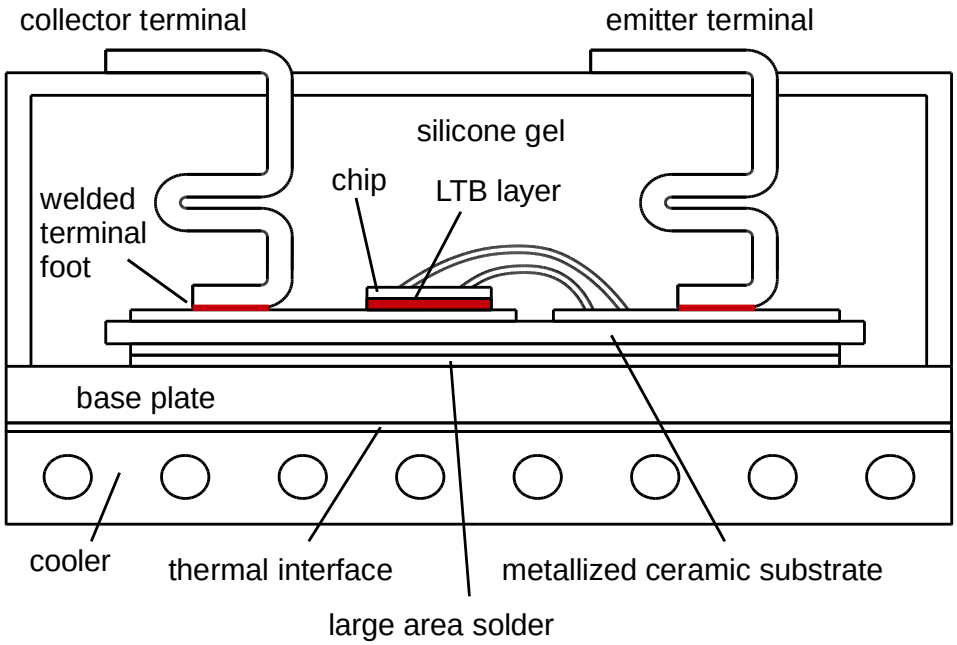

Figure 1: Schematic of the inner layout of an IGBT module.

2. Active area and temperature distribution

While keeping the outline of the HiPak module unchanged the design of the conductor leads and the substrate is optimized. An increase of the active IGBT area by 7% and of the active diode area by 42% is achieved. This allows higher output power especially in applications where the diode is normally limiting.

The design can also be used with the reverse conducting Bi-Mode IGBT (BiGT). In this case all chips are dissipating equal thermal power which leads to uneven temperature distribution with the chip arrangement as in the existing HiPak design (Figure 2 left). With the new design, the temperature distribution is improved by having only 12 chips arranged in the mid of the module compared to 18 chips at the periphery (Figure 2 right).

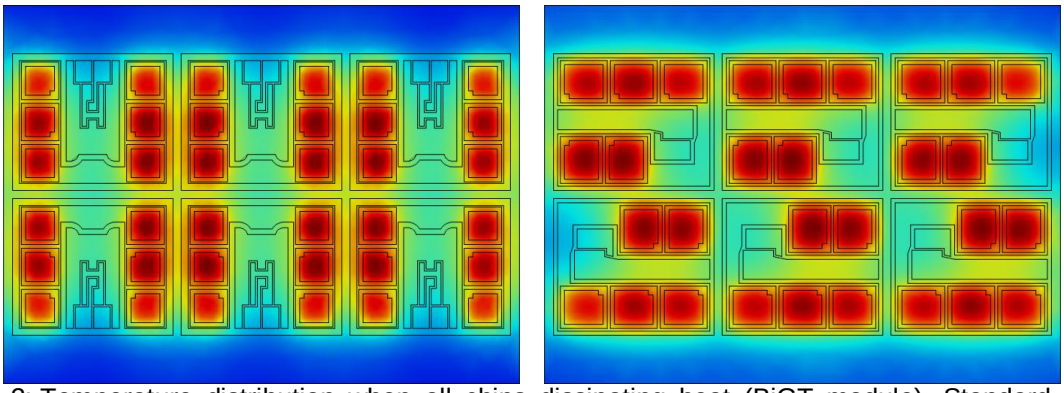

Figure 2: Temperature distribution when all chips dissipating heat (BiGT module). Standard HiPak design on the left and new design on the right.

3. Electro-magnetic behaviour

The IGBT module is turned on by applying a voltage of 15 V to the module's gate contact with reference to the auxiliary emitter contact. The following current rise builds up a magnetic field that induces a voltage into the control circuit. Consequently the gate-emitter voltages of the individual chips deviate from the 15 V applied externally to the module. This coupling effects influence the switching speed, the dynamic current balance in the module and the short circuit behaviour. Therefore an electro-magnetically robust design must ensure the coupling is homogeneous and with the right magnitude to achieve the desired switching behaviour.

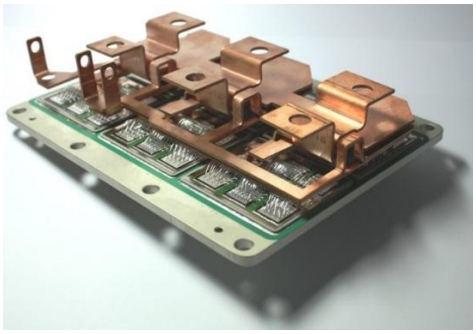

Figure 3: Open prototype for assessing electro-magnetic behaviour.

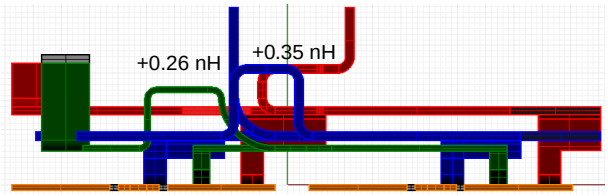

Figure 4: Additional loops used to adjust the switching speed of the module.

In order to experimentally asses the optimum coupling values three variants of the prototype are built (Figure 3 and Figure 4). The prototypes with nominal rating of 1700 V and 2700 A are built from three copper plates which correspond to collector, emitter and gate. In the first variant the gate plate closely follows the emitter in order to prevent undesired coupling of external fields into the control circuit. The second variant further exhibits a loop in the emitter plate that lifts the auxiliary emitter potential while turning-on. In the third variant a further loop is introduced to the gate plate that further increases the gate voltage. By using finite element simulation the induced voltage for a dI/dt of 10 kA/µs, which typically occurs in case of a short circuit, is calculated and given in the table below:

Prototype	**Loops**	**Induced voltage @ 10 kA/ µs**
Prototype 1, slow	none	-8.0 V
Prototype 2, medium	emitter	-4.6 V
Prototype 3, fast	gate + emitter	-1.8 V

Electrical measurements on the prototype have shown that the behaviour is as expected from the simulation. From prototype 1 to 3 the switching speed increases and the turn-on losses decrease. The switching curves under short circuit conditions [5] are shown in Figure 5. Prototype 1 is strongly damped and the current slowly reaches saturation. Prototype 2 is critically damped, the current rises fast and stabilizes at saturation. Prototype 3 exhibits a strong current overshoot that can lead to short circuit failure due to overheating or over voltage. As an optimum compromise between acceptable short circuit behaviour and low losses a coupling value between prototype 2 and 3 is targeted.

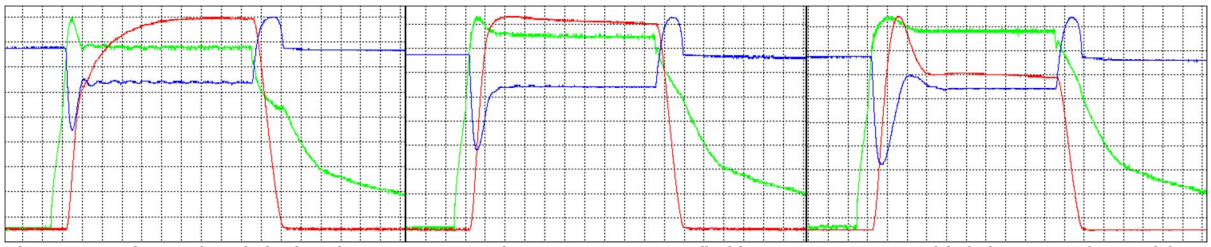

Figure 5: Short circuit behaviour measured on prototype 1 (left) to prototype 3 (right). CE-voltage blue, outer gate voltage green, current red.

4. Reliable joining techniques

4.1. Ultrasonic welding of power terminals

Ultrasonic welding [8] of the terminals to the ceramic circuit board is used to replace the solder joint. Compared to solder joints a welded joint does not undergo plastic deformation and fatigue during operation and therefore can reliably withstand higher stresses at elevated temperature. However, if too high forces are acting on the welded joint, a crack could initiate along the bonding interface and reducing the bond area, which may lead to premature failure of the joint. High forces typically occur when large temperature changes lead to internal thermo-mechanical stress. As a solution, a stress relief structure is implemented in the leg of the emitter terminal of a prototype module as shown in Figure 6

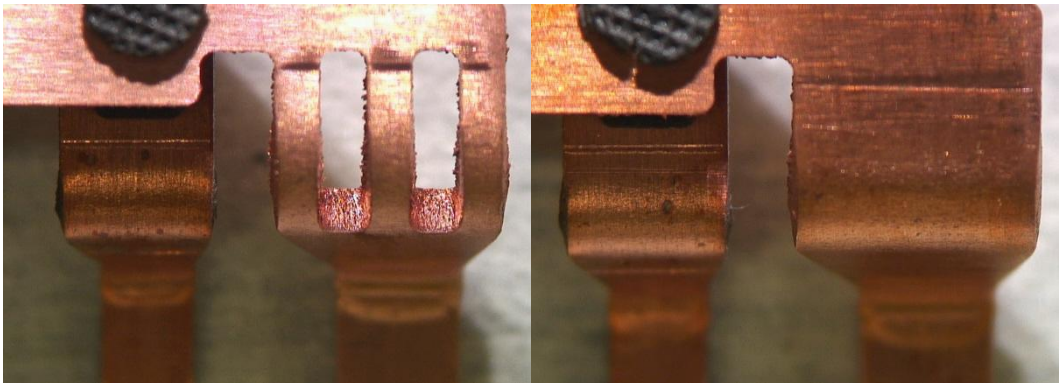

Figure 6: Emitter leg with and without stress relief structure.

The integrity of the joints has been investigated after stressing two prototype modules in a shock cycling experiment. The modules have been immersed in liquid of -40°C and +150°C with a dwell time of 10 minutes for each temperature. The welded area of each joint is determined by using scanning acoustic microscopy before the cycling experiment and after 100 and 200 cycles (Figure 7). Slight degradation of the joints is visible after 100 cycles. The images are evaluated using a grey value threshold set such that the determined area fits well the observed welding after the feet are sheared mechanically. The welding areas obtained by this method are plotted in the correlation plots in Figure 8. The plot on the left shows that the stress relief structure helps preventing degradation of the welding area by thermal shock cycles. However also without the stress relief structure, the degradation is only little. Further the plot on the right of Figure 8 shows that the welding area stabilizes in thermal shock cycling. There is no further degradation from 100 to 200 cycles independent of the presence of a stress relief structure.

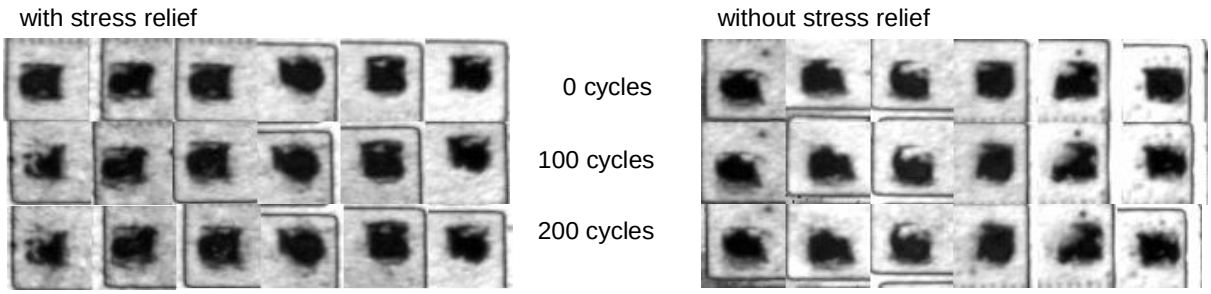

Figure 7: SAM scan of welding areas of prototypes with and without stress relief.

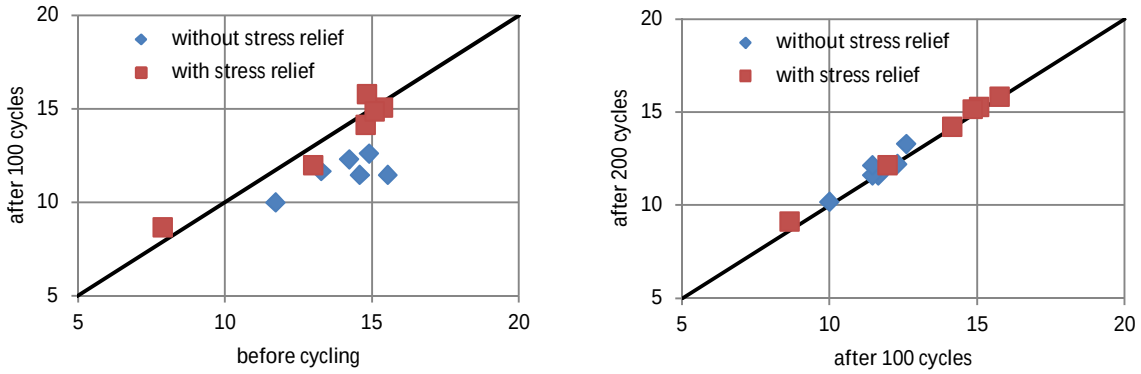

Figure 8: Correlation plots of welding area in mm^2. Before cycling versus after 100 cycles (left) and after 100 versus after 200 cycles (right).

4.2. Low temperature bonding

The IGBT and diode chips are attached to the metallized ceramic substrate, by using the low temperature bonding process (LTB) [6] also known as low temperature joining technique (LTJT) [7]. The process is done by disposing a layer of silver nano paste between substrate and the chips. Then pressure of up to 10 MPa at up to 310°C is applied to the assembly. The silver layer is sintered during up to 5 minutes. To prevent oxidation and promote adhesion of the bonding partners' surfaces, a silver plating on the chip side and a nickel-gold plating on the substrate side is used.

The particle size of the used powder is about 40 nm. The high surface energy of such nano-sized particles is a driver for surface diffusion in the sintering process and thus relatively low temperature in combination with pressure is sufficient to achieve a bond.

The LTB process window is assessed by varying the process parameters, temperature, pressure and time and subsequently characterizing the resulting bond by scanning acoustic microscopy (SAM), shear force measurements, cross sectioning and shock temperature cycling. The parameter range assessed is the following: time from 1 to 5 minutes, pressure from 1 to 10 MPa and temperature from 250°C to 310°C.

Figure 9 shows SAM images from the assessment. Two substrates are shown before and after thermal shock cycling bonded with low and high temperature, pressure and time, respectively. Low temperature, pressure and time lead to a weak bond which is not developed across the full area. Strong reflection of the acoustic signal leads to light grey appearance of the bond and indicates high porosity. After 2000 thermal shock cycles from -50°C to 150°C, three of five chips lifted off completely, whereas a slight degradation of the other two bonds is visible. This is in strong contrast with the sample bonded with high temperature, pressure and time. There the bond interfaces are imaged as nearly black areas in the SAM, which means almost the full acoustic signal is transmitted to the chip, indicating a highly dense joint. No degradation is visible after 2000 thermal shock cycles.

A cross-sectional image of the silver layer after sintering taken by scanning electron microscopy is shown in Figure 10. From that image the porosity is measured to be only 4.3%. With that low porosity the thermal conductivity of the layer can be expected to be not much below the 429 W/m*K of pure silver. With that high thermal conductivity and a final bond thickness of only 10 to 20 µm, the thermal resistance of the former soldered die attach is almost fully eliminated.

Low process parameters		High process parameters	
0 cycles	2000 cycles	0 cycles	2000 cycles

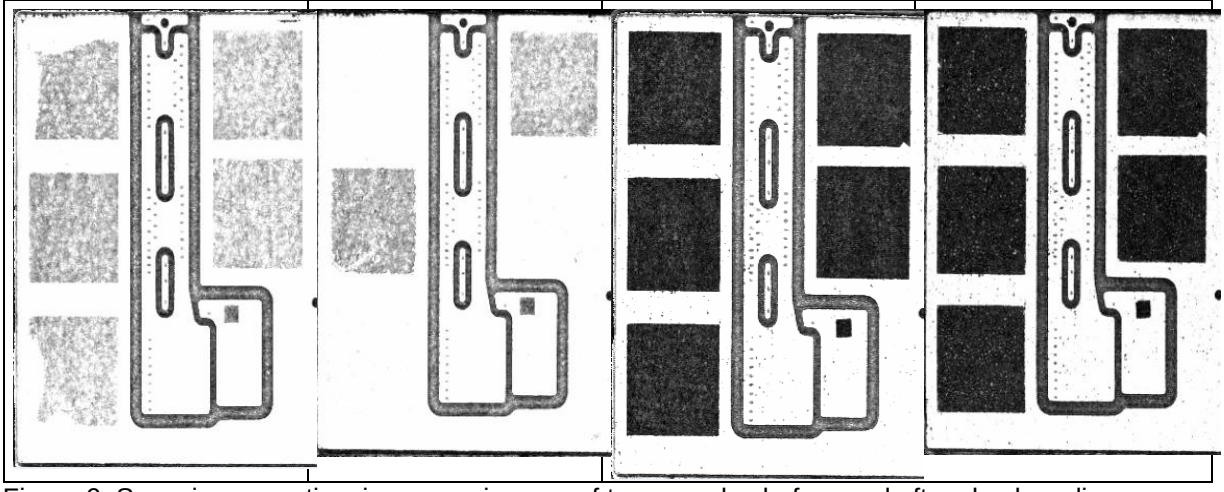

Figure 9: Scanning acoustic microscope images of two samples before and after shock cycling.

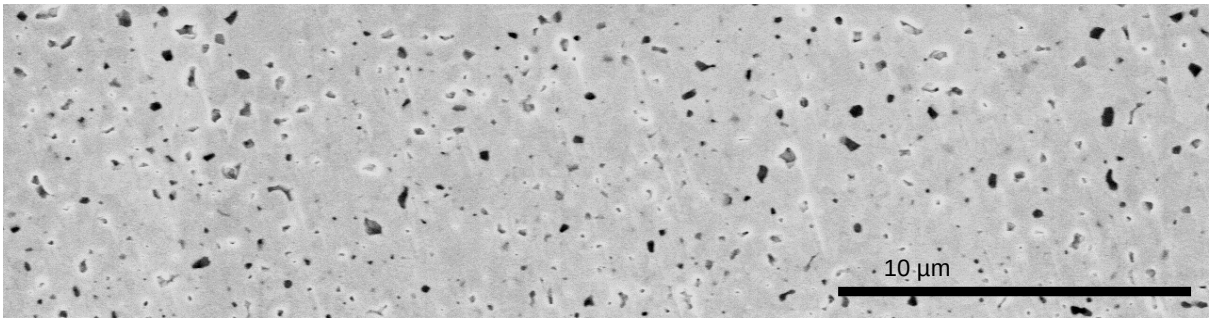

Figure 10: Cross section of sintered die attach under the scanning electron microscope. The observed porosity is 4.3%.

5. Conclusions

A HiPak2 IGBT module layout is shown with large silicon active area and well balanced temperature distribution in BiGT operating mode.

The switching speed of an IGBT module design is predicted by electro-magnetic simulations. The simulation method enables fine-tuning to meet the requirements of low loss and good short circuit behaviour.

Ultrasonically welded joints are generally stable in thermal shock cycling for the tested designs. A stress relief structure makes an otherwise mechanically stiff terminal design reliable.

High cycling life time of a silver sintered die attach has been demonstrated by thermal shock cycling.

A module that exhibits all the shown advantages will enable reliable operation at high temperature and at high currents and thus greatly contributes to smaller and more cost efficient converter designs.

6. References

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