A NEW FAULT LOCATION ALGORITHM FOR THREE-TERMINAL POWER LINE

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SYNOPSIS

This paper deals with fault location on three-terminal power line. The fault locator is considered as associated with the line protective relay, which communicates with the relays from the remaining line terminals and receives from them the phasors of measured three-phase currents. Three subroutines of the fault location algorithm are formulated and an issue of selecting the subroutine, which is valid in particular fault case, is considered. Sample results of ATP-EMTP based evaluation of the fault location algorithm are presented.

1. INTRODUCTION

Accurate location of faults on overhead lines for the inspection-repair purpose [1]–[8] is of vital importance for operators and utility staff for expediting service restoration, and thus to reduce outage time, operating costs and customer complains. An impedance principle, making use of the fundamental frequency voltages and currents, has been applied in different algorithms [3]–[7] designed for locating faults on three-terminal lines. In this paper a new fault location algorithm also categorized to such the principle is delivered, however, the other set of the fault locator input signals is utilized.

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2. NEW FAULT LOCATION ALGORITHM

Modern microprocessor-based protective relays exchange locally measured current phasors over long distances. For this purpose different forms of communication means are utilized. It is considered further that the fault location (FL) function is supplemented to the line protective relay at the end A (Fig. 1). Three-phase current from all line terminals: $\underline{I}_A$, $\underline{I}_B$, $\underline{I}_C$ – exchanged by protective relays A, B and C, together with the locally measured three-phase voltage phasor ($\underline{V}_A$) are assumed as the fault locator input signals. The measurements are considered further as synchronized, what can be accomplished using the well-known Global Positioning System (GPS) or the other techniques.

The proposed fault location technique is based on using three subroutines, denoted further: SUB_A, SUB_B, SUB_C. They are designated for locating faults: FA, FB, FC at hypothetical fault spots within particular line sections: AT, TB, TC, respectively. Note that any of the sections may be faulted at random. Therefore, the position of a fault is a random factor, and thus, the faulted line section is not known in advance. Therefore, the faulted section will be indicated using a special selection procedure.

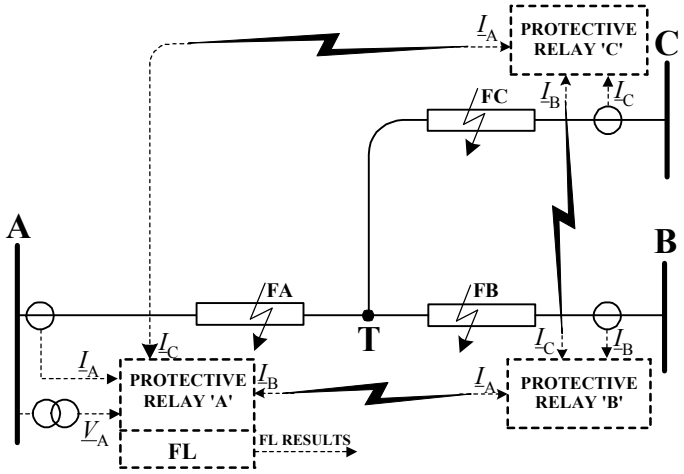

Fig. 1. Fault locator (FL) associated with protection of three-terminal line

2.1. Fault location algorithm – subroutine SUB_A

It is proposed to consider the natural fault loops for formulating the subroutines, analogously as in case of distance relays [2], [7]–[8]. The subroutine SUB_A, designed for locating faults (FA) within the line section AT (Fig. 2), is based on the following generalized fault loop model [8]:

$$\underline{V}_{Ap} - d_A \underline{Z}_{1LA} \underline{I}_{Ap} - R_{FA} \underline{I}_F = 0 \qquad (1)$$

where: d_A – unknown distance to fault on section AT (p.u.); R_{FA} – unknown fault resistance; $\underline{V}_{Ap}$, $\underline{I}_{Ap}$ – fault loop voltage and current; $\underline{Z}_{1LA}$ – positive sequence impedance of the section AT; $\underline{I}_F$ – total fault current.

Fault loop voltage and current are composed accordingly to the fault type [8], as the following weighted sums of the respective symmetrical components of the measured signals:

$$\underline{V}_{Ap} = \underline{a}_1 \underline{V}_{A1} + \underline{a}_2 \underline{V}_{A2} + \underline{a}_0 \underline{V}_{A0} \tag{2}$$

$$\underline{I}_{Ap} = \underline{a}_1 \underline{I}_{A1} + \underline{a}_2 \underline{I}_{A2} + \underline{a}_0 \frac{\underline{Z}_{0LA}}{\underline{Z}_{1LA}} \underline{I}_{A0} \tag{3}$$

where: $\underline{a}_1$, $\underline{a}_2$, $\underline{a}_0$ – weighting coefficients (Table 1); $\underline{V}_{A1}$, $\underline{V}_{A2}$, $\underline{V}_{A0}$ – symmetrical components of side A voltages; $\underline{I}_{A1}$, $\underline{I}_{A2}$, $\underline{I}_{A0}$ – symmetrical components of side A currents; $\underline{Z}_{0LA}$ – zero sequence impedance of the line section AT.

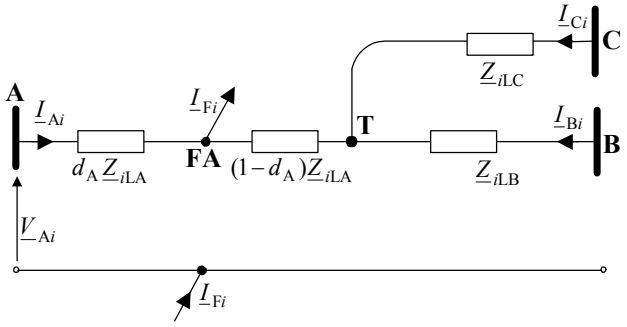

Fig. 2. Subroutine SUB_A: circuit diagram for the *i*th symmetrical component.

Table 1. Weighting coefficients for composing fault loop signals (2)–(3)

FAULT	$\underline{a}_1$	$\underline{a}_2$	$\underline{a}_0$
a-g	1	1	1
b-g	$-0.5 - j0.5\sqrt{3}$	$0.5 + j0.5\sqrt{3}$	1
c-g	$0.5 + j0.5\sqrt{3}$	$-0.5 - j0.5\sqrt{3}$	1
a-b, a-b-g a-b-c, a-b-c-g	$1.5 + j0.5\sqrt{3}$	$1.5 - j0.5\sqrt{3}$	0
b-c, b-c-g	$-j\sqrt{3}$	$j\sqrt{3}$	0
c-a, c-a-g	$-1.5 + j0.5\sqrt{3}$	$-1.5 - j0.5\sqrt{3}$	0

It is proposed to calculate the total fault current using the following generalized fault model:

$$\underline{I}_{\mathrm{F}} = \underline{a}_{\mathrm{F1}}\underline{I}_{\mathrm{F1}} + \underline{a}_{\mathrm{F2}}\underline{I}_{\mathrm{F2}} + \underline{a}_{\mathrm{F0}}\underline{I}_{\mathrm{F0}} \tag{4}$$

where: $\underline{a}_{\mathrm{F1}}$, $\underline{a}_{\mathrm{F2}}$, $\underline{a}_{\mathrm{F0}}$ – share coefficients, dependent on fault type (Table 2); the *i*th sequence component of the total fault current is determined as a sum of the *i*th (*i*=1–positive, *i*=2–negative, *i*=0–zero) sequence components of currents from all line terminals (A, B, C):

$$\underline{I}_{\mathrm{F}i} = \underline{I}_{\mathrm{A}i} + \underline{I}_{\mathrm{B}i} + \underline{I}_{\mathrm{C}i} \tag{5}$$

Table 2. Share coefficients used in fault model (4)

FAULT	$\underline{a}_{\mathrm{F1}}$	$\underline{a}_{\mathrm{F2}}$	$\underline{a}_{\mathrm{F0}}$
a-g	0	3	0
b-g	0	$1.5 + \mathrm{j}1.5\sqrt{3}$	0
c-g	0	$-1.5 - \mathrm{j}1.5\sqrt{3}$	0
a-b	0	$1.5 - \mathrm{j}0.5\sqrt{3}$	0
b-c	0	$\mathrm{j}\sqrt{3}$	0
c-a	0	$-1.5 - \mathrm{j}0.5\sqrt{3}$	0
a-b-g	0	$3 - \mathrm{j}\sqrt{3}$	$\mathrm{j}\sqrt{3}$
b-c-g	0	$\mathrm{j}2\sqrt{3}$	$\mathrm{j}\sqrt{3}$
c-a-g	0	$-3 - \mathrm{j}\sqrt{3}$	$\mathrm{j}\sqrt{3}$
a-b-c, a-b-c-g	$1.5 + \mathrm{j}0.5\sqrt{3}$	$1.5 - \mathrm{j}0.5\sqrt{3}$ *)	0

*) $\underline{a}_{\mathrm{F2}} \neq 0$, however, negative sequence component is not present.

For three-phase balanced faults it is proposed to use the superimposed (superscript: 'superimp.') positive sequence currents from the line ends A, B, C for calculating $\underline{I}_{\mathrm{F1}}$:

$$\underline{I}_{\mathrm{F1}} = \underline{I}_{\mathrm{A1}}^{\mathrm{superimp.}} + \underline{I}_{\mathrm{B1}}^{\mathrm{superimp.}} + \underline{I}_{\mathrm{C1}}^{\mathrm{superimp.}} \tag{6}$$

After resolving (1) into the real and imaginary parts, the unknown fault resistance (R_{FA}) and fault distance (d_{A}) can be determined, as for example the fault distance as:

$$d_{\mathrm{A}} = \frac{\mathrm{real}(\underline{V}_{\mathrm{Ap}})\mathrm{imag}(\underline{I}_{\mathrm{F}}) - \mathrm{imag}(\underline{V}_{\mathrm{Ap}})\mathrm{real}(\underline{I}_{\mathrm{F}})}{\mathrm{real}(\underline{Z}_{\mathrm{1LA}}\underline{I}_{\mathrm{Ap}})\mathrm{imag}(\underline{I}_{\mathrm{F}}) - \mathrm{imag}(\underline{Z}_{\mathrm{1LA}}\underline{I}_{\mathrm{Ap}})\mathrm{real}(\underline{I}_{\mathrm{F}})} \tag{7}$$

2.2. Fault location algorithm – subroutine SUB_B (SUB_C)

The subroutine SUB_C, designated for locating faults on the line section TC, is derived analogously to the subroutine SUB_B, and therefore is not presented. An analytic transfer

of three-phase measurements: $\underline{V}_{\mathrm{A}}$, $\underline{I}_{\mathrm{A}}$, $\underline{I}_{\mathrm{C}}$ to the beginning of the section TB, with strict taking into account the distributed parameter line model, is performed separately for each of the *i*th type of symmetrical component of three-phase voltage and current. Fig. 3 presents an equivalent circuit diagram of the line for the *i*th symmetrical component.

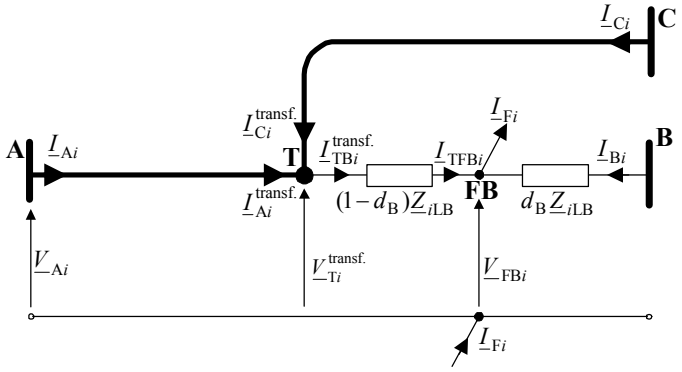

Fig. 3. Subroutine SUB_B: circuit diagram for the *i*th symmetrical component.

Transferring of voltage from the bus A to the tap point T results in:

$$\underline{V}_{Ti}^{\mathrm{transf.}} = \cosh(\underline{\gamma}_{i\mathrm{LA}}\lambda_{\mathrm{LA}})\cdot\underline{V}_{Ai} - \underline{Z}_{ci\mathrm{LA}}\sinh(\underline{\gamma}_{i\mathrm{LA}}\lambda_{\mathrm{LA}})\cdot\underline{I}_{Ai} \tag{8}$$

where: λ_{LA} – total length of the section AT (km); the parameters of the line section AT (for the *i*th sequence) are: $\underline{Z}_{ci\mathrm{LA}} = \sqrt{\underline{Z}'_{i\mathrm{LA}}/\underline{Y}'_{i\mathrm{LA}}}$ – surge impedance; $\underline{\gamma}_{i\mathrm{LA}} = \sqrt{\underline{Z}'_{i\mathrm{LA}}\underline{Y}'_{i\mathrm{LA}}}$ – propagation constant; $\underline{Z}'_{i\mathrm{LA}}$ – impedance (Ω/km); $\underline{Y}'_{i\mathrm{LA}}$ – admittance (S/km).

Transfer of the *i*th symmetrical sequence current from the beginning of the line section AT (bus A) to the end of the section (tap point T) gives:

$$\underline{I}_{Ai}^{\mathrm{transf.}} = \frac{-\sinh(\underline{\gamma}_{i\mathrm{LA}}\lambda_{\mathrm{LA}})\cdot\underline{V}_{Ai}}{\underline{Z}_{ci\mathrm{LA}}} + \cos(\underline{\gamma}_{i\mathrm{LA}}\lambda_{\mathrm{LA}})\cdot\underline{I}_{Ai} \tag{9}$$

Transfer of the current for the line section TC, performed analogously as in (9), gives $\underline{I}_{Ci}^{\mathrm{transf.}}$ (Fig. 3). The transferred *i*th symmetrical sequence current of the faulted line section TB (Fig. 3), flowing from the tap point T towards the fault point FB ($\underline{I}_{TBi}^{\mathrm{transf.}}$), is calculated as the sum of the currents transferred from the terminals: A (according to (9)) and from C (analogously as in (9)):

$$\underline{I}_{TBi}^{\mathrm{transf.}} = \underline{I}_{Ai}^{\mathrm{transf.}} + \underline{I}_{Ci}^{\mathrm{transf.}} \tag{10}$$

Using the determined transferred signals (8), (10), the fault loop voltage $\underline{V}_{\mathrm{Tp}}$ and current

$\underline{I}_{\mathrm{TBp}}$ are composed, as in (2)–(3). Then, analogously as in (1), the fault loop model for the subroutine SUB_B is formulated, and the unknowns d_{B}, R_{FB} are determined.

2.3. Selection of faulted line section

Three fault estimates are calculated assuming the fault to be on the AT, TB or TC segment of the line, respectively. In the first step of selecting the valid procedure, the results of the fault distance and resistance calculations are utilized. The subroutine, which yields the distance to fault indicating the considered fault as occurring outside the section range (outside the range: 0 to 1.0 p.u.), or/and the calculated fault resistance of negative value, is rejected. The second step of the selection is used when the first step is not sufficient. In this second step, the remote source impedances (behind the terminals B and C – if it is considered that the fault locator is installed at the station A (Fig.1), are calculated for different subroutines. For example, in case of considering the subroutine SUB_B (Fig. 3) for locating faults on the line section TB, the source impedance behind the bus B for the positive (negative) sequence is calculated as:

$$\underline{Z}_{1\mathrm{SB}}^{\mathrm{SUB\_B}} = \underline{Z}_{2\mathrm{SB}}^{\mathrm{SUB\_B}} = \frac{-\underline{V}_{\mathrm{B2}}^{\mathrm{SUB\_B}}}{\underline{I}_{\mathrm{B2}}} \tag{11}$$

where the estimated voltage at the bus B equals:

$$\underline{V}_{\mathrm{B2}}^{\mathrm{SUB\_B}} = \underline{V}_{\mathrm{T2}}^{\mathrm{transf.}} - (1-d_{\mathrm{B}})\underline{Z}_{1\mathrm{LB}}\underline{I}_{\mathrm{TB2}}^{\mathrm{transf.}} + d_{\mathrm{B}}\underline{Z}_{1\mathrm{LB}}\underline{I}_{\mathrm{B2}} \tag{12}$$

In the calculations (11)–(12) the negative sequence components are used. This can be applied for all faults except three-phase balanced faults, for which the negative sequence components are not present. Therefore, the superimposed positive sequence components have been recommended for use in case of three-phase balanced faults. Again, like in calculations according to (4), use of superimposed positive sequence components appears advantageous in comparison to use of the positive sequence components. Such preference results from the need for minimizing the shunt capacitance effect. The source impedance behind the bus C is calculated analogously to (11)–(12). Similarly, the source impedances are calculated according to the subroutine SUB_C.

Having calculated the impedances of the sources behind the remote buses B, C – according to both subroutines (SUB_B, SUB_C), first it is checked in which quadrant of the complex plane they are placed. For some rare fault cases a certain knowledge about the actual equivalent sources behind the line terminals has to be possessed. Note, that in case of the other fault location algorithms, which utilize incomplete three-end measurements [6]–[7], impedances of the sources are involved even in calculation of the distance to fault.

3. FAULT LOCATION FOR MULTITERMINAL LINE

Three-phase current acquired synchronously at all line terminals and additionally three-phase voltage from the terminal at which the fault locator (FL – Fig. 4) is installed, are taken as the input signals.

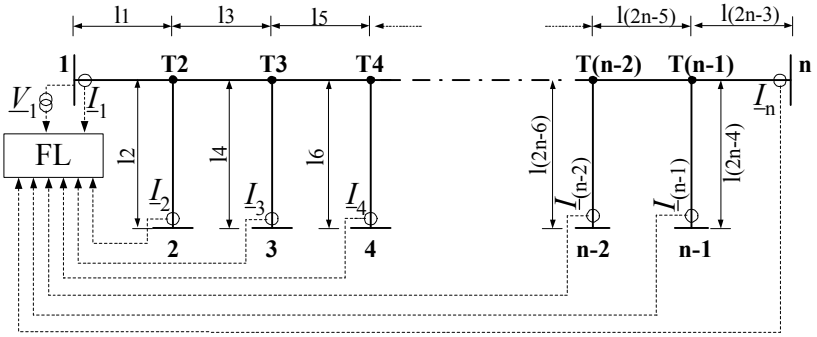

Fig. 4. Fault location on multi-terminal line with the assumed input signals.

4. ATP-EMTP BASED EVALUATION OF THE FAULT LOCATION ALGORITHM

ATP-EMTP program [9] was applied to evaluate performance of the developed fault location algorithm. The modeled 110 kV test network includes the line sections – AT: 100 km, TB: 80 km, TC: 50 km, having the positive (negative) and zero sequence impedances: $\underline{Z}'_{1L} = (0.0276 + j0.3151)$, $\underline{Z}'_{0L} = (0.275 + j1.0265)$; (Ω/km). The equivalent sources: $\underline{Z}_{1SA} = (0.65125 + j3.693)\Omega$, $\underline{Z}_{0SA} = (1.159 + j6.5735)\Omega$, $\underline{Z}_{iSB} = 2\underline{Z}_{iSA}$, $\underline{Z}_{iSC} = 3\underline{Z}_{iSA}$ were also included. Phase angles of the sources were assumed as: source A: 0^o, source B: -30^o and source C: -15^o.

The errorless current and voltage transformers were modeled. Analogue anti-aliasing filters with the cut-off frequency of 350 Hz were included, and 1 kHz sampling frequency was used. Full-cycle Fourier orthogonal filters were applied for determining phasors of the processed signals. The obtained continuous fault location results were averaged within the post-fault interval: from 30 up to 50 ms, after the fault inception.

Different specifications of faults have been considered in the study. However, only the results for the a–g faults, applied through 10 Ω fault resistance at different locations (0.1 to 0.9 p.u.) on particular line sections (Table 3 – Table 5) are presented here. Performance of the developed fault location algorithm for the other faults is also satisfactory.

Table 3. Fault location results: a–g fault on section AT, R_{FA}=10 Ω

d	**SUB_A**	SUB _B	SUB _C

(p.u.)	d_A (p.u)	R_{FA} (Ω)	d_B (p.u.)	R_{FB} (Ω)	d_C (p.u.)	R_{FC} (Ω)
0.1	**0.1001**	**9.99**	2.0542	10.22	2.8415	12.17
0.2	**0.2001**	**9.98**	1.8939	10.44	2.6016	13.01
0.3	**0.3001**	**9.96**	1.7428	10.65	2.3631	13.42
0.4	**0.4002**	**9.96**	1.6015	10.81	2.1285	13.47
0.5	**0.5003**	**9.95**	1.4702	10.91	1.9008	13.22
0.6	**0.6005**	**9.96**	1.3499	10.92	1.6833	12.74
0.7	**0.7008**	**9.97**	1.2413	10.82	1.4799	12.10
0.8	**0.8012**	**9.98**	1.1458	10.62	1.2949	11.38
0.9	**0.9018**	**10.00**	1.0649	10.33	1.1333	10.65

Table 4. Fault location results: a–g fault on section TB, R_{FB}=10 Ω

d_{B_actual} (p.u.)	SUB_A		**SUB _B**		SUB _C	
	d_A (p.u.)	R_{FA} (Ω)	d_B (p.u.)	R_{FB} (Ω)	d_C (p.u.)	R_{FC} (Ω)
0.1	2.4997	13.69	**0.0979**	**10.02**	0.6549	6.23
0.2	2.3796	14.12	**0.1982**	**10.01**	0.5878	6.15
0.3	2.2315	14.21	**0.2985**	**10.00**	0.5392	6.28
0.4	2.0690	14.02	**0.3988**	**9.99**	0.5118	6.60
0.5	1.8985	13.59	**0.4991**	**9.98**	0.5087	7.07
0.6	1.7234	13.00	**0.5994**	**9.98**	0.5334	7.64
0.7	1.5457	12.30	**0.6997**	**9.98**	0.5898	8.26
0.8	1.3660	11.53	**0.8000**	**9.97**	0.6827	8.90
0.9	1.1850	10.76	**0.9003**	**9.98**	0.8175	9.49

Table 5. Fault location results: a–g fault on section TC, R_{FC}=10 Ω

d_{C_actual} (p.u.)	SUB_A		SUB _B		**SUB _C**	
	d_A (p.u.)	R_{FA} (Ω)	d_B (p.u.)	R_{FB} (Ω)	d_C (p.u.)	R_{FC} (Ω)
0.1	1.6406	12.78	0.8723	9.88	**0.0996**	**10.02**
0.2	1.5935	12.88	0.8625	10.05	**0.1999**	**10.01**
0.3	1.5368	12.84	0.8577	10.20	**0.3001**	**10.00**
0.4	1.4731	12.67	0.8583	10.31	**0.4002**	**10.00**
0.5	1.4038	12.39	0.8646	10.37	**0.5004**	**9.99**
0.6	1.3302	12.02	0.8772	10.40	**0.6005**	**9.99**
0.7	1.2528	11.58	0.8964	10.37	**0.7006**	**9.99**
0.8	1.1721	11.09	0.9229	10.29	**0.8007**	**9.98**
0.9	1.0886	10.56	0.9573	10.16	**0.9007**	**9.99**

5. CONCLUSIONS

The new algorithm designed for locating faults on a three-terminal line has been presented. The specific set of the fault locator input signals: three-phase current from all line terminals and additionally the locally measured three-phase voltage, has been assumed. This fault location algorithm is intended for application with line protective relays. The developed fault

location algorithm consists of three subroutines, designated for locating faults within the respective line sections, and a multi-criteria procedure for selecting the faulted section.

ATP-EMTP software package was used to demonstrate the performance of the proposed fault location algorithm. The simulation results show that the accuracy of fault location is very high under various fault types, fault resistances, fault locations, pre-fault loading conditions and source impedances.

6. REFERENCES

[1] M. S. Sachdev (coordinator), "Advancements in microprocessor based protection and communication", *IEEE Tutorial*, Publ. No. 97TP120–0, 1997.

[2] IEEE Std C37.114: "IEEE Guide for Determining Fault Location on AC Transmission and Distribution Lines", *IEEE Power Eng. Society Publ.*, pp. 1-42, 8 June 2005.

[3] R. K. Aggarwal, D. V. Coury, A. T. Johns and A. Kalam, "A practical approach to accurate fault location on extra high voltage teed feeders", *IEEE Trans. Power Delivery*, Vol. 8, pp. 874-883, July 1993.

[4] A.A. Girgis, D.G. Hart and W.L. Peterson "A new fault location technique for two-and three-terminal lines", *IEEE Trans. Power Delivery*, Vol. 7, No.1, pp. 98-107, January 1992.

[5] D. A. Tziouvaras, J. Roberts and G. Benmmouyal, "New multi-ended fault location design for two- or three-terminal lines", *Proceedings of Seventh International IEE Conference on Developments in Power System Protection*, pp. 395 – 398, 9-12 April 2001.

[6] Y. Lin, C. Liu and C. Yu, "A new fault locator for three-terminal transmission lines using two-terminal synchronized voltage and current phasors", *IEEE Trans. Power Delivery*, Vol. 7, No.3, pp. 452-459, 2002.

[7] J. Izykowski, , R. Molag, E. Rosolowski and M.M. Saha, "Fault location in three-terminal line with use of limited measurements", *Proceedings of PowerTech* (*CD*), St. Petersburg, 27-30.06.2005.

[8] J. Izykowski, E. Rosolowski and M.M. Saha, "Locating faults in parallel transmission lines under availability of complete measurements at one end", *IEE Gener., Transm. and Distrib.*, Vol. 151, No. 2, pp. 268-273, March 2004.

[9] H. W. Dommel, *Electro-Magnetic Transients Program*, BPA, Portland, Oregon, 1986.

7. BIOGRAPHIES

Murari Mohan Saha (M´76, SM´87) was born in 1947 in Bangladesh. He received B.Sc.E.E. from Bangladesh University of Engineering and Technology (BUET), Dhaka in 1968 and completed M.Sc.E.E. in 1970. From 1969 to 1971 he was a lecturer at the department of Electrical Engineering at BUET, Dhaka. In 1972, he completed M.S.E.E. and in 1975 he was awarded with Ph.D. from the Technical University of Warsaw, Poland. He joined ASEA, Sweden, in 1975 as a Development Engineer and currently is a Senior Re-

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Jan Izykowski (M'1997, SM'04) was born in Poland in 1949. He received his M.Sc., Ph.D. and D.Sc. degrees from the Faculty of Electrical Engineering of Wroclaw University of Technology (WUT) in 1973, 1976 and in 2001, respectively. In 1973 he joined Institute of Electrical Power Engineering of the WUT where he is presently an Assosiate Professor and Director of this Institute. His research interests are in power system transients simulation, power system protection and control, and fault location. He is a holder of 13 patents and authored more than 150 technical papers.

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Przemyslaw Balcerek was born in 1976 in Poland. He received his M.Sc. and Ph.D degrees in Electrical Engineering from the Wroclaw University of Technology (WUT) in 2000, 2004 respectively. Fault location, instrument transformers and ATP-EMTP simulation of power system transients are in the scope of his research interests. Presently he is in ABB Corporate Research Center in Krakow/Poland as a research scientist.

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