Application

The master station processor module is used within a PROCONTROL master station.

Together with the modules 88 VA01/VA02 (control module for transfer procedure) and 88 VT01/VT02 (telegram handling module) it forms part of the central processor within the master station. This processor controls and monitors the entire data transfer on the connected PROCONTROL remote bus system.

Features

The module can be plugged into each of the two master stations of the PROCONTROL bus system, but is only available once for each station. It is provided with two standard interfaces: one of these is used to link the module to the master station bus to which all modules of the master station (including master station coupling modules 88 VK01) are connected. The second one is for the general-bus which only connects the modules 88 VP01/VP02, 88 VA01/VA02 and 88 VT01/VT02 with each other.

Two connectors and one pushbutton are provided at the front of the module.

A logic analyzer can be connected to this connector. With this analyzer, all important signals, program sequences and all telegrams can be measured for diagnostic functions.

By pressing the pushbutton RST, the entire master station can be reset and, thus, a defined initial state established.

Description

GENERAL DESIGN

The master station processor module controls and monitors the entire data transfer on the connected remote bus system. The functional sections (see also "Functional diagram") described below, enable this module to carry out these tasks. Some of the tasks, however, are carried out by the modules 88 VT01/VT02, 88 VA01/VA02 and 88 VK01 when instructed by the processor module.

PROGRAM MEMORY (PS)

The program needed for the processor is contained in the program memory, with a word width of 48 bits. The data word is divided into defined bit groups, which contain the required commands and data in coded form. These coded command fields are decoded and processed partly on the processor module itself and partly on the other above mentioned modules.

The module contains slots for 12 PROMs for storing the program. These slots are equipped with the program memories PS0 to PS5.

88 VP01-E/R1010: The program memories are 6 PROMs with 2 K, 8 bit (permits maximum 2 K program)

88 VP02-E/R1040: The program memories are 6 PROMs with 4 K, 8 bit (permits maximum 4 K program)

PROGRAM COUNTER

The instructions of every individual program step are stored in the program memory in certain memory locations. Every memory location is allocated individually by an address.
The program counter has the function of counting through the program steps. For each step it generates an address with which the program memory is accessed. The program data word belonging to this address is then made available on the data output lines (48-bit word).

The program counter can be loaded, incremented and decremented for each program instruction.

**PROGRAM COUNTER CONTROL CIRCUIT**

The program counter is controlled by the program counter control circuit. This generates, for every program step, one of three possible program counter commands: increment, decrement and load, and controls the program counter multiplexer.

With the "load" command, the counter can assume any state (and hence the memory location address) between 0 and 2047. The address to be loaded is switched through by the program counter multiplexer.

**PROGRAM ADDRESS BUFFER (STACK)**

This buffer serves to store the current program address of the program counter from which branching to a subroutine is to be effected. The buffer has space for 16 addresses. Thus, up to 16 subroutines can be nested in each other.

The STACK operates on the stacking principle. It is possible, within a subroutine, to jump again to one or more subroutines. The program address from which a branch to the first subroutine was made, is filed at the bottom of the buffer (lowest address in the buffer). The processor writes each address of the current subroutine from which a branch was made to another subroutine, into the next higher memory location.

After the last subroutine has been executed, the addresses of the stack locations are counted again in descending order. Thus the program counter is loaded again via the program counter multiplexer with the address at which the higher-level subroutine was interrupted. The address at which the main program itself was interrupted is, therefore, the last to be read from the buffer. The processor then continues with the main program.

**PROGRAM COUNTER MULTIPLIER**

During loading on the program counter, this multiplexer switches through one of three possible address sources for the next program step. The three address sources are:

- Program memory
- STACK
- Indirect address register

For branching from the main program to a subroutine, the address at which this subroutine begins in the program memory is contained in the 48-bit data word. In this case, the program memory itself is the source from which the program counter receives its load information via the multiplexer. The branch is made without any other conditions.

For returning from the subroutine to the main program, the counter receives this return address from the STACK via the multiplexer.

For indirect program branches, the branch address is dependent on certain other conditions. The address is made up of two parts:

- a base address (indirect address register),
- an address index from the index memory or index buffer.

**INDIRECT ADDRESS REGISTER**

In the case of indirect program branches, the fixed part of the starting address of the subroutine is written into the indirect address register. This information is taken from the program memory.
INDEX MEMORY (IS)

The index memory consists of a 1 K x 8-bit PROM and an up-stream 8-bit address register.

With this arrangement, it is possible to load an 8-bit data word of optional content as PROM address into the address register, in each of the 4 address ranges 0-255, 256-511, 512-767 and 768-1023, and to assign a code in the form of the PROM contents to each of these possible address combinations. The code selected in the PROM by the address is added by the adder as an address index of the base address contained in the indirect address register. Base address and added index are then loaded as an address for an indirect branch in the program counter via the program counter multiplexer.

ADDER

The adder derives the sum from the base address (in the indirect address register) and the index address (from the index memory or index buffer). The derived value is passed on to the program counter multiplexer as a branch address for indirect program branches.

CONSTANT DRIVER

The constant driver switches an 8-bit constant through the general-bus when instructed by the processor.

These constants are taken from the program memory (as are the base addresses for the indirect address register).

TEMPORARY REGISTER

The general bus has a data word width of 8 bits. The temporary register serves for quick temporary storage of 8-bit words from the general-bus. The outputs from this register also act directly on the general-bus.

DATA BUFFER

The data buffer is also used to store 8-bit data words from the general-bus. This buffer, however, has a capacity of 16 words of 8 bits each.

A 4-bit address register which also receives its address data from the general-bus serves to address the 16 memory locations.

POWER-ON DETECTOR

This circuit section generates a reset pulse PON (Power on Reset), when the voltage is connected, which is sent to the master station bus and which also acts internally on the general-bus. Thus, the entire master station is brought into a defined initial state. The RST pushbutton has the same effect (see "Operating functions").

Since the dual channel design of the PROCONTROL bus system only allows one master station to take over control of data transfer, both master stations are controlled by the monitoring station. This is achieved through a coupling module for monitoring station 88 VU01 in the master stations.

The processor module of the master station that is switched off, receives a reset signal MRST (Master Reset) from the 88 VU01. This is combined with signal PON, so that the program counter is set to zero and maintained at this value.

Signal MRST is present as long as the other master station is executing its program cycle. Due to the fact that the reset procedures (MRST signal and program-dependent transfer between 88 VP01/VP02 and coupling module for monitoring station 88 VU01 via the master station bus) are independent of each other the master station is also switched off in the case of simple hardware faults, and the redundant master station is positively switched on.
Functional sequences

The program of the master station processor module 88 VP01/VP02 implements such transfer system functions as are needed for proper data transfer in the PROCONTROL bus system. The entire program is made up of a multitude of individual functional sequences. The program-initiated actions and reactions of the processor module are dependent on the system configuration involved and the actions and reactions of all bus-connected modules. Detailed information is provided in the program description and the flow chart.

The most important functional sequences are listed below. The entire program can be subdivided into three main areas.

1. Initialization

This part of the program contains functional sequences for preparing the master station for data transfer:

- Checking whether the modules 88 VAO1/VAO2, 88 VTO1/VTO2 themselves and their PROMs are plugged in (station address PROM on 88 VAO1/VAO2, constant PROM on 88 VTO1/VTO2)
- Resetting all coupling modules 88 VK01 available in the station
- Resetting the telegram handling module 88 VTO1/VTO2
- Loading program relevant data into certain registers
- Obtaining cycle start permission from coupling module monitoring station 88 VU01 and outputting a feedback signal to the 88 VU01 to indicate correct cycle start
- Storing the total number of telegrams of the multi-purpose processing stations after "Power On" or after pressing pushbutton ZT in module 88 VAO1/VAO2 (see module description "Control module for transfer procedure 88 VAO1/VAO2", GKE 705 179).

With the exception of the last one, all these items are repeated before the system cycle is performed.

2. System Cycle

This part of the program contains functional sequences for data transfer:

- Generating call and instruction telegrams to the stations
- Controlling the bus coupling modules for master station 88 VK01 for telegram distribution
- Buffering the transferred telegrams (e.g. for repetition)
- Evaluating the acknowledgement and event announcements (on the noise channel) from 88 VK01 modules.
- Repeating telegrams when errors occur
- Identifying and calling the event stations
- Analyzing the telegrams (telegram types, function code, addresses)
- Counting the telegrams transferred by a station
- Counting the stations (via station address counter on 88 VAO1)
- Reacting in the appropriate manner when errors are detected.

Data transfer is carried out in two ways:

a) Cyclic mode

With this, every station connected to the bus system is called in sequence by the master station to transfer all of its telegrams. When the last station available in the system has been called, the processor restarts from the beginning with the initialization part of the program.

b) Event mode

If event announcements are recognized, the processor interrupts the cyclic mode. After the event generating stations have been identified, they are given - also in sequence - permission to transfer their event telegrams. When there are no more event announcements, the cyclic mode is resumed from the place at which it was interrupted.
3. DIAGNOSTIC FUNCTIONS

This part of the program contains the functional sequences for diagnostics, which provide information on the operating state of the system components. The most important diagnostic functions are:

- Cyclic hardware test of the master station bus and the general-bus in the initialisation program
- Monitoring the transmission clock pulse and CRC generators
- Disturbance during telegram analysis
- Acknowledgement errors, CRC errors
- Stations do not respond
- Difference in addresses between call and response
- Difference between telegram numbers
- Disturbances in the coupling modules 88 TK02
- Testing all remote bus lines
- Plausibility check of the received telegram contents

Operating modes

CENTRAL CLOCK

Printed circuit board 1 of the module incorporates a circuit logic for generating the required system clock pulses within the module. They are derived from the frequency of a 10 MHz oscillator. In this frequency line, plug-in jumper place X 102 is provided (see "Mechanical design"). This jumper is removed for factory-internal testing purposes only. It must be in place for normal operation in the master station.

Operating function

RESETTING

A pushbutton RST is provided at the front of the module (see "Mechanical design").

Pressing this button generates a reset signal, which - the same as when power is connected (see "POWER-ON DECODER") - establishes a defined initial state for the entire master station.

Test function

Two test plugs X1 and X2 are provided at the front of the module.

To these, the 8 data lines of the general bus as well as the whole 48-bit data word of the program memory are connected. The individual command fields are also available here in coded form.

Thus, the entire master station program can be observed by means of a connected logic analyzer.

ANNOUNCEMENTS TO COUPLING MODULE 88 VU01

The following announcements are transferred to the coupling module of monitoring station 88 VU01:

- Information on the start and end of a system cycle carried out by the processor
- Disturbances detected during the hardware test (see "Diagnostic information").
Functional diagram

The module consists of 2 printed circuit boards. Each printed circuit board is equipped with one connector $X3$ (upper connector) and one connector $X4$ (lower connector).

Each connector $X3$ contains the interface to the master station bus and the voltage supply. Each connector $X4$ incorporates the interface to the general bus.
Connection diagram in the master station

- Monitoring module for master station 88 VU02
  - GSS
  - VSS
  - UD +
  - ZD
- Telegram handling module 88VT01/VT02
  - GSS
  - VSS
  - UD +
  - ZD
- Control module for transfer procedure 88 VA01/VA02
  - GSS
  - VSS
  - UD +
  - ZD
- Master station processor module 88 VP01/VP02
  - VSS
  - UD +
  - ZD
- Coupling module for master station (1) 88 VK01
  - VSS
  - UD +
  - ZD
- Coupling module for master station (8) 88 VK01
  - VSS
  - UD +
  - ZD
**Mechanical design**

**Board size:** 6 units, 1 division, 220 mm deep

**Connector:** according to DIN 41 612
4 x 48-pole, edge connector type F
(each for X3 and X4)

according to MIL-C-24 308
2 x 37-pole female connector type HD
Fabricated by AMP (for X1 and X2)

**Weight:** approx. 0.5 kg

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**ORDER NUMBERS OF THE PROGRAM MEMORY MODULES ON PRINTED CIRCUIT BOARD 2**
(see also diagram on next page)

<table>
<thead>
<tr>
<th>Memory modules:</th>
<th>Order number:</th>
<th>Order number:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Component)</td>
<td>(PROM programmed)</td>
</tr>
<tr>
<td><strong>.88 V01/R1010:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = A246/PS0</td>
<td>GJTN160199P2</td>
<td>GJR2352002Pxxxx</td>
</tr>
<tr>
<td>2 = A247/PS1</td>
<td>GJTN160199P2</td>
<td>GJR2352003Pxxxx</td>
</tr>
<tr>
<td>3 = A248/PS2</td>
<td>GJTN160199P2</td>
<td>GJR2352004Pxxxx</td>
</tr>
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<td>4 = A249/PS3</td>
<td>GJTN160199P2</td>
<td>GJR2352005Pxxxx</td>
</tr>
<tr>
<td>5 = A250/PS4</td>
<td>GJTN160199P2</td>
<td>GJR2352006Pxxxx</td>
</tr>
<tr>
<td>6 = A251/PS5</td>
<td>GJTN160199P2</td>
<td>GJR2352007Pxxxx</td>
</tr>
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<td><strong>.88 V02/R1040:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 = A226/PS6</td>
<td>GJTN160259P1</td>
<td>GJR2353302Pxxxx</td>
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<td>8 = A227/PS7</td>
<td>GJTN160259P1</td>
<td>GJR2353303Pxxxx</td>
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<tr>
<td>9 = A228/PS8</td>
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<td>10 = A229/PS9</td>
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<td>11 = A230/PS10</td>
<td>GJTN160259P1</td>
<td>GJR2353306Pxxxx</td>
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<tr>
<td>12 = A231/PS11</td>
<td>GJTN160259P1</td>
<td>GJR2353307Pxxxx</td>
</tr>
</tbody>
</table>

**Note:**

The mounting position of the components is marked by an imprint on the printed circuit board.  

***xxx = Position numbers corresponding to the appropriate revision.***
POSITION OF THE MEMORY MODULES ON PRINTED CIRCUIT BOARD 2
(For explanations see previous page)

Important:
The module should only be plugged into the slot range 09 - 45 (general-bus range, lower connector) of the master station (double subrack AA, AB).

Note:
The plug-in jumper X202 is not present on 88 VP02. On 86 VP01, pin 1 must always be connected to pin 2.
POSITION OF THE MEMORY MODULE ON PRINTED CIRCUIT BOARD 1 AND FRONT PANEL

88VP01-E
88VP02-E

Memory module: Order number: Order number (88 VP01): Order number (88 VP02):
(8) = A145/IS. (component) (PROM programmed) (PROM programmed)
GJTN160183PI GJR2352001Pxxx GJR2353301Pxxx

xxxx = Position number corresponding to the appropriate revision.

Note:
Next to the component its designation and position on the printed circuit board is stated. Both printed circuit boards are connected with each other electrically and mechanically.

Explanation:
(1) = motherboard (2) = sub-board
Technical data

In addition to the system data the following values apply:

**POWER SUPPLY**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>88 VP01</th>
<th>88 VP02</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating voltage</td>
<td>UD⁺ = +5 V</td>
<td>UD⁺ = +5 V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>ID = 2.8 A</td>
<td>ID = 3.3 A</td>
</tr>
<tr>
<td>Power dissipation typ.</td>
<td>PV = 14 W</td>
<td>PV = 16.5 W</td>
</tr>
<tr>
<td>Reference potential</td>
<td>ZD = 0 V</td>
<td>ZD = 0 V</td>
</tr>
</tbody>
</table>

**STANDARD CONNECTIONS**

VSS - Standard interface to the master station bus

GSS - Standard interface to the general bus

**ORDERING DATA**

Type designation: 88 VP01-E/R1010 *
88 VP02-E/R1040 **

Order number: GJR2311300R1010 *
GJR23711000R1040 **

* 88 VP01-E/R1010 is to be replaced by
88 VP02-E/R1040

** 88 VP02-E/R1040 replaces 88 VP01-E/R1010

Technical data are subject to change without notice!