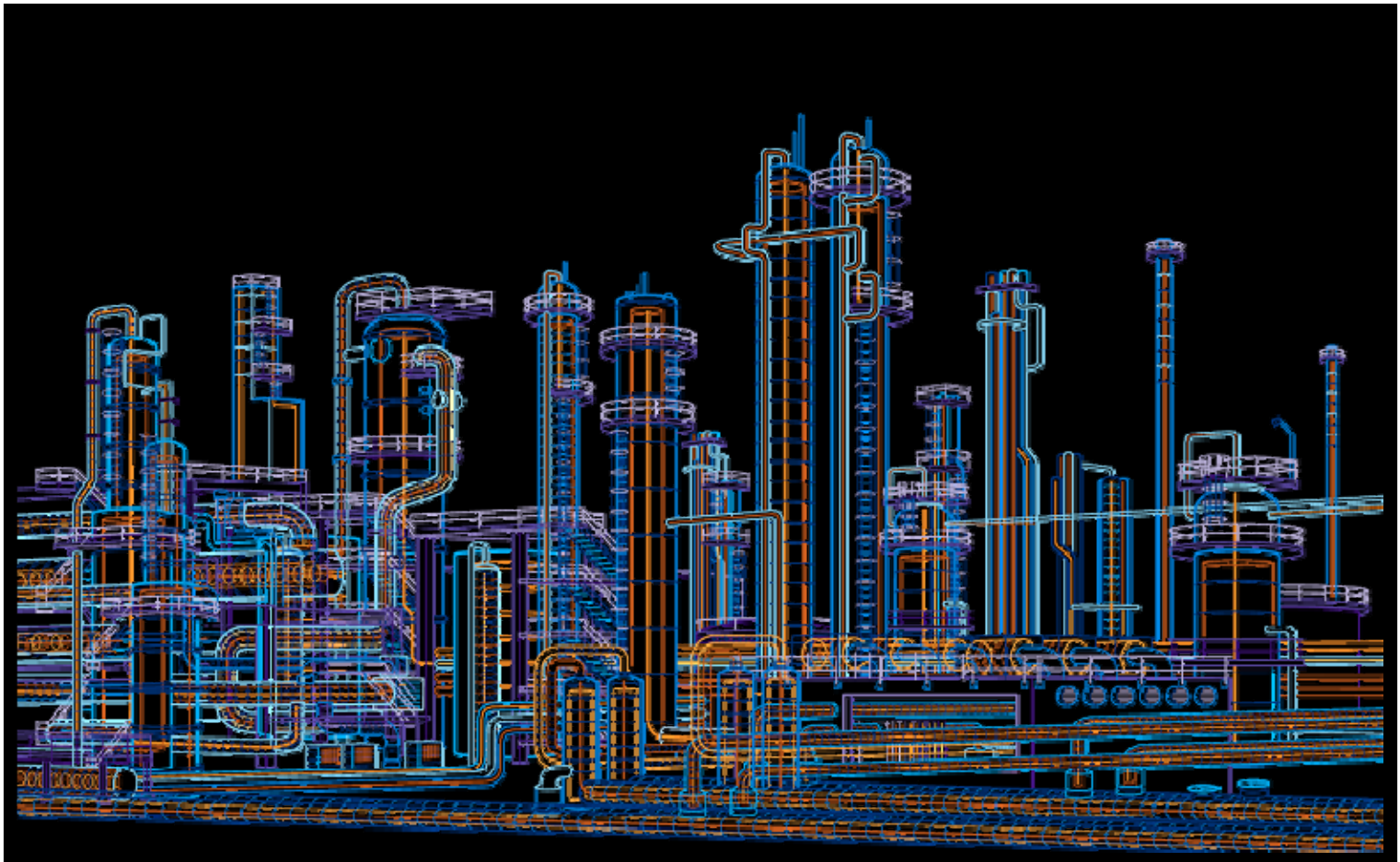

System 800xA
PC Toolkit Library for Melody
Function Diagram Template - PC_CTRL_1
User Manual

System Version 5.1

Power and productivity
for a better world™

Purpose

The purpose of this document is to describe the features and functionality of the function diagram template for a standard PID controller. This document will define the ABB Control System standards for the implementation of the Toolkit specification to be adopted across all sites and on all plants.

Conditions

The System Extension supports System 800xA System Version 5.1 or higher.

Notice

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Table of contents

1. Function 4
1.1 General Functional Description 4
1.2 Used Blocks 4
1.2.1 Function Blocks 4
1.2.2 Diagram Output References 5
1.2.3 I/O Modules 6
1.2.4 Diagram Input References 6
1.3 Function Template 7
1.4 Configurable Parameters 15
1.4.1 Function Blocks 15
1.4.2 IO Modules 20
1.4.3 Diagram Output References / Signal Parameters 21
1.5 Additional Information 22
1.6 Performance of the function module in a fault scenario 23
2. Document References 23

1. Function

1.1 General Functional Description

The function diagram template PC_CTRL_1 realizes a loop control functions in the process control system. The template covers the following main functionality:

- Standard PID controller
- Change of controller operating mode (manual/automatic) via external logic
- Change of controller set point mode (internal/external) via external logic
- Display of the measuring signal at the input card with its measurement range and engineering unit
- Supervision of the input signal for faults (e.g. short circuits, line break, board error, channel error…)
- In case of an error or fault condition, a substitute value may be used. Three substitute value strategies are available:
  1. The input value is written to the output value, no default value handling
  2. The last valid value at the input is written to the output and retained
  3. The output value is set to a preconfigured/substitute value
- Supervision of the input signal against an operating range (Limit ALD, Limit AHD), two low (Limit L, Limit LL) and two high (Limit H, Limit HH) limits. Whenever a limit is violated, an alarm/event is generated (depending on the alarm/event configuration)
- Supervision of the output signal against one limit range (OutLimit L, OutLimit H). Whenever a limit is violated, an alarm/event is generated (depending on the alarm/event configuration)
- En-/Disabling alarms via logic
- Inhibiting limit supervision output for further processing via logic
- Manipulating the output value of the module via faceplate (using alternative value)
- Filtering of the input signal

1.2 Used Blocks

1.2.1 Function Blocks

Function Block	Name	Library	Description
APIDL-00	PC_CTRL_1	CLC	Controller function large Function Block description see /6/ Operation description see /1/
IVDEC-R0	PC_CTRL_1	Analog/Binary	Invalid decoder Real
IVCOD-R0	PC_CTRL_1	Analog/Binary	Invalid coder Real
OR-B0	PC_CTRL_1	Binary	OR Boolean

Function Block	Name	Library	Description
BSFUP_P	PC_CTRL_1		Bit select function diagram
AND-B0	PC_CTRL_1	Binary	AND Boolean
DELAY-00	PC_CTRL_1	Binary	Delay Boolean
LWR-R0	PC_CTRL_1	Analog/Binary	Write value with enable Real
LWRNV-R0	PC_CTRL_1	Analog/Binary	Write value with enable Real to Hybrid
LE-R0	PC_CTRL_1	Analog/Binary	Analog comparator A<B
GT-R0	PC_CTRL_1	Analog/Binary	Analog comparator A>B
ADD-B0	PC_CTRL_1	Analog	Adder
SUBB-R0	PC_CTRL_1	Analog	Subtracter
ABS-R0	PC_CTRL_1	Analog	Absolute value
DYNOR-00	PC_CTRL_1	Binary	OR dynamic
CONPSRC	PC_CTRL_1	Connectors	Connector source
CONPSNK	PC_CTRL_1	Connectors	Connector sink

Table 1.1 Function Blocks

1.2.2 Diagram Output References

Signal	Data Type	Description
AHDY01	LIMIT	Fixed/Split-Range/Cas-Master
AHHY01	LIMIT	Fixed/Split-Range/Cas-Master
AHY01	LIMIT	Fixed/Split-Range/Cas-Master
ALDY01	LIMIT	Fixed/Split-Range/Cas-Master
ALLY01	LIMIT	Fixed/Split-Range/Cas-Master
ALY01	LIMIT	Fixed/Split-Range/Cas-Master
DEVY01	ANALOG	Fixed/Split-Range/Cas-Master
KPY01	ANALOG	Fixed/Split-Range/Cas-Master
O01	BINARY	Fixed/Split-Range/Cas-Master
O02	BINARY	Fixed/Split-Range/Cas-Master
O03	BINARY	Fixed/Split-Range/Cas-Master
O04	BINARY	Fixed/Split-Range/Cas-Master
O05	BINARY	Fixed/Split-Range/Cas-Master
O06	BINARY	Fixed/Split-Range/Cas-Master
O07	BINARY	Fixed/Split-Range/Cas-Master
O08	BINARY	Fixed/Split-Range/Cas-Master
O09	BINARY	Fixed/Split-Range/Cas-Master

Signal	Data Type	Description
O10	BINARY	Fixed/Split-Range/Cas-Master
O11	BINARY	Fixed/Split-Range/Cas-Master
O12	BINARY	Fixed/Split-Range/Cas-Master
O13	BINARY	Fixed/Split-Range/Cas-Master
O14	BINARY	Fixed/Split-Range/Cas-Master
O15	BINARY	Fixed/Split-Range/Cas-Master
O16	BINARY	Fixed/Split-Range/Cas-Master
O17	BINARY	Fixed/Split-Range/Cas-Master
O18	BINARY	Fixed/Split-Range/Cas-Master
O19	BINARY	Fixed/Split-Range/Cas-Master
TDMY01	ANALOG	Fixed/Split-Range/Cas-Master
TDPY01	ANALOG	Fixed/Split-Range/Cas-Master
TIMY01	ANALOG	Fixed/Split-Range/Cas-Master
TIPY01	ANALOG	Fixed/Split-Range/Cas-Master
TSTA01	PACKED	Fixed/Split-Range/Cas-Master
VDPY01	ANALOG	Fixed/Split-Range/Cas-Master
VD-Y01	ANALOG	Fixed/Split-Range/Cas-Master
WAY01	ANALOG	Fixed/Split-Range/Cas-Master
WSTA01	PACKED	Fixed/Split-Range/Cas-Master
XAY01	ANALOG	Fixed/Split-Range/Cas-Master
XSTA01	PACKED	Fixed/Split-Range/Cas-Master
Y02	ANALOG	Fixed/Split-Range/Cas-Master
YAY01	ANALOG	Fixed/Split-Range/Cas-Master
YSTA01	PACKED	Fixed/Split-Range/Cas-Master

Table 1.2 Function Diagram Output References

1.2.3 I/O Modules

Function Block	Name	Library	Description
2WEX-00	PC_CTRL_1	I/O	HW in analog Ex (CAI10Ex) 2 wire
AOEX-00	PC_CTRL_1	I/O	HW - Out analog Ex (CAO10Ex) standard

Table 1.3 I/O Modules

1.2.4 Diagram Input References

The diagram input references are connected internal and not connecte4d for external connection in this function diagram template.

1.3 Function Template

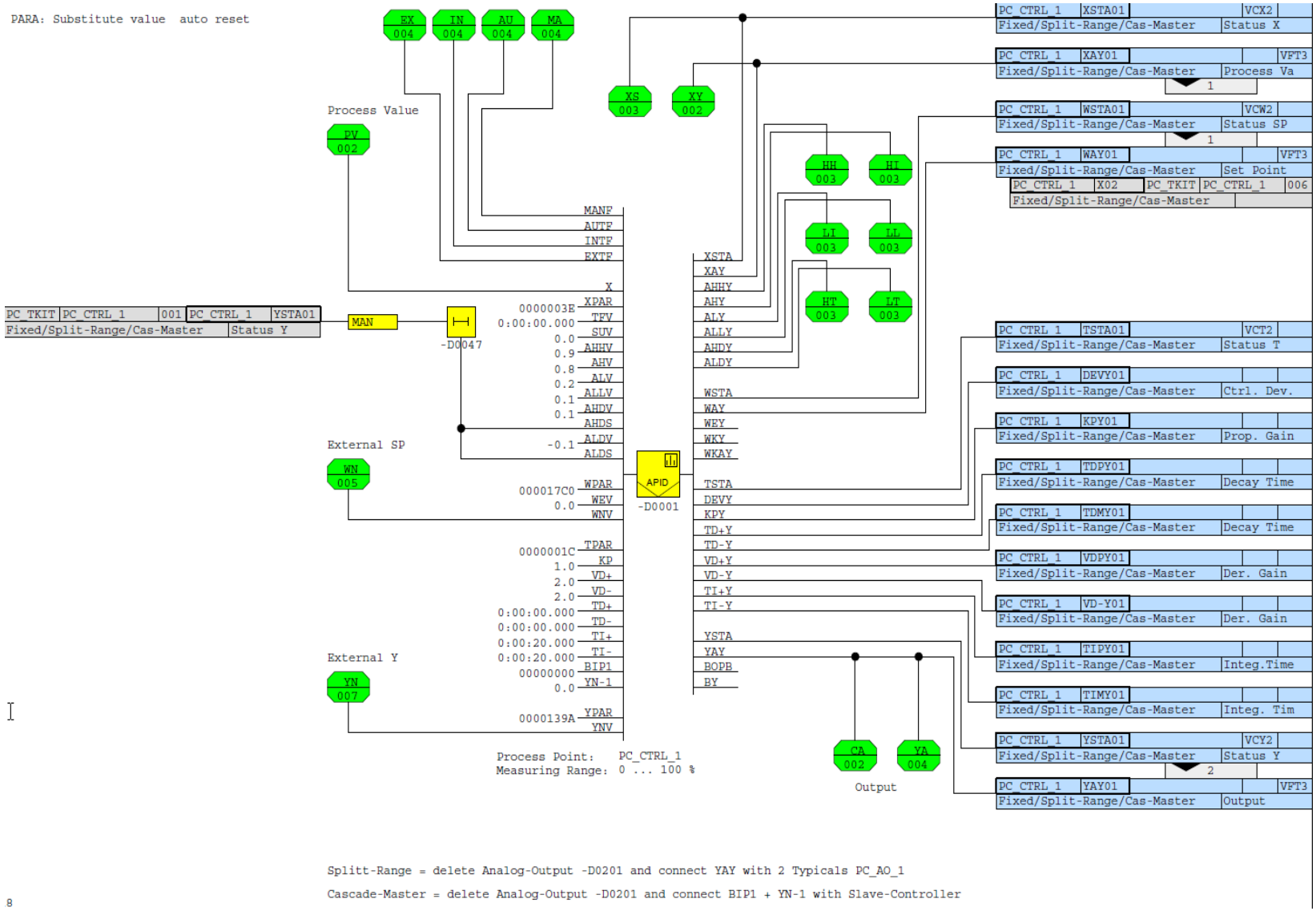

Figure 1.1 Function Template PC_CTRL_1 (Page 1/8)

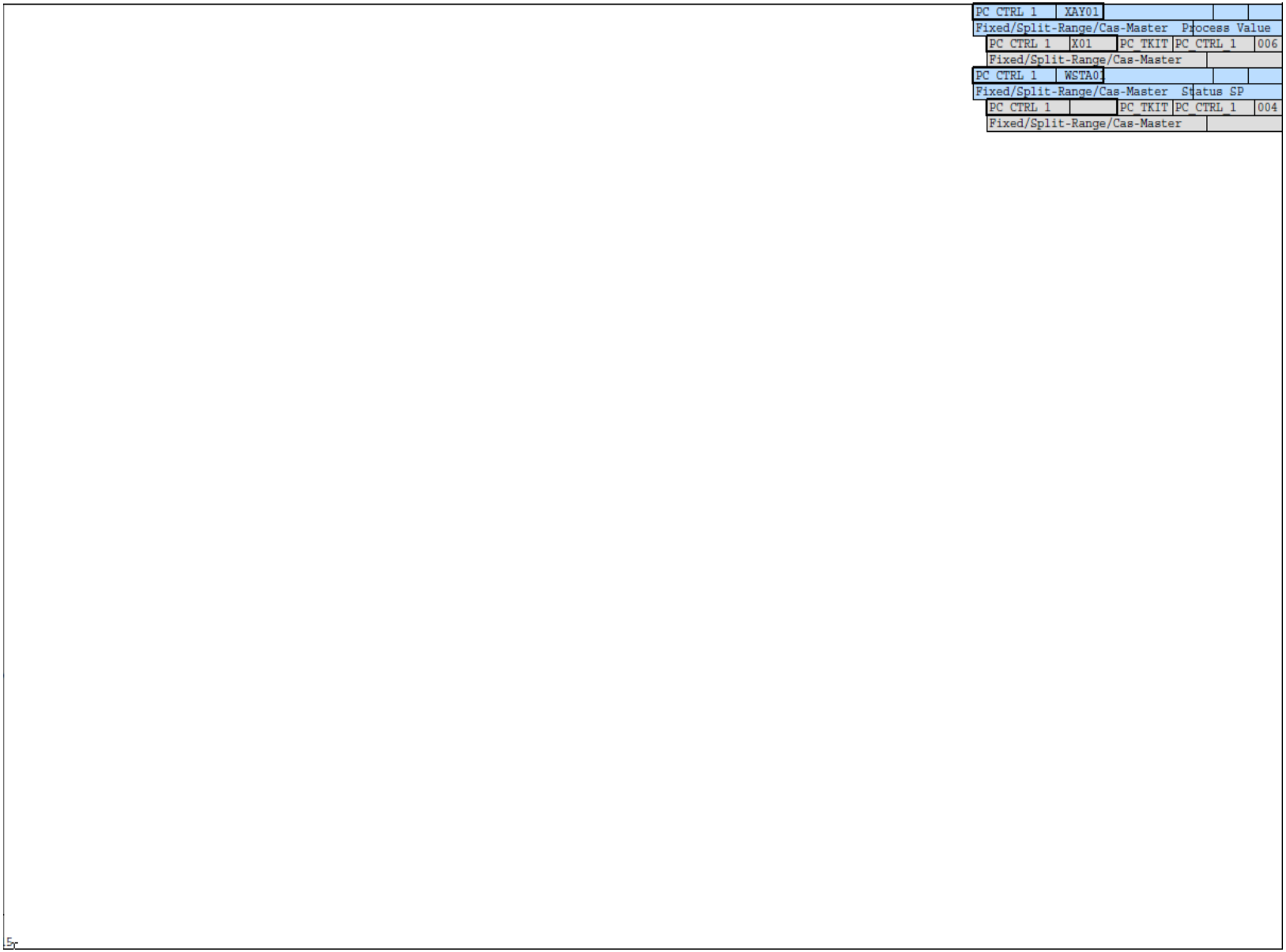

Figure 1.2 Function Template PC_CTRL_1 (Page 2/8)

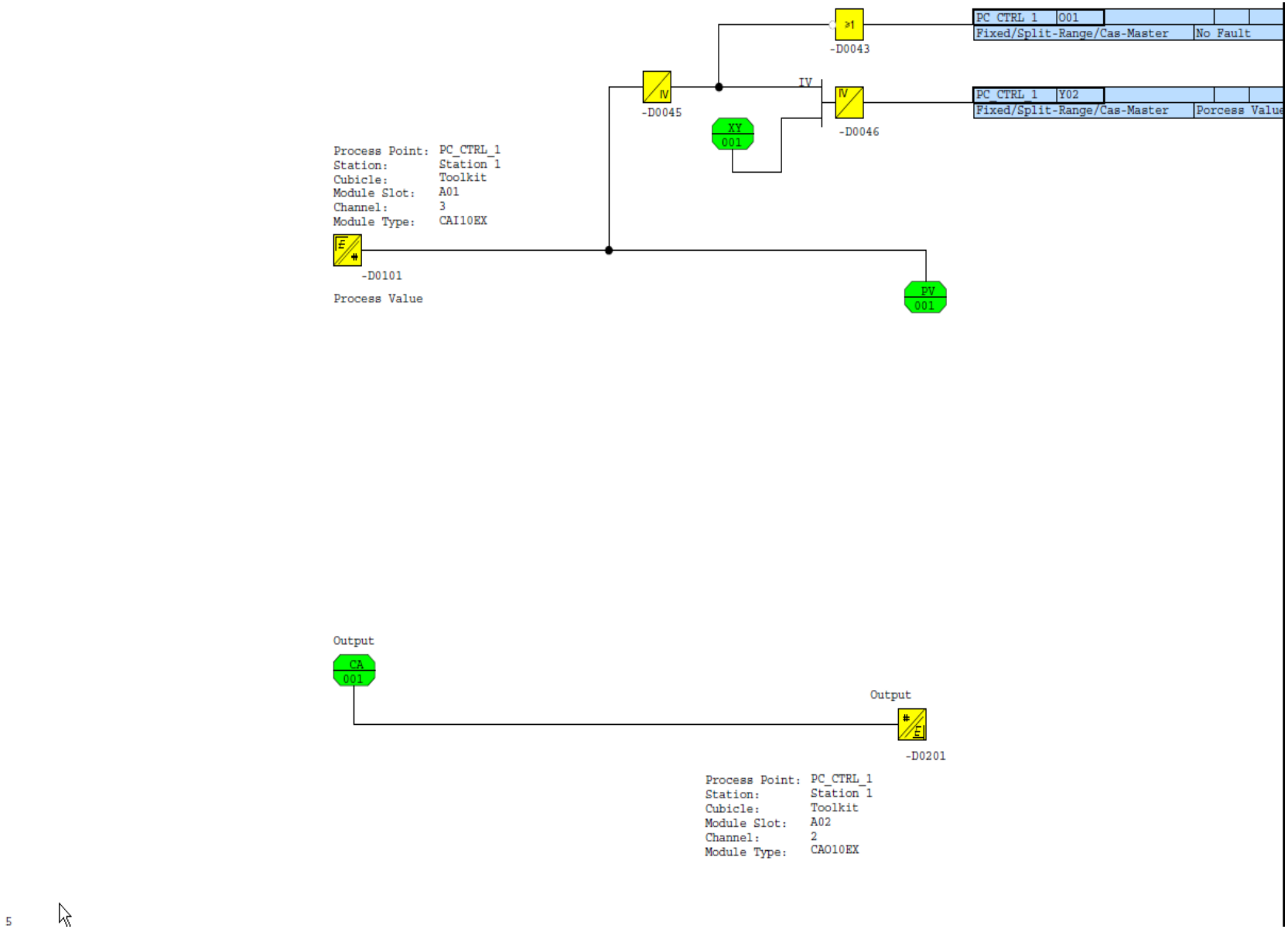

Figure 1.3 Function Template PC_CTRL_1 (Page 3/8)

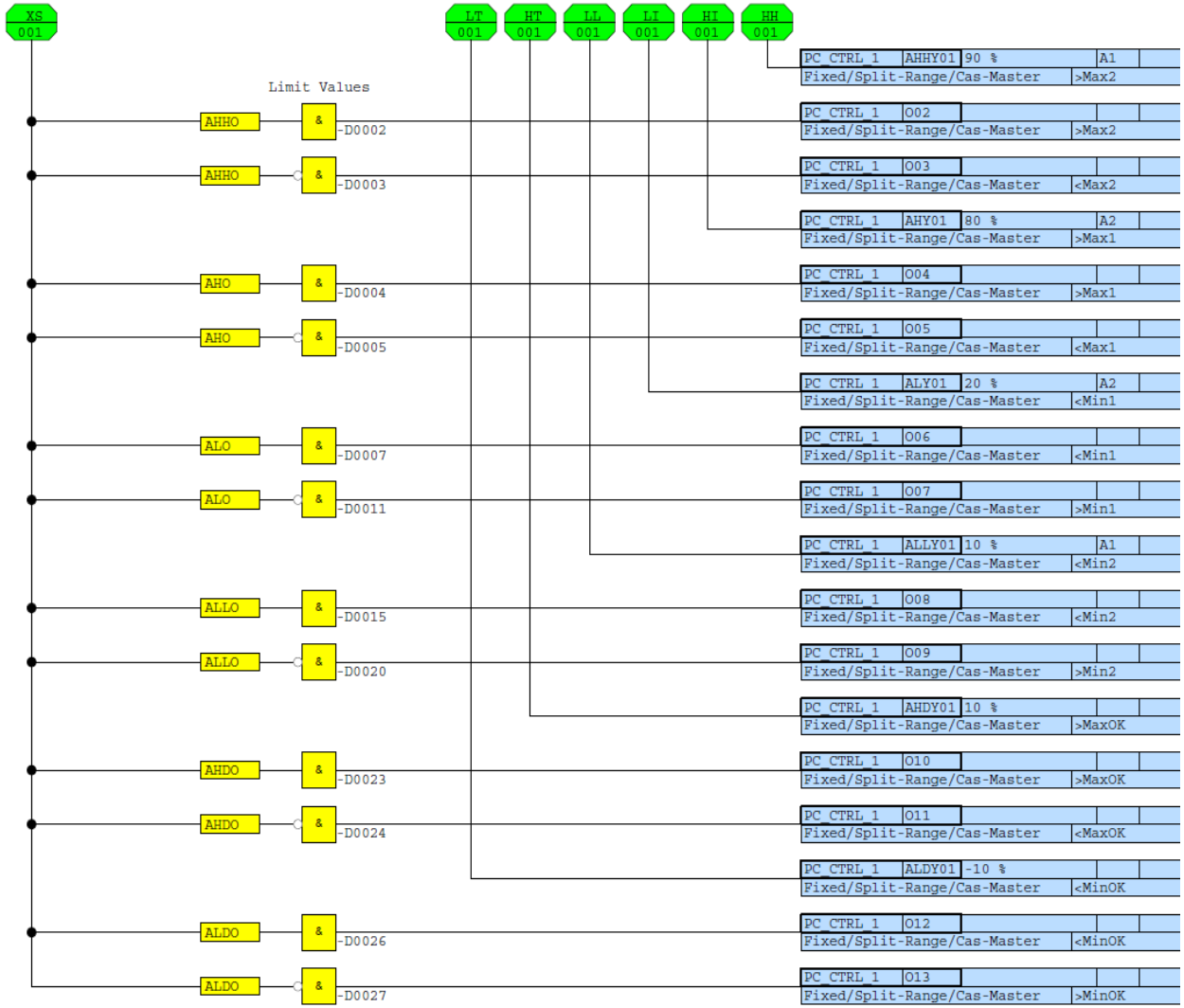

Figure 1.4 Function Template PC_CTRL_1 (Page 4/8)

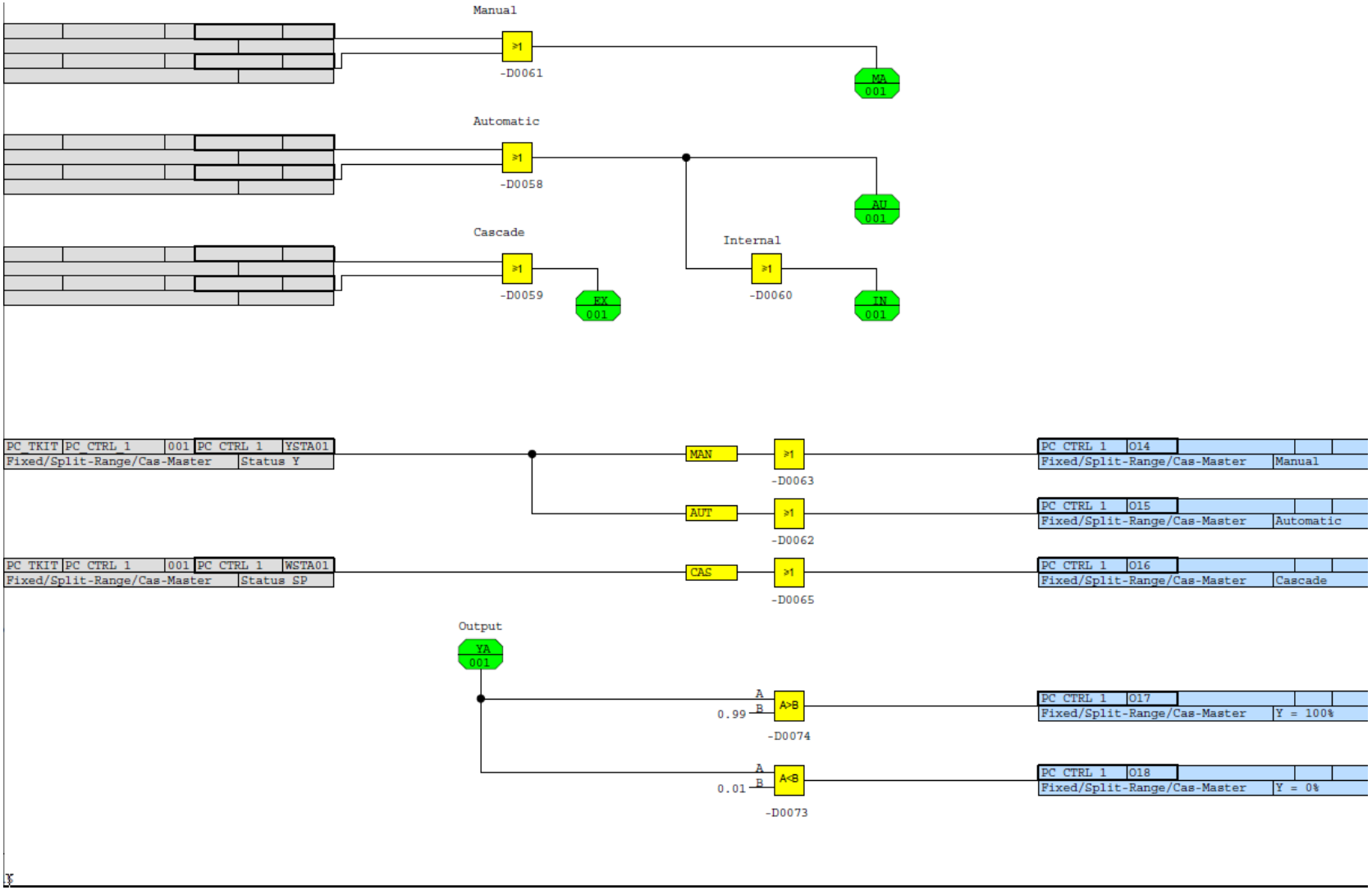

Figure 1.5 Function Template PC_CTRL_1 (Page 5/8)

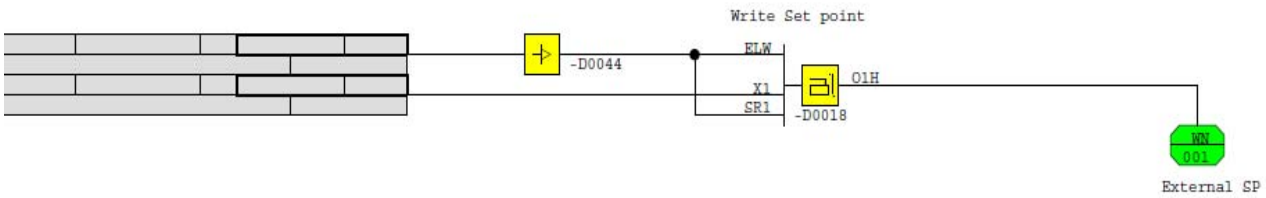

Figure 1.6 Function Template PC_CTRL_1 (Page 6/8)

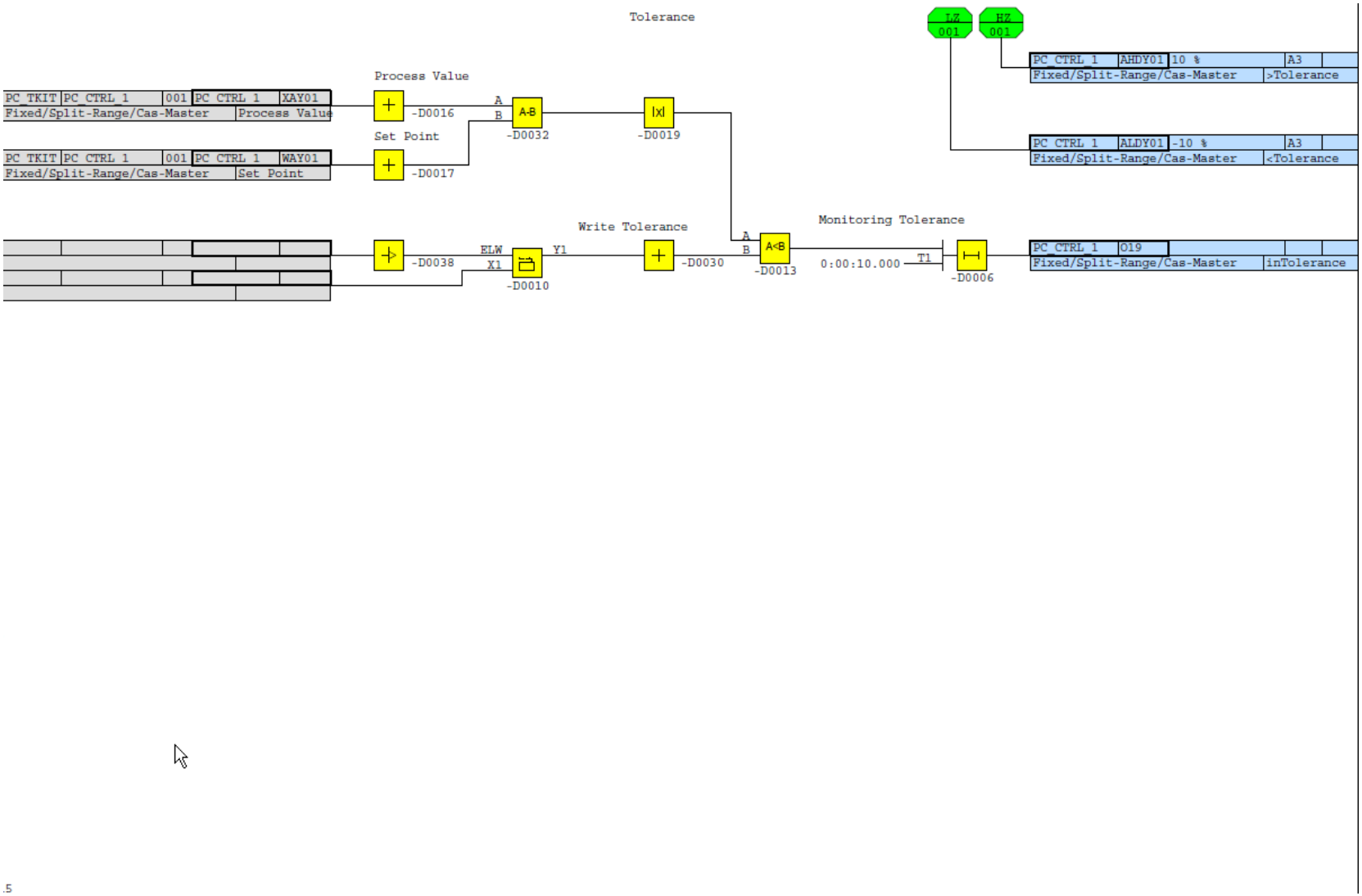

Figure 1.7 Function Template PC_CTRL_1 (Page 7/8)

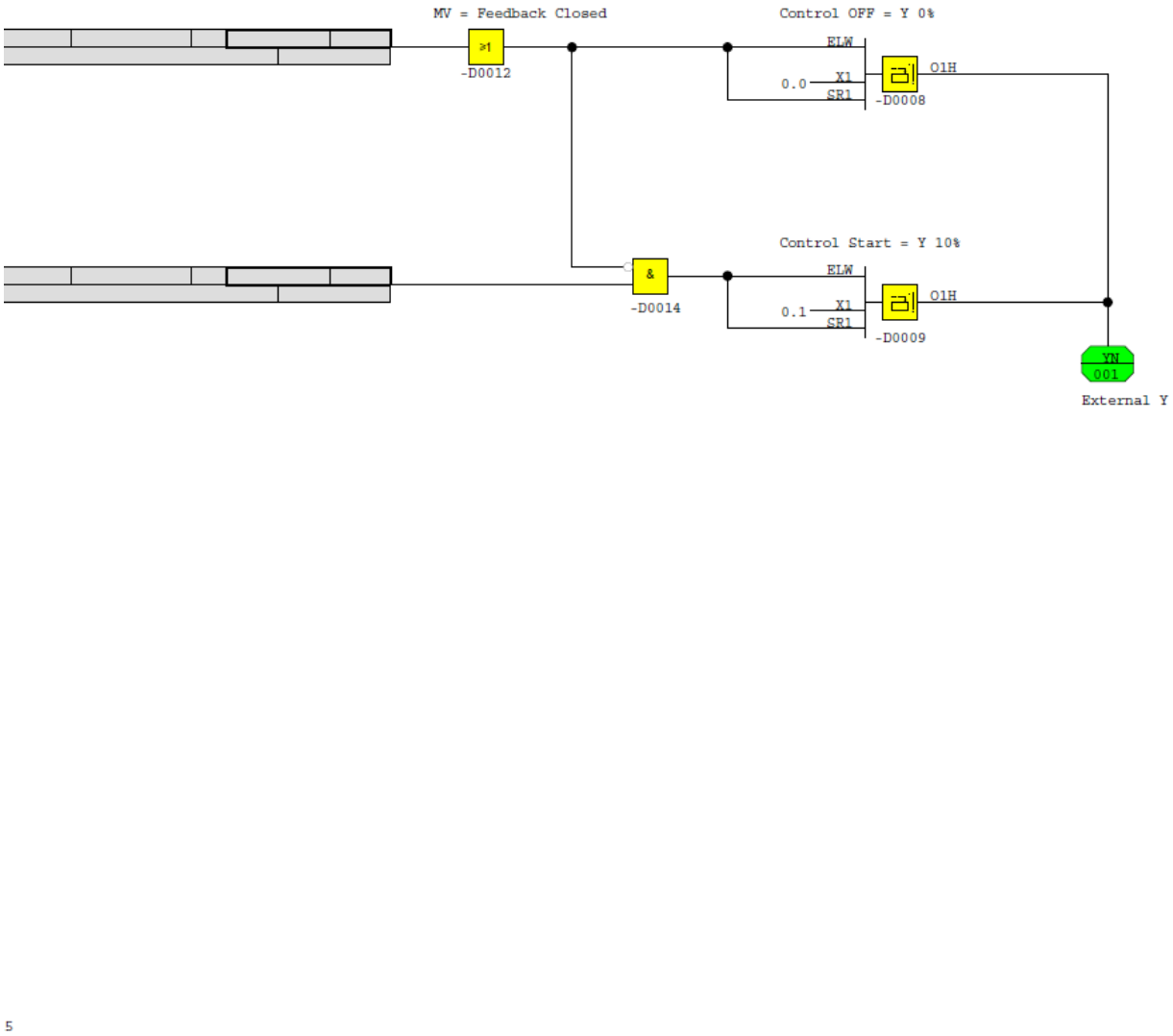

Figure 1.8 Function Template PC_CTRL_1 (Page 8/8)

1.4 Configurable Parameters

The following parameters are in the function diagram template and can be engineered using Excel sheet data mechanisms.

In general function block parameters and signals can be exported to Excel sheet and can be engineered and imported.

1.4.1 Function Blocks

The visible and not connected parameters in the function diagram template are in **Bold**.

PC_CTRL_1

Function Block	Input	Value	Data Type	Description
ADD-R0	X1	0.0	Real	Input real
APIDL-00	AHB	0.01	Real	H-limit hysteresis
APIDL-00	AHD	0	Bool	Disable H-limit
APIDL-00	AHDB	0.01	Real	H-tolerance hysteresis
APIDL-00	AHDD	0	Bool	Disable H-tolerance limit
APIDL-00	AHDS	Connected	Bool	H-tolerance message suppr.
APIDL-00	**AHDV**	**0.1**	**Real**	**H-tolerance value**
APIDL-00	AHHB	0.01	Real	HH-limit hysteresis
APIDL-00	AHHD	0	Bool	Disable HH-limit
APIDL-00	AHHS	0	Bool	HH-limit message suppr.
APIDL-00	**AHHV**	**0.9**	**Real**	**HH-limit value**
APIDL-00	AHS	0	Bool	H-limit message suppr.
APIDL-00	AHTB	0.01	Real	H-transient hysteresis
APIDL-00	AHTD	0	Bool	Disable H-transient limit
APIDL-00	AHTS	0	Bool	H-transient message suppr.
APIDL-00	AHTV	0.7	Real	H-transient value
APIDL-00	**AHV**	**0.8**	**Real**	**H-limit value**
APIDL-00	AII	0	Bool	Interlock AUT
APIDL-00	AKFR	0	Bool	Reset access lock
APIDL-00	AKFS	0	Bool	Set access lock
APIDL-00	ALB	0.01	Real	L-limit hysteresis
APIDL-00	ALD	0	Bool	Disable L-limit
APIDL-00	ALDB	0.01	Real	L-tolerance hysteresis
APIDL-00	ALDD	0	Bool	Disable L-tolerance limit
APIDL-00	ALDS	Connected	Bool	L-tolerance message suppr.

Function Block	Input	Value	Data Type	Description
APIDL-00	**ALDV**	**-0.1**	**Real**	**L-tolerance value**
APIDL-00	ALLB	0.01	Real	LL-limit hysteresis
APIDL-00	ALLD	0	Bool	Disable LL-limit
APIDL-00	ALLS	0	Bool	LL-limit message suppr.
APIDL-00	**ALLV**	**0.1**	**Real**	**LL-limit value**
APIDL-00	ALS	0	Bool	L-limit message suppr.
APIDL-00	ALTB	0.01	Real	L-transient hysteresis
APIDL-00	ALTD	0	Bool	Disable L-transient limit
APIDL-00	ALTS	0	Bool	L-transient message suppr.
APIDL-00	ALTV	0.3	Real	L-transient value
APIDL-00	**ALV**	**0.2**	**Real**	**L-limit value**
APIDL-00	ARB	1.0	Real	End position ARW band
APIDL-00	ARN	0	Bool	End position I-behaviour
APIDL-00	ATRV	0.0	Real	Transient value defin. ext.
APIDL-00	ATV	0.670166	Real	Alternative value
APIDL-00	AUTF	Connected	Real	Mode of operation AUT
APIDL-00	**BIP1**	**00000000**	**Packed Bool**	**Balancing request from slave**
APIDL-00	BRT	0:00:10.000	Duration	Switchov. filter time const.
APIDL-00	BT	0:00:10.000	Duration	Sync. value transient time
APIDL-00	C1	0.0	Real	Offset
APIDL-00	CII	0	Bool	Interlock DDC
APIDL-00	COMF	0	Bool	Mode of operation DDC
APIDL-00	COMH	0	Bool n	DDC error-free
APIDL-00	COMV	00000000	LVR	Computer value
APIDL-00	CUT	0.05	Real	Threshold square root extr.
APIDL-00	DAC1	0.0	Real	e processing offset
APIDL-00	DAF1	0	Integer	e processing arithmetic type
APIDL-00	DAK1	1.0	Real	e processing gain
APIDL-00	DAX1	0.0	Real	e processing aux. variable
APIDL-00	DBV	0.0	Real	Dead band value
APIDL-00	DDN	0	Bool	D-ratio dead band off
APIDL-00	DIN	0	Bool	I-ratio dead band off
APIDL-00	DN-	1	Bool	D-ratio switchoff minus
APIDL-00	DN+	1	Bool	D-ratio switchoff plus
APIDL-00	DPN	0	Bool	P-ratio dead band off

Function Block	Input	Value	Data Type	Description
APIDL-00	EII	0	Bool	Interlock EXT
APIDL-00	EXTF	Connected	Bool	Mode of operation EXT
APIDL-00	FI1	0	Bool	Backup input boolean
APIDL-00	FIP1	00000000	Packed Bool	Backup input PBool
APIDL-00	FX1	0.0	Real	Backup input real
APIDL-00	HV	1.05	Real	H-limit reached
APIDL-00	III	0	Bool	Interlock INT
APIDL-00	IN-	0	Bool	I-ratio switchoff minus
APIDL-00	IN+	0	Bool	I-ratio switchoff plus
APIDL-00	INTF	Connected	Bool	Mode of operation INT
APIDL-00	IV	0	Bool	Invalid
APIDL-00	K1	1.0	Real	Weighting factor K
APIDL-00	KCN	0	Bool	Switchoff compens. Kp change
APIDL-00	**KP**	**1.0**	**Real**	**Proportional gain**
APIDL-00	LKFR	0	Bool	Interl. mode switchov. reset
APIDL-00	LKFS	0	Bool	Interl. mode switchov. set
APIDL-00	LOCI	0	Bool	Local intervention
APIDL-00	LOCV	0.0	Real	Local intervention value
APIDL-00	LV	-0.05	Real	L-limit
APIDL-00	MANF	Connected	Bool	Mode of operation MAN
APIDL-00	MDO	00000000	Packed Bool	Oper. word operation
APIDL-00	MII	0	Bool	Interlock MAN
APIDL-00	OVT1	1	Bool	Override type for signal n
APIDL-00	OVTI	0	Bool	Override type slave contr.
APIDL-00	OVV1	-1.0	Real	Override signal n
APIDL-00	PN	0	Bool	Switchoff P-ratio
APIDL-00	**SUV**	**0.0**	**Real**	**Substitute value**
APIDL-00	**TD-**	**0:00:00.000**	**Duration**	**Decay time minus**
APIDL-00	**TD+**	**0:00:00.000**	**Duration**	**Decay time plus**
APIDL-00	TFB	2.0	Real	Linear range NIFIL
APIDL-00	**TFV**	**0:00:00.000**	**Duration**	**Filter time constant**
APIDL-00	**TI-**	**0:00:20.000**	**Duration**	**Integration time minus**
APIDL-00	**TI+**	**0:00:20.000**	**Duration**	**Integration time plus**
APIDL-00	**TPAR**	**0000001C**	**Packed Bool**	**Parameter setting time func.**
APIDL-00	TRT	0:00:05.000	Duration	Transient reset delay

Function Block	Input	Value	Data Type	Description
APIDL-00	TRV	2.0	Real	Transient value
APIDL-00	**VD-**	**2.0**	**Real**	**Derivative gain minus**
APIDL-00	**VD+**	**2.0**	**Real**	**Derivative gain plus**
APIDL-00	WAC1	0.0	Real	Aux. variable offset
APIDL-00	WAF1	0	Integer	Selection comp. function
APIDL-00	WAK1	1.0	Real	Aux. variable gain
APIDL-00	WAX1	0.0	Real	Input aux. variable
APIDL-00	WBN	0	Bool	Disable limitation for W
APIDL-00	WCV	0.0	Real	Offset set point Wext.
APIDL-00	WET	0:00:10.000	Duration	Time for bump sm. filter
APIDL-00	**WEV**	**0.0**	**Real**	**External set point**
APIDL-00	WHN	0	Bool	Disable H-limit
APIDL-00	WHV	1.0	Real	H-limit value
APIDL-00	WHVS	1.0	Real	H-limit standard
APIDL-00	WKC	0.0	Real	Offset ratio for Wext.
APIDL-00	WKHV	1.05	Real	H-limit ratio
APIDL-00	WKK	1.0	Real	Gain for ratio
APIDL-00	WKLV	-0.05	Real	L-limit ratio
APIDL-00	WKV	1.0	Real	Ratio value for Wext.
APIDL-00	WLN	0	Bool	Disable L-limit
APIDL-00	WLV	0.0	Real	L-limit value
APIDL-00	WLVS	0.0	Real	L-limit standard
APIDL-00	WN-	0	Bool	Stop minus direction
APIDL-00	WN+	0	Bool	Stop plus direction
APIDL-00	WNH	Connected	Bool	Hold last value
APIDL-00	WNV	00000000	LVR	Set point control
APIDL-00	WOV	0.0666667	Real	Set point operator
APIDL-00	**WPAR**	**000017C0**	**Packed Bool**	**Parameter setting W-function**
APIDL-00	WRN	0	Bool	Disable gradient limitation
APIDL-00	WRT-	0:00:00.000	Duration	Value gradient limit. minus
APIDL-00	WRT+	0:00:00.000	Duration	Value gradient limit. plus
APIDL-00	X	Connected	Real	Input real
APIDL-00	XAC1	0.0	Real	Aux. variable offset
APIDL-00	XAF1	0	Integer	Selection comp. function
APIDL-00	XAK1	1.0	real	Aux. variable gain

Function Block	Input	Value	Data Type	Description
APIDL-00	XAX1	0.0	BReal	Input aux. variable
APIDL-00	**XPAR**	**0000003E**	**Packed Bool**	**Parameter setting X-function**
APIDL-00	XX1	1.0	Real	Coordinate X
APIDL-00	XY1	1.0	Real	Coordinate Y
APIDL-00	YAC1	0.0	Real	Aux. variable offset
APIDL-00	YAF1	0	Integer	Selection comp. function
APIDL-00	YAK1	1.0	Real	Aux. variable gain
APIDL-00	YAX1	0.0	Real	Input aux. variable
APIDL-00	YBN	0	Bool	Disable limitation for Y
APIDL-00	YCRD	0	Bool	Selection start value 100 %
APIDL-00	YFSS	0	Bool	Forced switch-off
APIDL-00	YFSV	0.0	Real	Value for forced switch-off
APIDL-00	YHN	0	Bool	Disable H-limit
APIDL-00	YHV	1.0	Real	H-limit value
APIDL-00	YHVS	1.0	Real	H-limit standard
APIDL-00	YLN	0	Bool	Disable L-limit
APIDL-00	YLV	0.0	Real	L-limit value
APIDL-00	YLVS	0.0	Real	L-limit standard
APIDL-00	YN-	0	Bool	Stop minus direction
APIDL-00	YN+	0	Bool	Stop plus direction
APIDL-00	**YN-1**	**0.0**	**Real**	**Yn-1**
APIDL-00	YNH	0	Bool	Y hold last value
APIDL-00	YNV	Connected	LVR	Y substitute value extern
APIDL-00	YOV	0.0	Real	Positioning variable oper.
APIDL-00	**YPAR**	**0000139A**	**Packed Bool**	**Parameter setting Y-function**
APIDL-00	YRN	0	Bool	Disable gradient limitation
APIDL-00	YRT-	0:00:00.000	Duration	Value gradient limit. minus
APIDL-00	YRT+	0:00:00.000	Duration	Value gradient limit. plus
BSFUP_P	BIT	12	Bool	
BSFUP_P	BIT	2	Bool	
BSFUP_P	BIT	24	Bool	
BSFUP_P	BIT	24	Bool	
BSFUP_P	BIT	25	Bool	
BSFUP_P	BIT	25	Bool	
BSFUP_P	BIT	26	Duration	

Function Block	Input	Value	Data Type	Description
BSFUP_P	BIT	26	Bool	
BSFUP_P	BIT	27	Bool	
BSFUP_P	BIT	27	Bool	
BSFUP_P	BIT	28	Bool	
BSFUP_P	BIT	28	Bool	
BSFUP_P	BIT	29	Bool	
BSFUP_P	BIT	29	Bool	
BSFUP_P	BIT	2	Bool	
BSFUP_P	BIT	3	Bool	
DELAY-00	RS1	0	Bool	Reset
DELAY-00	RS1	0	Bool	Reset
DELAY-00	RS2	0	Bool	Reset
DELAY-00	RS2	0	Bool	Reset
DELAY-00	**T1**	**0:00:10.000**	**Duration**	**Delay in starting**
DELAY-00	T1	0:00:00.000	Duration	Delay in starting
DELAY-00	T2	0:00:00.000	Duration	Drop delay
DELAY-00	T2	0:00:00.000	Duration	Drop delay
DYNOR-00	T	0:00:02.000	Duration	Time value
DYNOR-00	T	0:00:02.000	Duration	Time value
GT-R0	**B**	**0.99**	**Real**	**Input real**
LE-R0	**B**	**0.01**	**Real**	**Input real**
LWRNV-R0	PARA	00000001	Packed Bool	PBool
LWRNV-R0	PARA	00000001	Packed Bool	PBool
LWRNV-R0	PARA	00000001	Packed Bool	PBool
LWRNV-R0	**X1**	**0.0**	**Real**	**Input real**
LWRNV-R0	**X1**	**0.1**	**Real**	**Input real**
LWR-R0	PARA	00000001	Packed Bool	PBool

Table 1.4 Parameters of Function Block PC_CTRL_1

1.4.2 IO Modules

PC_CTRL_1

Function Block	Input	Value	Data Type	Description
AOEX-00	CY1	0	Bool	Falling characteristic
AOEX-00	EBMO	1	Bool	Elec. burden monitoring

Function Block	Input	Value	Data Type	Description
AOEX-00	LZ	1	Bool	Keep last value
AOEX-00	SUV	0.0	Real	Live Zero
AOEX-00	SUV_LAV	0	Bool	Substitute value definition
AOEX-00	SUV_ON	0	Bool	Substitute value on

Table 1.5 Parameters of IO Module PC_CTRL_1

PC_CTRL_1

Function Block	Input	Value	Data Type	Description
2WEX-00	HV	1.1001	Real	Max. threshold
2WEX-00	LINR	1.0	Real	MIn. threshold
2WEX-00	LV	0.149902	Real	Filter Time constant
2WEX-00	NLF	1	Bool	Tolerance band
2WEX-00	TF1	0:00:02.000	Duration	Non-linear filter
2WEX-00	TOLB	0.00976562	Real	Linear range

Table 1.6 Parameters of IO Module PC_CTRL_1

1.4.3 Diagram Output References / Signal Parameters

PC_CTRL_1

Signal	Data Type	Value High	Value Low	Alarm Template	Archive Template
AHDY01	LIMIT	>MaxOK	<MaxOK		
AHHY01	LIMIT	>Max2	<Max2	A1	
AHY01	LIMIT	>Max1	<Max1	A2	
ALDY01	LIMIT	<MinOK	>MinOK		
ALLY01	LIMIT	<Min2	>Min2	A1	
ALY01	LIMIT	<Min1	>Min1	A2	
DEVY01	ANALOG	Ctrl. Dev.			
KPY01	ANALOG	Prop. Gain			
O01	BINARY	No Fault			
O02	BINARY	>Max2			
O03	BINARY	<Max2			
O04	BINARY	>Max1			
O05	BINARY	<Max1			
O06	BINARY	<Min1			
O07	BINARY	>Min1			

Signal	Data Type	Value High	Value Low	Alarm Template	Archive Template
O08	BINARY	<Min2			
O09	BINARY	>Min2			
O10	BINARY	>MaxOK			
O11	BINARY	<MaxOK			
O12	BINARY	<MinOK			
O13	BINARY	>MinOK			
O14	BINARY	Manual			
O15	BINARY	Automatic			
O16	BINARY	Cascade			
O17	BINARY	Y = 100%			
O18	BINARY	Y = 0%			
O19	BINARY	inToleranc			
TDMY01	ANALOG	Decay Time			
TDPY01	ANALOG	Decay Time			
TIMY01	ANALOG	Integ. Tim			
TIPY01	ANALOG	Integ.Time			
TSTA01	PACKED	Status T		VCT2	
VDPY01	ANALOG	Der. Gain			
VD-Y01	ANALOG	Der. Gain			
WAY01	ANALOG	Set Point			Fast_7d
WSTA01	PACKED	Status SP		VCY2	
XAY01	ANALOG	Process Va			Fast_7d
XSTA01	PACKED	Status X		VCX2	
Y02	ANALOG	Porcess Va			
YAY01	ANALOG	Output			Fast_7d
YSTA01	PACKED	Status Y		VCY2	

Table 1.7 Signal Parameters of PC_CTRL_1

1.5 Additional Information

- The substitute value strategy is realized in the function block using the input “PARA” (hold last valid value or substitute value with auto reset).
- In addition to them an alternative value can be activated independent from the invalidity status of the function.
- In the input configuration of “X” and in the tab quality a substitute value (actual value or a fixed value) can be defined.

1.6 Performance of the function module in a fault scenario

In a fault scenario the module will generate an alarm/event and the function diagram output reference “O01” will be set to true.

2. Document References

Ref.	Document title	Document number
/1/	System 800xA PC Toolkit Library for Melody – Operation, User Manual	3BDA033439R5101EN
/2/	System 800xA PC Toolkit Library for Melody – Installation and Configuration, User Manual	3BDA033456R5103EN
/3/	S+ Engineering Function Blocks Operation	2VAA000580-530
/4/	S+ Control – Melody – Analog Input	2VAA000592-100
/5/	S+ Control – Melody – Analog Output	2VAA000594-100
/6/	S+ Engineering: Function Block APID	2VAA000575-530
/7/	S+ Engineering: Function Blocks Analog / Binary	2VAA000571-530
/8/	S+ Engineering: Function Blocks Binary	2VAA000572-530
/9/	S+ Engineering: Function Blocks Analog	2VAA000570-530

Table 2.1 References

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