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1 CONFIGURATION LOGIC CIRCUITS

1.1 Application

Different protection, control and monitoring functions within the REx 5xx protection, control and monitoring terminals are quite independent as far as their configuration within the terminal is concerned. The user can not enter and change the basic algorithms for different functions, since they are located in the digital signal processors and extensively type tested. Different configurations of functions within the terminals can be set up in the best possible way so as to suit various special requirements for different applications.

For this purpose, a few additional logic circuits are necessary. These allow the user to configure the terminals according to his needs and also to build in some special logic circuits, employing different logic gates and timers.

1.2 Design

The blocks of configuration logic circuits, as shown in Fig. 1, are built into each REx 5xx terminal and are thus available to the user.

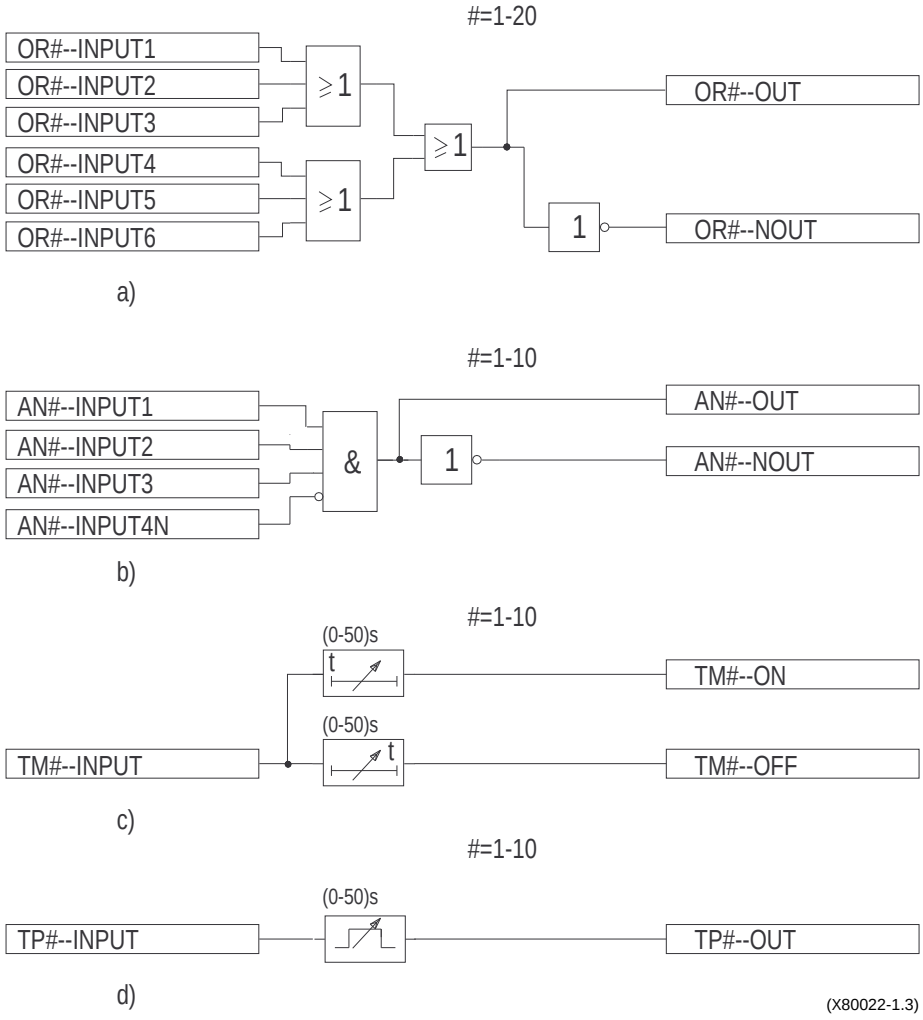

Fig. 1 Block diagram of the configuration logic circuits as built into the REx 5xx terminals

The configuration logic OR gates - as shown in Fig. 1a - have six inputs, designated ORn--INPUTm, where n runs from 1 to 20 and presents the serial number of the block, and m presents the serial number of the inputs in the block. Each OR circuit has two outputs, ORn--OUT and ORn--NOUT (inverted).

The configuration logic AND gates - as shown in Fig. 1b - have four inputs (one of them inverted), designated ANn--INPUTm (ANn--INPUTNm is inverted), where n runs from 1 to 10 and presents the serial number of the block, and m presents the serial number of the inputs in the block. Each AND circuit has two outputs, ANn--OUT and ANn--NOUT (inverted).

The configuration logic TM timers delayed at pick-up and at drop-out - as shown in Fig. 1c - have a settable time delay between 0 and 50,00 s in steps of 0,01 s. The input signal for each time delay block has the designation TMn--INPUT, where n runs from 1 to 10 and presents the serial number of the logic block. The output signals of each time delay block are TMn--ON and TMn--OFF. The first one belongs to the timer delayed on pick-up and the second one to the timer delayed on drop-out. Both timers within one block have always the same setting.

The configuration logic pulse timers TP - as shown on Fig. 1d - have a settable length of a pulse between 0 and 50,00 s in steps of 0,01 s. The input signal for each pulse timer has the designation TPn--INPUT, where n runs from 1 to 10 and presents the serial number of the logic block. Each pulse timer has one output, designated by TPn--OUT.

The appendix, attached to this description of the configuration logic circuits (CLC), gives the following information:

- a simplified terminal diagram of the CLC
- a terminal diagram for the CLC
- a description of the connection and production signals for the CLC
- a description of the setting parameters for the CLC

1.3 Setting instructions

Time delays and pulse lenghts for the different timers must be set under the sub menu:

Configuration
FunctionInputs
LogicTM (LogicTP)

Both timers in the same logic block (the one delayed on pick-up and the one delayed on drop-out) have always a common setting value. Setting value of the pulse length is independent on one another for all pulse circuits.

Setting values of time delays for different timers must correspond to the requirements on time delay for each separate logic circuit with built in timer.

1.4 Configuration

Execution of functions as defined by the CLC blocks runs in a fixed priority sequence. Execution of different blocks follows the same order as their serial numbers, starting always by n = 1. It is necessary to consider this fact always when connecting in series two or more logical gates from blocks with different serial numbers. OR function in the same logic block will also be executed before the AND function.

For this reason it is necessary to design the logic circuits carefully and check always the execution sequence for different functions. In the opposite cases additional time delays must be introduced into the logic schemes to prevents them against possible false operations.

When a negating function is used in a logic consisting of several logic blocks, the negation is not necessarily active in the first program loop after a status change. This can also cause false operations if not considered in the design of logic functions.

To safeguard against these false operations, a final time delay have to be added to the logics with negating functions utilising several AND and/or OR gates connected in series as well as to the logic circuits where the logic OR and AND gates do not follow one another with increasing serial numbers. This time delay needs to be at least the number of gates connected in series, multiplied by 8 ms. For an example see Fig. 2. When such a time delay can not be accepted, please contact ABB Relays AB for consulting.

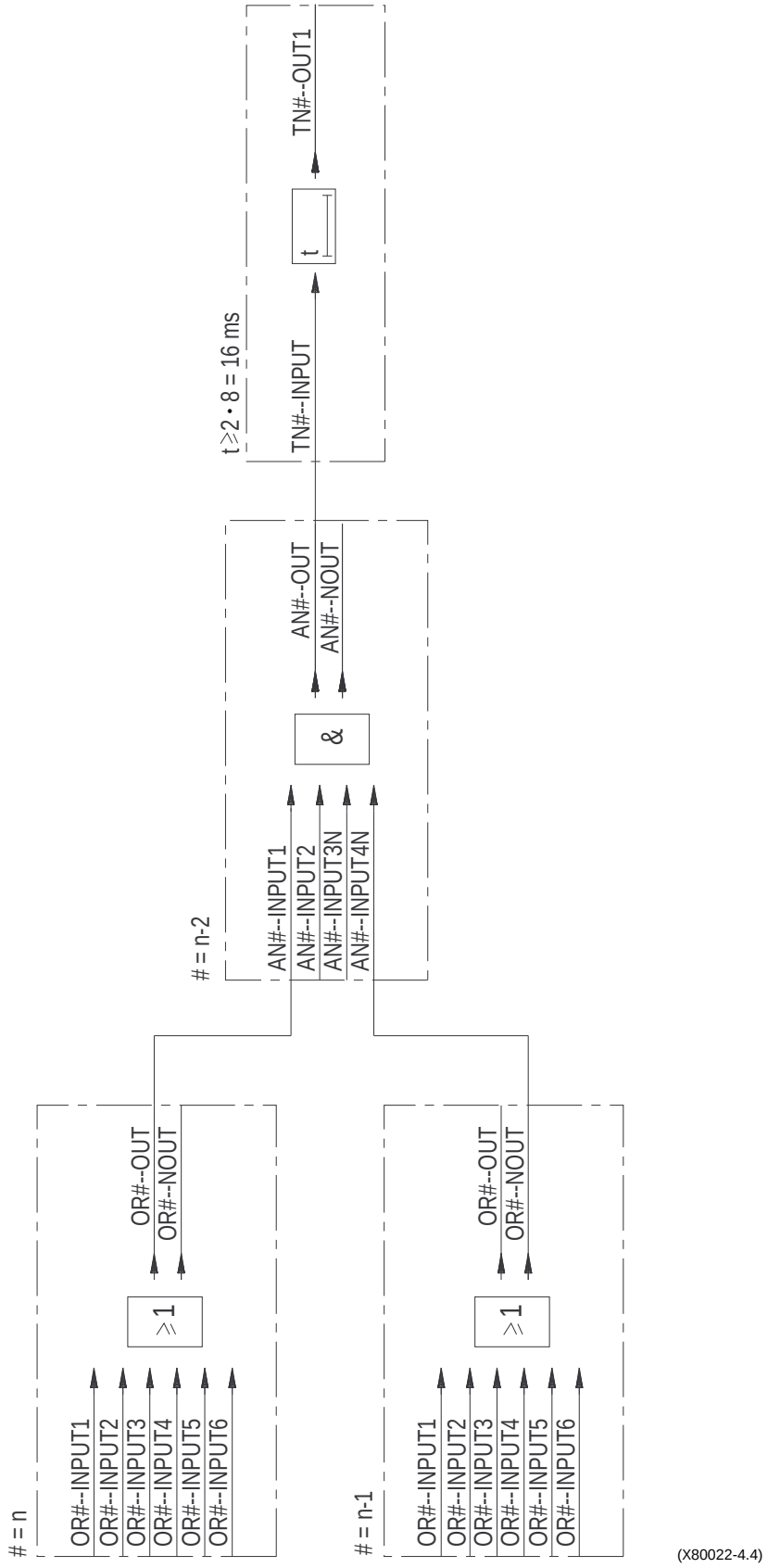

Fig. 2 Example of logic with negating function or inverse order of logic gates.

1.5 Testing

Testing of the separate configuration logic circuits can be carried out for each group and each circuit separately. For each block it is thus necessary to configure all input signals to the corresponding binary inputs, and all output signals to the corresponding binary outputs of the terminal. The operation of each separate block is then checked by applying the rated DC voltage to the corresponding binary inputs and observing the logic statuses of the corresponding binary outputs. Configuration of the corresponding logic circuits takes place under:

Configuration
Binary Inputs
I/O module n

for the binary inputs and under:

Configuration
Binary Outputs
I/O module n

for the binary outputs

The configuration logic blocks included in the operation of the different functions must be tested at the same time as their corresponding functions.

1.6 Appendix

1.6.1 Terminal diagrams

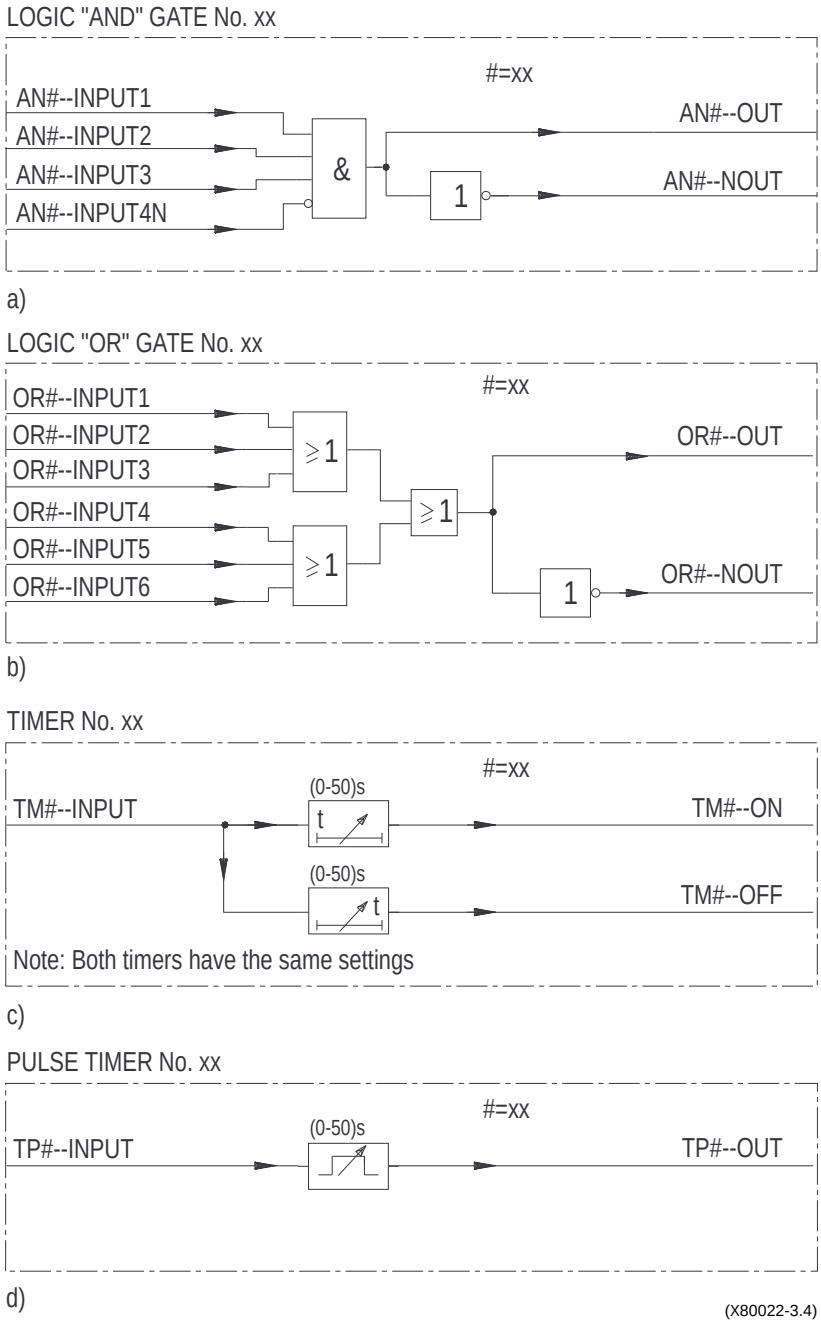

Fig. 3 Terminal diagrams of the CLC functions.

1.6.2 Signal list

CONNECTIONS:	TO:	SETTING:	DESCRIPTION:
			Logic OR gates
OR-gate No.#			**OR-gate No. #, where # goes from 1 to 20**
OR#--INPUT1	BI		Binary input No. 1 to the configuration logic gates No. #
OR#--INPUT2	BI		Binary input No. 2 to the configuration logic gates No. #
OR#--INPUT3	BI		Binary input No. 3 to the configuration logic gates No. #
OR#--INPUT4	BI		Binary input No. 4 to the configuration logic gates No. #
OR#--INPUT5	BI		Binary input No. 5 to the configuration logic gates No. #
OR#--INPUT6	BI		Binary input No. 6 to the configuration logic gates No. #
			Logic AND gates
AND-gate No. #			**AND-gate No. #, where # goes from 1 to 10**
AN#--INPUT1	BI		Binary input No. 1 to the configuration logic gates No.#
AN#--INPUT2	BI		Binary input No. 2 to the configuration logic gates No.#
AN#--INPUT3	BI		Binary input No. 3 to the configuration logic gates No.#
AN#--INPUT4N	BI		Binary input No. 4 to the configuration logic gates No.# (inverted)
			Logic timers
TM#--INPUT	BI		Binary input to the timers delayed on pick-up and drop-out No.#, where goes # from 1 to 10
TP#--INPUT	BI		Binary input to the pulse timer No.#, where goes # from 1 to 10

PRODUCTION	TO:	SETTING:	DESCRIPTION:
			Logic OR gates
OR-gate No. #			**OR-gate No.#, where # goes from 1 to 20**
OR#--OUT	BO		Binary output from the OR logic gates No.#
OR#--NOUT	BO		Inverted binary output from the OR logic gates No.#
			Logic AND gates
AND-gate No.#			**AND-gate No. #, where # goes from 1 to 10**
AN#--OUT	BO		Binary output from the AND logic gates No.#
AN#--NOUT	BO		Inverted binary output from the AND logic gates No.#
			Timer delayed on pick-up and drop-out
TM#--ON	BO		Binary output from the timer delayed on pick-up No.#, where goes # from 1 to 10
TM#--OFF	BO		Binary output from the timer delayed on drop-out No.#, where goes # from 1 to 10
			Pulse timer
TP#--OUT	BO		Binary output from the pulse timer No.#, where goes # from 1 to 10

1.6.3 Setting table

PARAMETER:	SETTING RANGE:	SETTING	DESCRIPTION:
		ACTUAL	
			Timers TM delayed on pick-up and drop-out
t1	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 1
t2	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 2
t3	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 3
t4	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 4
t5	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 5
t6	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 6
t7	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 7
t8	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 8
t9	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 9
t10	(0,00 - 50,00) s		Time delay set on the configuration logic timers delayed on pick-up and drop-out No. 10
			Pulse timers TP
t1	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 1
t2	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 2
t3	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 3
t4	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 4
t5	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 5
t6	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 6
t7	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 7
t8	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 8
t9	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 9
t10	(0,00 - 50,00) s		Time delay set on the configuration logic pulse timer No. 10