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Abstract— Traditionally, the major driver in IGBT and diode development is to minimize the static and dynamic losses. A significant reduction of the n-base thickness would yield this, however it can also jeopardize the switching characteristic leading to high overshoot voltages during diode reverse recovery. In this paper, we present an improved Field-Charge Extraction (FCE) concept that is achieving a soft reverse recovery behavior inherently. The new design allows for a 10% reduction of the thickness of the diode's n-base, while still maintaining the blocking capability and the softness of the conventional diode. Therefore, the technology curve and the ruggedness are improved significantly.

I. INTRODUCTION

The request for lower losses and higher power densities for a minimized device footprint has been the traditional trend in power semiconductor developments. High power applications demand fast switching devices to benefit in overall losses. Unfortunately, a high commutation rate of the IGBT in combination with a short diode tail triggers oscillations of the antiparallel free-wheeling diode, which are more pronounced at high stray inductances and low currents. In the past such reverse recovery behavior has been optimized by carefully designing the silicon specification, the buffer and by applying life-time and/or emitter controlled principals [1]–[3]. It was shown previously that the introduction of backside p+ structures can improve the softness of the switching characteristic and can also be utilized to improve on the technology curve in the lower voltage range [4], [5]. In contrast to the CIBH concept [6], for the FCE concept, the p+ areas are not free-floating but connected to the cathode contact [7].

Figure 1a shows the schematic cross-sections of the active area of the conventional diode. A high p+ doping forms the anode contact and a deep diffused p- buffer anode is incorporated to support the electric field during blocking [8]. An n-buffer layer is introduced at the cathode and the high n+ doping concentration forms the contact. Deep levels generated by heavy ion-irradiation tailor the static and dynamic properties. In contrast to this uniform backside contact the cathode of the FCE-diode consists of a two-dimensional lattice of p+ islands embedded in the high n+ cathode doping (figure 1b, c). Obviously, the larger the p+ area the more pronounced is the impact on the forward voltage drop. Therefore the p+ area must be restricted to a small fraction of the total chip-area. In our case this is less than 10% and does therefore hardly affect the forward voltage drop of the diode. The direct comparison yielded less than 50mV at nominal current. However, the p+ areas are the key enablers for very soft reverse recovery as it is shown in the next section.

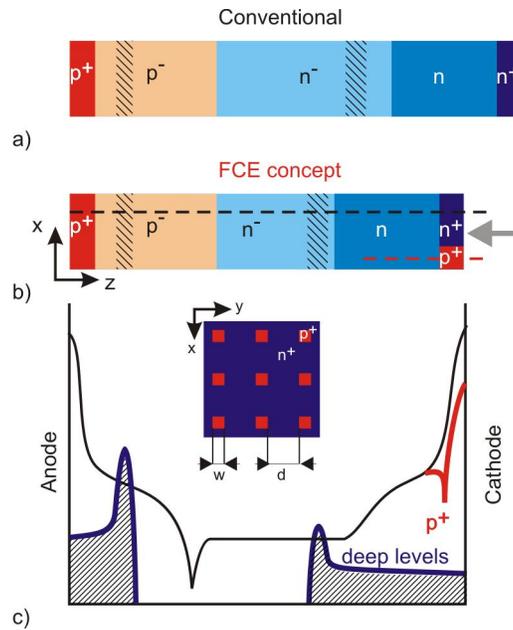


Figure 1. Schematic drawing of the diode structure. a) Cross-section of the active area region of the conventional diode. b) Cross-section of the FCE concept with additional p+ areas incorporated at the cathode side. c) Schematic doping profiles with deep levels. The inset shows the backside of the diode with the isolated p+ areas in the n+ cathode contact. The width w and the distance d are critical for the performance.

II. SIMULATIONS

TCAD device simulations were performed to study the reverse recovery behavior of the conventional and the FCE diode (figure 2a). While the reference diode shows a clear snap-off during the tail phase for the simulated conditions, the FCE diode effectively prevents this mode of operation. The reason for the snap-off during turn-off is discussed with the help of the extracted electron density for three time-steps (figure 2b). During reverse recovery the backside is positively charged and electrons are extracted at the backside while holes are consumed at the anode. At time t_1 the device is still fully flooded with plasma. This is extracted at both contacts, until at time t_2 (maximum reverse recovery current) the space-charge-region (SCR) at the anode side starts to evolve and also at the cathode-side a small SCR is formed. At time t_3 before the snap-off the remaining neutral plasma is located in between the two SCRs. The sudden extraction of the charge carriers will generate high over-voltages due to the large current change.

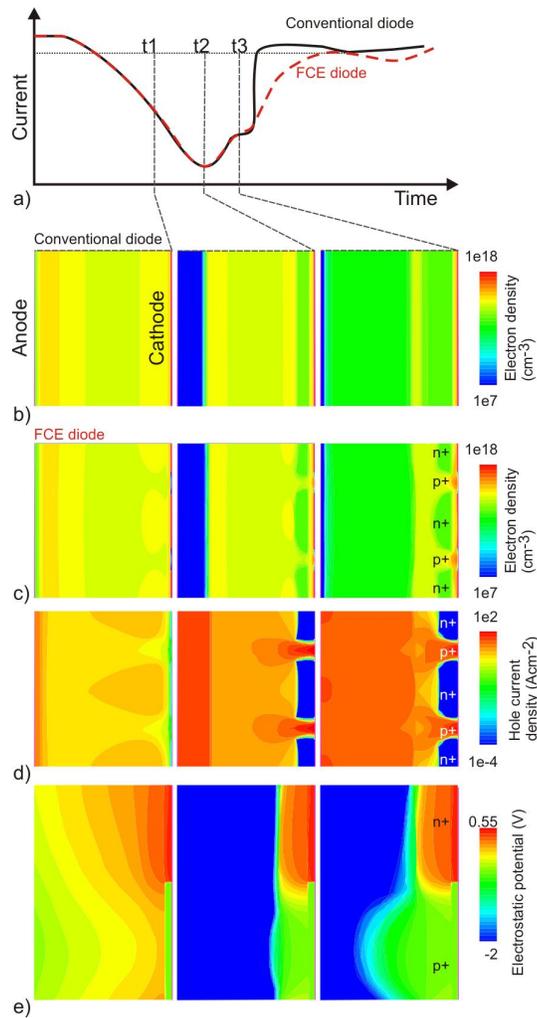


Figure 2. a) Simulated current waveform for a conventional and the FCE diode. The marked three time-steps (t_1 , t_2 , t_3) are linked to the two-dimensional plots of the simulated parameters. b) Electron density for the conventional diode. c) Electron density (FCE). d) Hole current density (FCE). e) Close-up of the electrostatic potential at the cathode sided p+/n+ junction.

The electron density of the FCE-diode shows the expected periodicity (cathode side; Figure 2c), due to the backside structuring. At the maximum reverse recovery current (t_2) the SCR at the anode side is formed as usual. However, in contrast to the conventional diode the electrons accumulate in front of the cathode-side p+ area for the FCE case and a neutral plasma region is formed there. The hole-current density indicates a high current being injected from the p+ regions (figure 2d). Therefore, the continuously supplied charge carriers prevent the snap-off effectively. The close up of the electrostatic potential at the cathode shows the forward biasing phenomena of the pn-junction (figure 2e). During switching the electrons accumulate in front of the p+ region and start to flow laterally towards the n+ region. This results in a forward biasing of the cathode-sided pn- junction.

In a simplified one-dimensional equation the condition for hole-injection can be written as:

$$V_{bi}(T) \leq j(T) \frac{d_{eff}}{eN_D\mu_n(T)} \tag{1}$$

Where T is the temperature, j is the current density during recovery, d_{eff} is the effective distance the electrons need to travel laterally in front of the p+, e is the electronic charge, N_D is the doping concentration of the buffer layer and μ_n is the temperature dependent mobility. As long as the induced voltage drop at the junction is exceeding the temperature dependent built-in voltage V_{bi} of about 0.7V,

the p+ region will be injecting. In addition, the injection depends on the doping levels and the temperature. From this equation it can be concluded that the FCE effect would work best at high current densities (equivalent to the turn-off of high forward currents) and elevated temperatures resulting in reduced mobility. By design this can be supported through the extension of the lateral dimension of the p+ regions and a low n-buffer doping concentration, which is still preventing reach through of the electric field during blocking and ensuring a high safe-operating area. Unfortunately, the plasma evolving in front of the p+ areas deteriorates the injection, because effectively the distance the electrons need to travel laterally is reduced and therefore the induced voltage drop decreases. The main parameters influencing the effect are the doping concentration of the buffer and the electron mobility. The latter one changes within the desired temperature range from $T_j = -50^\circ\text{C}$ to 150°C almost by one order of magnitude and the buffer-doping concentration must be sensitively tuned during fabrication. For low temperatures the forward biasing effect works less efficient, because the built-in voltage increases, the charge is reduced and the mobility is increased.

III. EXPERIMENTAL

In this paper the conventional diode is compared to two FCE diodes later on referred to as FCE1 and FCE2. The FCE1 diode is utilizing the same silicon specification like the conventional diode and the FCE2 diode is thinned by 10%. To maintain the blocking capability the resistivity has been adjusted accordingly (see table 1). The diodes were assembled in an industrial package consisting of 12x diodes and 24x IGBTs. The nominal current of such a package is 1.5kA and the rated voltage is 3.3kV. The inset in figure 3a is showing such a module. The modules were tested under harsh softness condition at a high voltage of 2.5kV and at a low current of 50A.

TABLE I. TABLE OF INVESTIGATED DIODES

Parameter	Diode type		
	Conventional	FCE1	FCE2
Thickness a.u.	1	1	0.9
Resistivity a.u.	1	1	1.6
Blocking	>3.8kV	>3.8kV	>3.8kV

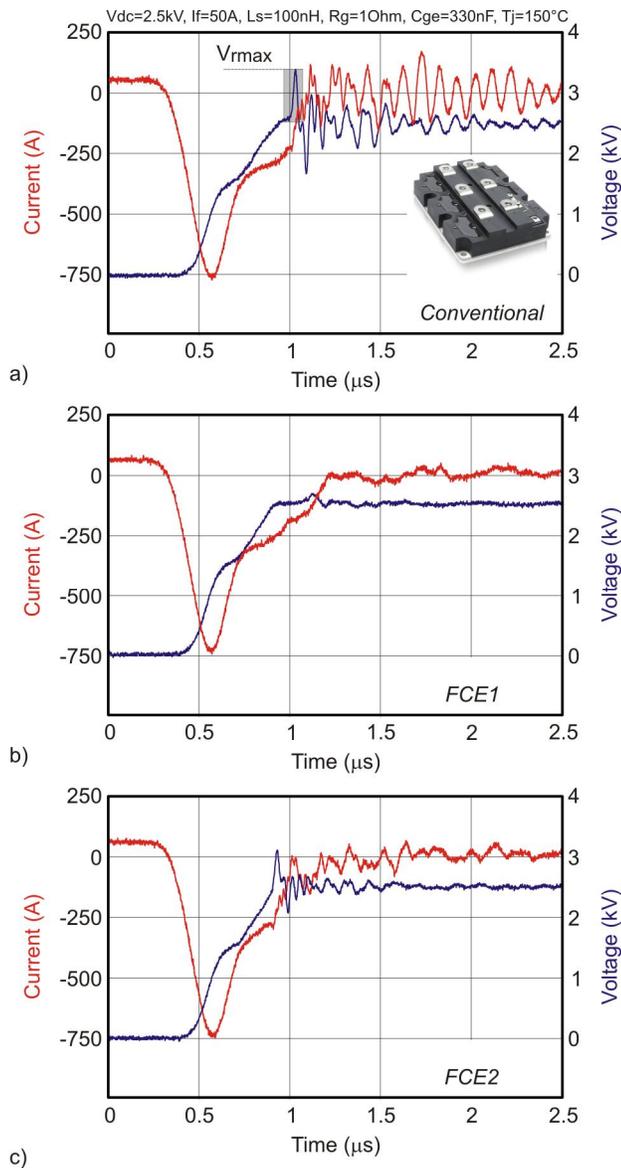


Figure 3. Diode turn-off waveforms measured on modul-level at $T_j=150^\circ\text{C}$. a) Conventional diode module. The resulting overvoltage is highlighted by a grey bar. b) FCE1. c) FCE2.

The turn-off waveform in figure 3a shows a snap-off at the end of the tail-phase resulting in an overvoltage of almost 3.3kV. The FCE1 diode in contrast shows a soft reverse recovery for the same conditions. All oscillations are prevented by the controlled injection of holes from the p+ area. Although, the thinned FCE2 diode does not outperform the FCE1 diode, it still shows a soft turn-off behavior. It is important to note that a conventional diode without the p+ areas at the cathode using the same silicon like FCE2 would generate an overvoltage exceeding 4kV. At high temperatures the FCE-type diode clearly demonstrates its advantages.

A widely used parameter to assess softness is the maximum reverse voltage during recovery V_{rmax} . Figure 4a shows the summary of the softness measurements of the three diodes under consideration. At elevated temperatures of $T_j=150^\circ\text{C}$ the worst case condition for the conventional diode is at the previously shown switching current of 50A. For increased forward currents the measured overvoltage is reduced. Overall, the FCE1 diode shows the best softness behavior over the full current range, restricting the overvoltage below 2.7kV, while the FCE2 diode is generating higher overshoot voltages up to 3.1kV. As discussed previously the FCE-effect is decreased when approaching low temperatures of $T_j=-40^\circ\text{C}$. According to equation (1) this would result in a lower forward biasing. The V_{rmax} analysis is shown in figure 4b. As expected the FCE1 diode shows the best performance, while the FCE2 diode is in particular for higher current

densities generating high reverse voltages of approximately 3.4kV. Nevertheless, the highest overvoltage at $T_j=-40^{\circ}\text{C}$ is generated by the conventional diode at low current.

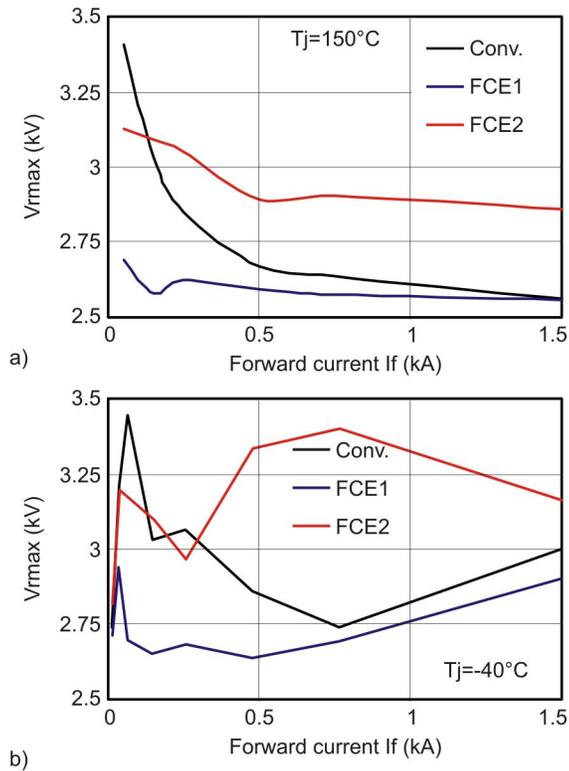


Figure 4. Maximum reverse voltage during diode turn-off for the three diode versions at $T_j=150^{\circ}\text{C}$ (a) and $T_j=-40^{\circ}\text{C}$ (b).

The safe operating area (SOA) of the FCE2 diode was investigated and compared to the conventional diode (figure 5). The measurements were performed on substrate level (2x diodes and 4x IGBTs) and the switching conditions were scaled up to module conditions. At a quarter of the nominal current the conventional diode shows a snap-off behavior resulting in a high overvoltage peak exceeding 5kV. For the same commutation rate of approximately $1.8\text{kA}/\mu\text{s}$ (equivalent to $10.8\text{kA}/\mu\text{s}$ on module-level) the FCE2 diode shows a soft reverse recovery. In this case, the newly achieved softness-level is even improving the SOA-capability, because such a high peak voltage can destroy the diode rated at 3.3kV. The maximum reverse recovery current is increased for the FCE2 diode compared to the conventional one. This is a result of the modified high-resistivity silicon, since it was not observed for the FCE1 diode.

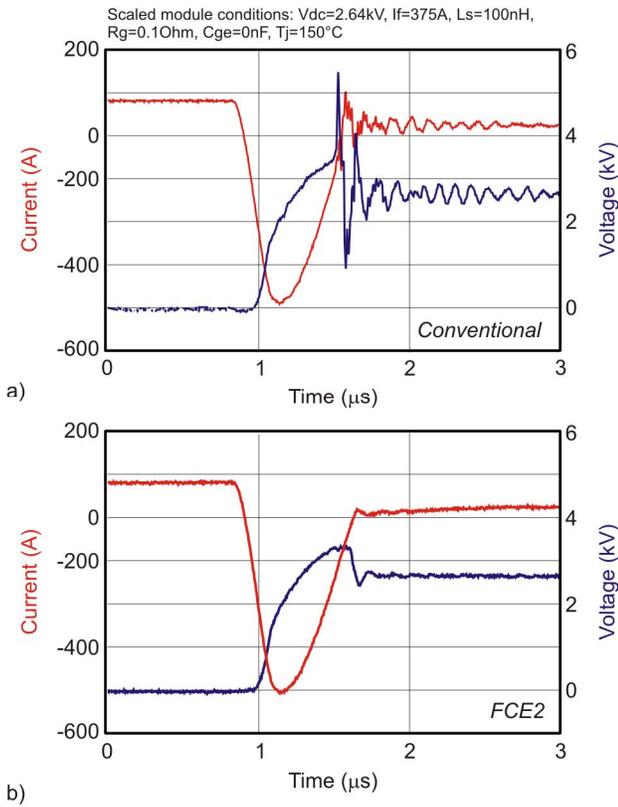


Figure 5. Measured waveforms under SOA-conditions. a) Conventional diode. b) FCE2. The conditions were scaled from substrate to module-level.

IV. CONCLUSION

It has been shown that the injection of holes enables soft reverse recovery behavior even though harsh switching conditions have been combined with an aggressive silicon specification design. Therefore, for the FCE concept, applying the backside p+ areas is relaxing the tight restrictions to the silicon design given by the softness requirement. This flexibility can be utilized for either designing ultra-soft diodes and/or low loss thin n-base diodes with an advantageous technology curve (figure 6). A 10% thickness reduction demonstrated in this paper is lowering the on-state voltage drop and switching losses significantly.

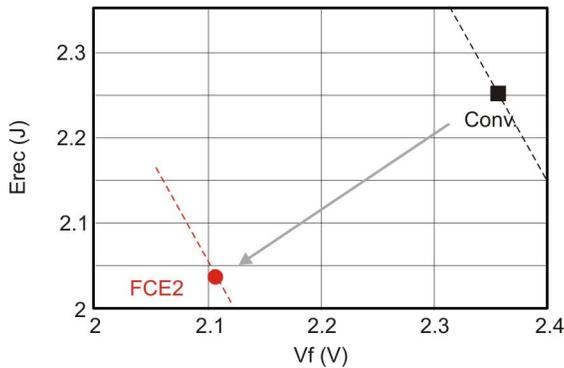


Figure 6. Comparison of the FCE1 diode and the conventional diode for the switching-losses versus forward voltage drop trade-off. (Conditions: $V=1.8kV$, $I=1.5kA$, $L_s=100nH$, $C_{ge}=330nF$, $R_g=1\Omega$, $T_j=150^\circ C$).

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