DPU2000/1500R/2000R

MODBUS / MODBUS PLUS
MODBUS TCP/IP

AUTOMATION TECHNICAL GUIDE

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Section 1 - Introduction

With the introduction of a microprocessor based protective relay, today's relay protection engineer must be familiar with topics outside of traditional relaying schemes. It is intended that the production of this manual will enable the relay engineer to understand the principles of a microprocessor-based relay's inclusion in a substation automation project.

Substation automation is heavily dependent upon integration of the appropriate components to allow reporting of metering and event data. The foundation of a successful automation solution is thorough engineering of a communication system. The Distribution Protection Unit (DPU) is the culmination of intensive design efforts and relaying experience, which combine protective relaying and communication capabilities at an economical price. Through the evolution of protective relays, it was decided that a special manual needed to serve today's power automation specialist.

This guide is intended to give the reader an in-depth explanation of the communication interfaces available with the Distribution Protection Unit. Successful integration of microprocessor based relays like the DPU depends on not just understanding the bits and bytes of a particular protocol. It is the inherent understanding and application of such esoteric topics as physical interfaces, real time control, manufacturer independent device integration, throughput vs. speed of communication, … which influences the success of an automation project.

In many cases the individual performing the SCADA integration is not a relay protection engineer. This manual departs from the standard type of relay manual in that each data type is explained and each bit, byte and word meaning is explained. Several application examples are given within each section. A description of each protocol command is illustrated for the benefit of the user. Appendices are included detailing application notes, which augment the text. An explanation of the product's physical interfaces and the connectivity required is explored in depth. Explanations of register's uses to increase overall throughput are also explored. Throughput is always an issue when the system is commissioned. Understanding ways to improve the system data update is explained.

Several steps are required to permit successful communication between devices:

1. Identification of the hardware components (Section 2)
2. Correct physical connection between devices (Section 3).
3. Correct device configuration of port protocol and operation parameters (Section 4).
4. Generation and interpretation of the protocol command strings (Section 6).

The following sections shall explore the following procedures in depth when establishing a communication automation system, utilizing the DPU2000, DPU1500R and DPU2000R. An additional Section (Section 7) illustrates troubleshooting and commissioning of the Modbus/Modbus Plus Networks.

The DPU, DPU2000, DPU1500R and DPU2000R all have networking capabilities. The DPU has the most limited network capabilities whereas the DPU2000R has the most expansive of connectivity options and array of protocols. Figure 1-1 shows the general look of the units as viewed from the front.

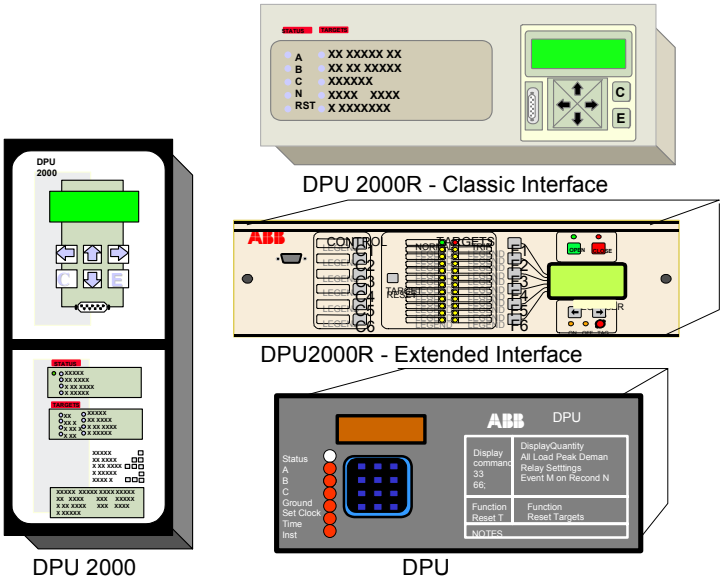


Figure 1-1. Distribution Protection Unit Product Family

The products differentiate themselves as listed in Table 1-1. Table 1-1 lists the available protocols within the relays. Standard Ten Byte is an ABB protocol which is within each of the protective relays. Standard Ten Byte is an asynchronous byte oriented protocol. The programming software WIN ECP [Windows External Communication Program]) allows configuration of the relay through a port on the units. Standard Ten Byte is available through an RS 232 or RS 485 port on the DPU.

INCOM is an ABB protocol, which is a derivative of Standard Ten Byte. It is a modulated synchronous bit stream using the same commands as in the Standard Ten Byte protocol. INCOM is available on each of the protective relays as indicated within Table 1-1. Its physical interface is proprietary in that the DPU node expects a modulated signal.

Serial **Modbus** is an industrial de-facto standard protocol, which has been widely embraced by the utility industry. Modbus has two emulation's, RTU, which is a synchronous protocol and ASCII which is an asynchronous protocol. Modbus uses only one command set, but two emulation's. Modbus strengths are that it uses a standard RS 232 or RS 485 interface to interconnect nodes on a network.

TCP/IP Modbus is an evolution of Serial Modbus in that it uses Ethernet as the mechanism to transfer the Modbus Serial packets across an Ethernet LAN. It is gaining in popularity in that several protocols and network transmissions may peaceably coexist on a single network cable. Network Modbus (or TCP/IP Modbus) has its own protocol conventions and is not merely initiation of an Ethernet TELNET session over the Local Area Network (LAN).

Modbus Plus is a hybrid protocol refinement of Modbus. Modbus Plus has a proprietary physical interface which is available to device manufacturers through a connectivity program with Groupe Schneider. The interface offers greater speed and communication features than Modbus.

DNP 3.0 is a protocol, which has its roots deep in the utility industry. It is an asynchronous protocol that allows connectivity through a standard RS 232 or RS 485 port. It includes such defined capabilities as file transfer, and timestamping as part of the protocol, which makes it desirable for a utility implementation. UCA is a newly emerging protocol based upon an object oriented device structure.

UCA stands for Utility Communication Architecture. Instead of the traditional mindset of data access using address, index terminology, data is retrieved or modified by using predefined "names" to access or modify data. The hardware topology employed for this new protocol is Ethernet (just as that for Network Modbus), however the messaging structure and data access definitions are markedly different. Later sections shall explore the UCA construction from a hardware topology and a software access/control standpoint.

Table 1-1. Protocol Capabilities Listed by Product Type

Product	Protocol	Notes
DPU	TEXT ASCII COMMAND SCRIPT	Not Addressable RS 232 Only
DPU 2000	Standard Ten Byte	Addressable Front Com, Com 1 and Aux Com
	INCOM	2 Wire (AND SHIELD) Current Injection Physical Interface
	Modbus	RS 232 or RS 485
	DNP 3.0	RS 232 or RS 485
DPU 2000R	Standard Ten Byte	RS 232 or RS 485
	INCOM	2 Wire (AND SHIELD) Current Injection Physical Interface
	Serial Modbus	RS 232 or RS 485
	Modbus Plus	Proprietary Current Injection Physical Interface
	Network Modbus	Ethernet Interface Copper or Fiber Optic
	DNP 3.0	RS 232 or RS 485
	UCA	Ethernet Interface Copper or Fiber Optic

Within this document, only **Modbus, Modbus Plus TCP/IP Modbus** protocol shall be covered in depth. Standard 10 Byte, UCA, INCOM and DNP 3.0 shall be explained superficially. If one would need to reference the specific details of Standard Ten Byte or INCOM protocols, please reference the engineering specifications concerning these topics in Appendix A of this document.

Section 2 - Communication Card Identification and Physical Port Characteristics

The communication connector at the front of the unit (near the target LED's) communicates to the ECP or WinECP configuration program. This communication port is referred to as COM 0 and is common to both the DPU2000, DPU1500R and DPU2000R.The protocol emulated through this front port is an addressable emulation of Standard 10 Byte Protocol. With the addition of a communication card option, the unit emulates the protocols described in Table 1-1. The inclusion of optional communication boards enables the rear ports (as shown in Figure 2-2) of their respective units.

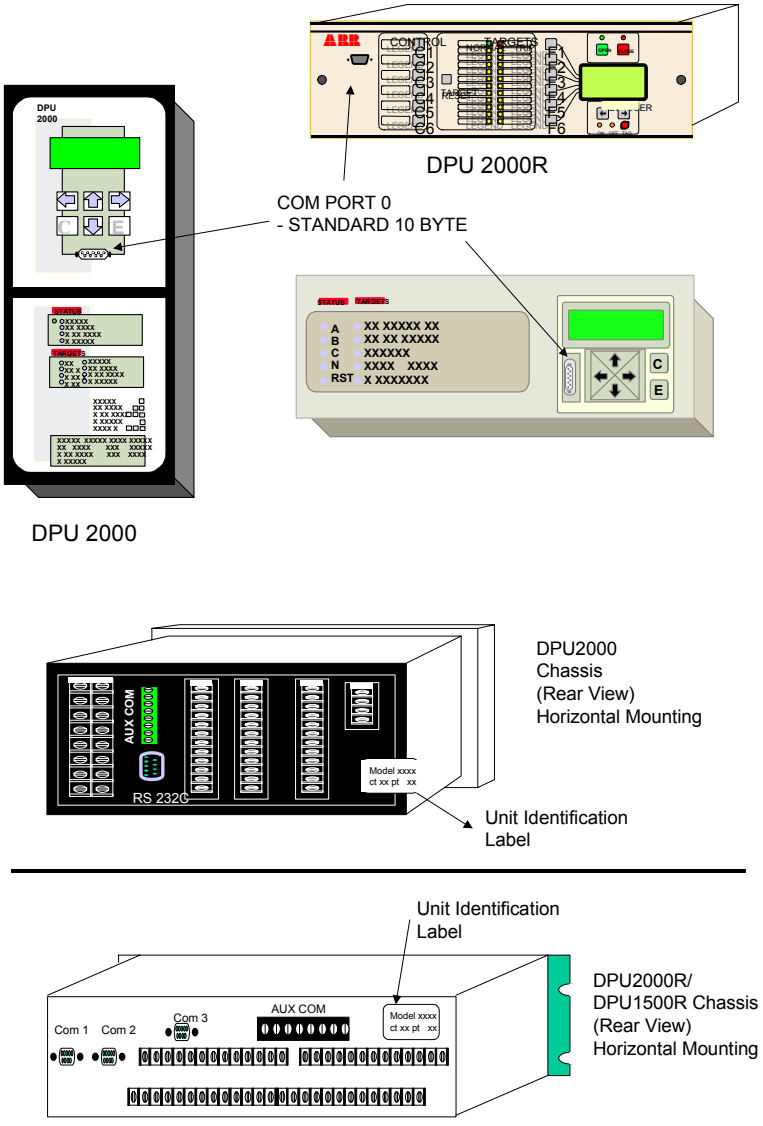
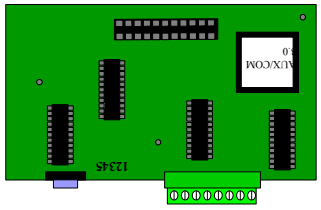


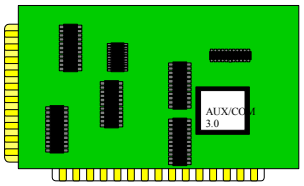
Figure 2-1. Physical Optional Communication Card Port Locations

The DPU2000 and DPU2000R differ in physical appearance. The communication cards inserted within the unit also differ in form, fit and construction. A typical DPU2000 and DPU2000R's communication card is illustrated in Figure 2-3 of this document. As shown, the DPU2000R has two physical interface connectors built onto the card.

The form factor of these connectors are industry common DB 9 and “PHOENIX 10 POSITION” connectors. The “PHOENIX 10 POSITION” connector has a capacity to land two 18 wire gauge conductors at each position. The DPU2000 has the communication port connectors fixed as part of the chassis. The physical card slot for housing the communication card is marked on the chassis as “COM”. The communication card mates with internal connectors allowing electrical and physical connections for the communication card and chassis mounted physical connectors.



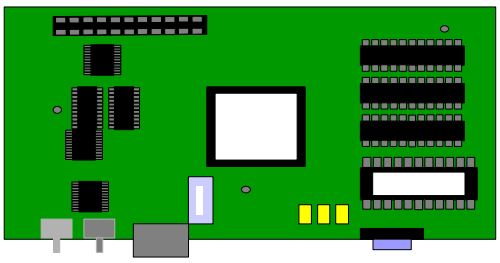
DPU1500R/DPU2000R COMMUNICATION CARD (TYPICAL)



DPU2000 COMMUNICATION CARD (TYPICAL)

Figure 2-3. DPU2000 and DPU1500R/DPU2000R Communication Cards

The ethernet cbased protocol hardware cards my only be addedto the DPU 2000R based platforms. As per the selections in Tables 2-3 and 2-5, the ethernet cards may not be inserted in aDPU 1500R or a DPU 2000. The form factor of the card is illustrated in figure 2-3a. Note the card does not have a Phoenix connector to connect RS485 connections nor does it have IRIG B connections



DPU 2000 R COMMUNICATION CARD (TYPICAL)

Figure 2-3a. DPU 2000R Communication Cards

The DPU2000 Communication card is housed within a removable chassis. The communication card mates with edge card connectors located at the front and bottom of the removable chassis. Figure 2-3 illustrates the mounting location of the DPU2000 Communication card. Figure 2-4 illustrates the communication port locations of the DPU2000, which may be configured to communicate with the protocols described in Section 2 of this document.

The DPU2000R mates with the unit’s main board to enable/disable Com Ports 1, 2, 3, and AUX COM. The communication cards physical interfaces protrude through the sheet metal back plate housing of the unit and allow for access to the physical connection ports. Figure 2-5 illustrates the location of the communication board assembly.

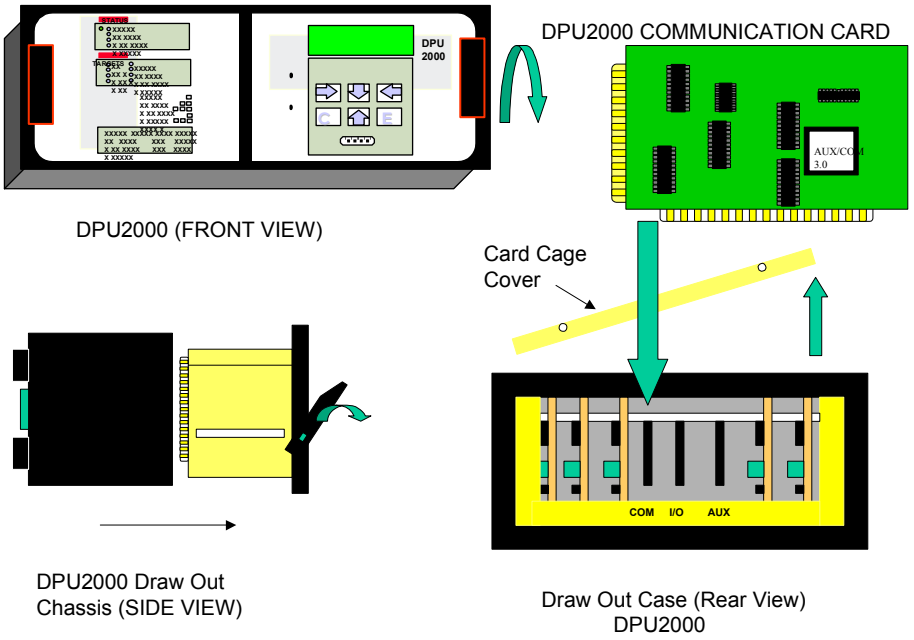


Figure 2-4. Physical Communication Card Location for the DPU2000

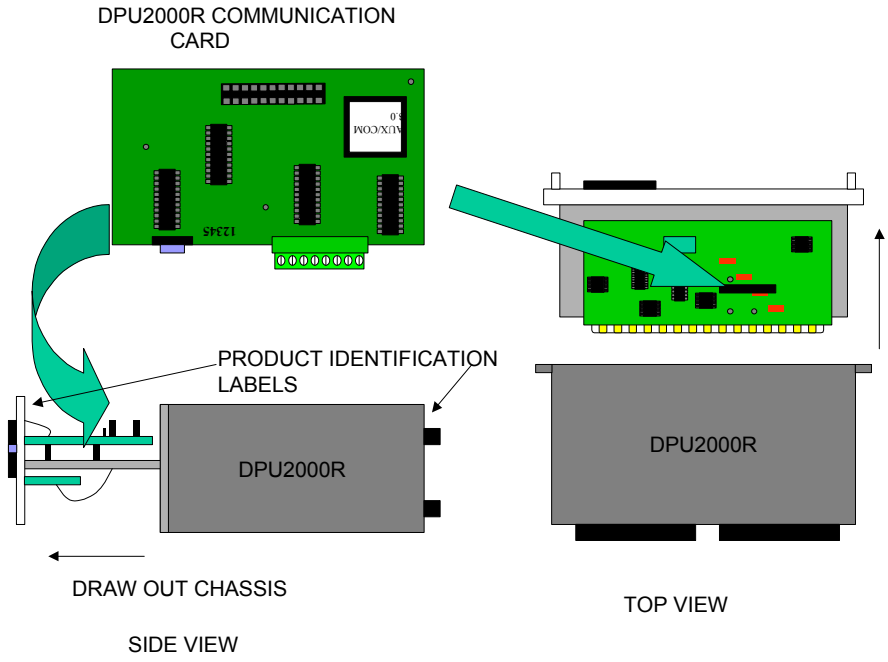


Figure 2-5. Physical Communication Card Location for the DPU1500R/DPU2000R

CAUTION: REMOVAL OF THE DRAW OUT CHASSIS COMPONENTS WILL DE-ENERGIZE THE ELECTRONICS OF THE UNIT THEREBY PREVENTING SYSTEM PROTECTION. EXTREME CARE MUST BE TAKEN WHEN REMOVING THE ELECTRONIC DRAWER FROM THE CHASSIS SINCE ALL PROTECTIVE RELAY FUNCTIONALITY WILL BE TERMINATED.

CAUTION: IF THE UNIT IS UNDER POWER THE CT's ARE SHORTED INTERNALLY THROUGH THE CHASSIS INERTNAL CONNECTORS. HOWEVER, EXTREME CAUTION MUST BE EXERCISED WHEN REMOVING THE DRAW OUT CASE FROM AN ENERGIZED UNIT. ABB TAKES NO RESPONSIBILITY FOR ACTIONS RESULTING FROM AVOIDANCE OF THIS WARNING AND CAUTION NOTICE.

CAUTION: Sensitive electronic components are contained within the DPU2000 and DPU2000R/DPU1500R units. The individual removing the component boards from the fixed chassis must be grounded to the same potential as the unit. IF THE OPERATOR AND THE CASE ARE NOT CONNECTED TO THE SAME GROUND POTENTIAL, STATIC ELECTRICITY MAY BE CONDUCTED FROM THE OPERATOR TO THE INTERNAL COMPONENTS RESULTING IN DAMAGE TO THE UNIT.

Communication Card Part Number Options

The DPU2000 and DPU2000R/DPU1500R may be ordered with a variety of communication options as listed in Table 2-1. The communication option card installed in the unit is identified by the part number located on the unit or identified through the ECP, WinECP or Front Panel (LCD) interfaces.
The protocols available are:

- ❑STANDARD TEN BYTE® – This is an ABB specific ASCII encoded (asynchronous) 10 byte communication protocol. It allows attainment of all relay parameters. It is the base unit protocol in which configuration programs such as ECP, and WinECP communicate to the DPU2000 or DPU2000R. It is the protocol standard for the COM 0 communication port of the DPU2000 and DPU2000R. Standard 10 Byte does not utilize a proprietary hardware physical interface. Appendix B includes the DPU2000 and DPU2000R/DPU1500R Standard 10 Byte Protocol Document.

- ❑INCOM® – This is an ABB Specific bit oriented (synchronous) protocol. INCOM uses the same commands as Standard Ten Byte, but its inherent bandwidth utilization is far greater than Standard Ten Byte is in that no data encoding is required. INCOM only defined two baud rates 9600 and 1200. INCOM is a proprietary interface in that its physical presentation to the communication medium is dependent upon the baud rate selected. 1200 Baud uses current injection baseband signal presentation, whereas 9600-Baud implements a phase shift frequency in its representation of digital 1 and 0 values. Appendix B includes the DPU2000 and DPU2000R/DPU1500R Standard Ten Byte Protocol document which describes INCOM in further detail.
- ❑DNP 3.0® – This is a Utility industry standard protocol allowing communication between a host and slave devices. DNP 3.0 is a byte oriented (asynchronous) protocol which is physical interface device independent. The protocol allows for time synchronization, and unsolicited event reporting. It is a very popular protocol in utility installations. The discussion of DNP 3.0 protocol is included in this document.
- ❑SPACOM® – This is an ABB Specific byte oriented (asynchronous) protocol common in Europe. It is a Master-Slave protocol which is implemented on a variety of physical interfaces. SPACOM protocol is not covered within this document.
- ❑SERIAL MODBUS® – This is an Industrial standard. The protocol allows a single master device to communicate with several slave devices. It has gained wide acceptance in that a great majority of utility devices incorporate Modbus protocol. Modbus Protocol is physical interface independent. Modbus Protocol has two emulation's RTU (a synchronous bit oriented emulation) and ASCII (an asynchronous byte oriented emulation). The DPU2000 and DPU2000R may be configured for both emulations. The discussion of Modbus protocol is included in this document. Please reference the DPU2000 and DPU2000R Modbus/Modbus Plus Automation Technical Guide TG 7.11.1.7-51 for a discussion of this protocol.
- ❑MODBUS PLUS® – This protocol is also and industrial standard. Modbus Plus allows up to 64 devices to communicate among each using token passing techniques. The Modbus Plus protocol is fast (1 megabaud) and uses several advanced techniques to maximize bandwidth. The physical interface to Modbus Plus is proprietary and regulated by Groupe Schneider. Modbus Plus is the incorporation of Modbus commands on a HDLC®- like protocol using a current injection interface. The discussion of Modbus Plus protocol is not included in this document. Please reference the DPU2000 and DPU2000R Modbus/Modbus Plus Automation Technical Guide TG 7.11.1.7-51 for a discussion of this protocol.
- ❑PG&E® – This protocol is a bit oriented asynchronous protocol allowing a Master Device to communicate with several slave devices. PG&E protocol is a Utility protocol. The protocol is not described in this document

- TCP/IP MODBUS® – This protocol is derived from the Modbus protocol and is an extension of the protocol on an Ethernet MMS Transport Layer. It is also gaining wide acceptance since it is used frequently with Programmable Logic controllers found commonly in Industrial and Utility applications.
- UCA – This evolving protocol is based upon an Ethernet standard in which each of the elements within the protocol are object oriented. This next step in network protocol architecture allows the device to be self reporting with regard to the protocol objects defined in the device.

The device configuration for the DPU2000 is illustrated in Tables 2-1 and 2-2 illustrating the configuration options. The generic part number for the DPU2000 is 4 8 7 M R X D Z – C S S S Q. Deciphering the part numbers: found on the labels of the unit or obtained through ECP or the Front Panel LCD Interface, allows easy identification of the communication options found on the unit.

Table 2-1. DPU2000 Communication Options

If Part Number Position "Z" is	**The DPU2000 has Installed Option** **For unit** 4 8 7 M R X D **Z** – C S S S Q (COMMUNICATION PHYSICAL INTERFACE OPTION)
1	RS232 (COM 3) Isolated Port Enabled
2	RS485 (AUX COM PORT) and RS232 (COM 3) Ports Enabled
3	INCOM (AUX COM PORT) Enabled
4	RS485 (AUX COM PORT) Ports Enabled
If Part Number Position "Q" is	**The DPU2000 has an Installed Option** **For unit** 4 8 7 M R X D C – Z S S S **Q** (COMMUNICATION PHYSICAL INTERFACE OPTION)
0	STANDARD TEN BYTE
1	DNP 3.0
2	SPACOM
4	MODBUS

Table 2-2. DPU2000 Communication Card Matrix for Unit 4 8 7 M R X D Z – C S S S Q

"Z" Digit	"Q" Digit	COM 3	AUX COM RS485	INCOM	IRIG B
1	0	Standard 10 Byte **RS232**			
2	0	Standard 10 Byte **RS232**	Standard 10 Byte		Available
2	1	Standard 10 Byte or DNP 3.0 **RS232**	Standard 10 Byte or DNP 3.0		
2	2	Standard 10 Byte **RS232**	SPACOM		
2	4	Standard 10 Byte or Modbus **RS232**	Standard 10 Byte or Modbus		Available
3	0			Available	Available
4	0		Standard 10 Byte	Available	Available
4	1		DNP 3.0	Available	Available
4	2		SPACOM		
4	4		Modbus	Available	Available
5	0		Standard 10 Byte		

The device configuration for the DPU2000R is illustrated in Tables 2-3 and 2-4 illustrating the configuration options. The generic part number for the DPU2000 is 4 8 7 X X X Y Z – X X X X Q. Deciphering the part numbers: found on the labels of the unit or obtained through ECP or the Front Panel LCD Interface, allows easy identification of the communication options found on the unit.

Table 2-3. DPU2000R Communication Options

IF PART NUMBER POSITION "Y" IS	**THE DPU 2000R HAS AN INSTALLED OPTION** **For unit** 587 X X X **Y** Z – X X X X Q (X = Don't Care) (FRONT PANEL INTERFACE OPTION)
0	Horizontal Unit Mounting – NO FRONT PANEL LCD INTERFACE
1	Horizontal Unit Mounting – FRONT PANEL LCD INTERFACE IS INCLUDED
2	Horizontal Enhanced OCI – FRONT PANEL LCD AND PUSHBUTTON INTERFACE INCLUDED
3	Horizontal Enhanced OCI – FRONT PANEL LCD AND PUSHBUTTON INTERFACE INCLUDED with Hot Line Tagging.
5	Vertical Unit Mounting – NO FRONT PANEL LCD INTERFACE
6	Vertical Unit Mounting – FRONT PANEL LCD INTERFACE IS INCLUDED
7	Vertical Enhanced OCI – FRONT PANEL LCD AND PUSHBUTTON INTERFACE INCLUDED
8	Vertical Enhanced OCI – FRONT PANEL LCD AND PUSHBUTTON INTERFACE INCLUDED with Hot Line Tagging.
IF PART NUMBER POSITION "Z" IS	**THE DPU 2000R HAS AN INSTALLED OPTION** **For unit** 587 X X X Y **Z** – X X X X Q (X = Don't Care) (COMMUNICATION PHYSICAL INTERFACE OPTION)
0	RS 232 (COM 1) Non-isolated Port is active on the unit
1	RS 232 (COM 2) Isolated Port Only is active on the unit (SEE NOTE)
2	RS 485 (AUX COM PORT) and RS 232 (COM 3) Ports on Option Card.
3	INCOM (AUX COM PORT)and RS 485 (AUX COM PORT) Ports on Option Card
4	INCOM (AUX COM PORT) and RS 485 (AUX COM PORT) Ports on Option Card
5	RS 485 (AUX COM PORT) Port On Option Card
6	Modbus Plus Port (COM 3) on the Option Card
7	Modbus Plus (COM 3) and RS 485 (AUX COM PORT) on the Option Card
8	RS 485 (COM 3) and RS 485 (AUX COM PORT) Ports on the Option Card
E	Ethernet Fiber Optic and Copper Option Card
	NOTE: * = If the option denoted in part number position "Y" is a 0 or 5, the COM 2 port is enabled, If the option denoted in part number position "Y" is a 1 or 5 the COM 2 Port is enabled.
IF PART NUMBER POSITION "Q" IS	**THE DPU 2000R HAS AN INSTALLED OPTION** **For unit** 587 X X X Y Z – X X X X **Q** (X = Don't Care) (COMMUNICATION PHYSICAL INTERFACE OPTION)
0	STANDARD TEN BYTE
1	DNP 3.0
2	SPACOM
3	PG&E
4	SERIAL MODBUS /NETWORK MODBUS PLUS/MODBUS PLUS (Depending on hardware interface selected in Position Z)
6	UCA

Table 2-4. DPU1500R Communication Options

If Part Number Position "Y" is	The DPU1500R has an Installed Option For unit 5 7 7 X X X **Y** Z – X X X X Q (X = Don't Care) (FRONT PANEL INTERFACE OPTION)
0	Horizontal Unit Mounting – No front panel LCD interface.
1	Horizontal Unit Mounting – Front panel LCD interface is included.
5	Vertical Unit Mounting – No front panel LCD interface.
6	Vertical Unit Mounting – Front panel LCD interface is included.
If Part Number Position "Z" is	**The DPU1500R has an Installed Option** **For unit** 5 7 7 X X X Y **Z** – X X X X Q (X = Don't Care) (COMMUNICATION PHYSICAL INTERFACE OPTION)
0	RS232 (COM 1) Non-Isolated Port is active on the unit.
1	RS232 (COM 2) Isolated Port Only is active on the unit. (SEE NOTE)
2	RS485 (AUX COM PORT) and RS232 (COM 3) Ports on Option Card.
3	INCOM (AUX COM PORT) and RS485 (AUX COM PORT) Ports on Option Card.
4	INCOM (AUX COM PORT) and RS485 (AUX COM PORT) Ports on Option Card.
5	RS485 (AUX COM PORT) Port On Option Card.
8	RS485 (COM 3) and RS485 (AUX COM PORT) Ports on the Option Card.
	NOTE: * = If the option denoted in part number position "Y" is a 0 or 5, the COM 2 port is enabled, if the option denoted in part number position "Y" is a 2 or 6 the COM 2 Port is disabled.
If Part Number Position "Q" is	**The DPU1500R has an Installed Option** **For unit** 5 7 7 X X X Y Z – X X X X **Q** (X = Don't Care) (COMMUNICATION PHYSICAL INTERFACE OPTION)
0	STANDARD TEN BYTE
1	DNP 3.0
4	Modbus (Depending on hardware interface selected in Position Z)

Table 2-5. DPU2000R Communication Card Matrix for Unit 5 8 7 X X X Y Z – X X X X Q

Q

"Z" Digit	"Q" Digit	COM 1 RS 232	COM 2 RS 232	COM 3	AUX COM	INCOM	Time Syncrhonization
0	0	Note 1	Standard 10 Byte				
1	0	Note 1		Standard 10 Byte **RS 232**			
2	0	Note 1		Standard 10 Byte **RS 232**	Standard 10 Byte **RS 485**		IRIG B
2	1	Note 1		Standard 10 Byte or DNP 3.0 **RS 232**	Standard 10 Byte or DNP 3.0 **RS 485**		
2	2	Note 1		Standard 10 Byte **RS 232**	SPACOM **RS 485**		
2	4	Note 1		Standard 10 Byte or Modbus **RS 232**	Standard 10 Byte or Modbus **RS 485**		IRIG B
3	0	Note 1				AVAILABLE	IRIG B
4	0	Note 1			Standard 10 Byte **RS 484**	AVAILABLE	IRIG B

"Z" Digit	"Q" Digit	COM 1 RS 232	COM 2 RS 232	COM 3	AUX COM	INCOM	Time Syncrhonization
4	1	Note 1			DNP 3.0 **RS 485**	AVAILABLE	IRIG B
4	2	Note 1			SPACOM **RS 485**		
4	4	Note 1			Modbus **RS 485**	AVAILABLE	IRIG B
5	0	Note 1			Standard 10 Byte **RS 485**		
6	4	Note 1	Standard 10 Byte	Modbus Plus			
7	4	Note 1		Modbus Plus	Standard 10 Byte **RS 485**		
8	0	Note 1		Standard 10 Byte **RS 485**	Standard 10 Byte **RS 485**		IRIG B
8	1	Note 1		Standard 10 Byte or DNP 3.0 **RS 485**	Standard 10 Byte or DNP 3.0 **RS 485**		
8	4	Note 1		Standard 10 Byte or Modbus **RS 485**	Standard 10 Byte or Modbus **RS 485**		IRIG B
E	4	Note 1			Network Modbus **Ethernet Copper or Ethernet Fiber Optic**		SNTP
E	6	Note 1			UCA or Network Modbus **Ethernet Copper or Ethernet Fiber Optic** Note 2		SNTP

NOTE 1: Enabled Standard 10 Byte if Digit "Y" is 0 or 5. Front Panel Interface not included Unavailable if Digit "Y" is 1, 2, 3, 4, 6, 7, or 8.
NOTE 2: Only one port Copper or Fiber Optic is enabled, both protocols co-exist on the same medium.

The visual identification of a DPU1500R/DPU2000R communication card is completed through visual inspection of the card component location and of the part number of the base printed circuit board as illustrated in Table 2-6.

Table 2-6. DPU1500R/DPU2000R Communication Card Matrix

"Z" Digit	Raw Circuit Board Part Number	Components To Look For
1	COMM 485 PCB 613709-005 REV0	Parts near black 9 pin 232 connector are populated
2	2000R AUX COM 613708-005 REV0	Parts in middle of board are not populated –2 DC/DC Converters (U1 & U8)
3	AUX COM 613708-005 REV0	Only parts in middle of board – no DC/DC Converters, has Transformer T2
4	AUX COM 613708-005 REV0	Parts near black 9 pin 232 connector are not populated – only 1 DC/DC Converter (U1)
5	COMM 485 PCB 613709-005 REV0	Parts near green connector are populated
6	MODBUS COMM PCB 613720-002 REV1	RS-485 option parts NOT populated (area inside dotted border)
7	MODBUS COMM PCB 613720-002 REV1	Fully populated
8	AUX & AUX 613755-002 REV0	Fully populated
E	TO BE DETERMINED	----------

Table 2-7. DPU1500R Communication Card Matrix for Unit 5 7 7 X X X Y Z – X X X X Q

"Z" Digit	"Q" Digit	COM 1 RS232	COM 2 RS232	COM 3	AUX COM RS485	INCOM	IRIG B
0	0	Note 1	Standard 10 Byte				
1	0	Note 1		Standard 10 Byte **RS232**			
2	0	Note 1		Standard 10 Byte **RS232**	Standard 10 Byte		Available
2	1	Note 1		Standard 10 Byte or DNP 3.0 **RS232**	Standard 10 Byte or DNP 3.0		
2	4	Note 1		Standard 10 Byte or Modbus **RS232**	Standard 10 Byte or Modbus		Available
3	0	Note 1				Available	Available
4	0	Note 1			Standard 10 Byte	Available	Available
4	1	Note 1			DNP 3.0	Available	Available
4	4	Note 1			Modbus	Available	Available
5	0	Note 1			Standard 10 Byte		
NOTE 1-Available if Digit "Y" is 0 or 5.Front Panel Interface not included. Unavailable if Digit "Y" is 1 or 6.							

Unit Communication Card Verification

There are several ways to identify the communication cards inserted in the DPU 2000R /1550R / 2000 units. Some of the methods require the unit to be powered up. Other methods require the unit to be taken out of service.

To identify the unit part number of the present DPU, the following steps may be executed to facilitate unit identification.

1. With the unit energized:
   - If the unit has a Front Panel LCD (Refer to Tables 2-1 through 2-3 inclusive for identification) Interface
     1. Depress the "E" Key.
     2. Depress the Arrow Down Key "↓" once to highlight the SETTINGS field. Depress the "E" Key.
     3. Depress the Arrow Down Key "↓" twice to highlight the UNIT INFORMATION field. Depress the "E" key.
     4. The Serial Number and Catalog Number shall be displayed. Fill in Table 2-1 with the required data.
   - If the Unit does not have a Front Panel LCD Interface (Refer to Tables 2-1 through 2-3 inclusive for identification) and the user has DOS ECP or if the user wishes not to use the unit's Front Panel LCD Interface.
     1. Start ECP.
     2. Select the appropriate communication parameters so that the personal computer attached to the DPU 2000 or DPU 2000(R) will communicate via the null modem cable connection. (See Figures 3-3 and 3-4, pages 16 and 17).
     3. Depress enter to allow attachment of the unit.
     4. The Serial Number and Catalog Number shall be displayed.

   - If the unit has an Enhanced Front Panel Interface (Refer to Tables 2-1 through 2-3 inclusive for identification) and the user wishes to obtain the information via the front panel interface, the following procedure must be followed to identify the board type present in the protective relay.
     1. From the metering screen displayed on the front panel interface, depress F1.
     2. From the displayed submenu, depress the selection associated with F2- MAIN MENU.
     3. The selection of submenus will be displayed, depress the key F6 associated with the submenu, PAGE DOWN.
     4. Depress the key F4 to display the submenu selection UNIT INFO.

5. This selection shall display the part number, serial number of the unit and the associated software versions for the CPU, DSP (Digital Signal Processor) and the Communication firmware present in the unit.

- If the Unit does not have a Front Panel LCD (Refer to Tables 2-1 through 2-3 inclusive for identification) Interface and the user has WINECP or if the user wishes not to use the unit's Front Panel Interface.
  1. Connect WIN ECP to the COM 0 port and attach the unit using the correct cable which varies whether the unit is a "CLASSIC " or Enhanced Front Panel Interface Version.
  2. Start WIN ECP.
  3. Depress the "DIRECT ACCESS" selection button presented in the pop-up window.
  4. Depress the "CONNECT" option selection presented within the pop-up window.
  5. Select the "HELP" menu option at the top right-hand section of the menu bar.
  6. Select the Drag-Down menu item "UNIT INFORMATION".
  7. A pop-up window shall appear with the Serial Number and Catalog Number.

2. At the back of the chassis, in the left-hand lower section of the unit, a label shall appear indicating the serial number and model number of the unit. It should match the data presented in the, WIN ECP or Front Panel Interface (FPI) menus. If it does not, please contact the factory.

As a final check, if the can be powered-down or if protection can be interrupted, loosen the front panel screws at the front of the unit. Remove the product component drawer from the chassis. Face the front panel interface, and rotate the board so that the semiconductor components are directly visible. On the backside of the metal panel supporting the Front Panel Interface, a label shall be available indicating the serial number and model number. These numbers should match those obtained in steps 1 and 2. If they do not, please contact the factory.

Section 3 - DPU2000, DPU1500R and DPU2000R Device Connectivity

Communication between devices is only possible through connectivity of the units through a physical media interface. There are two physical interface types on a DPU2000R and a DPU2000. Table 3-1 lists the characteristics for each of the port types. Those physical interfaces are:

- RS 232 (isolated and non-isolated)
- Ethernet – 10 Base T interface
- Ethernet – 10 Base FL interface

Table 3-1. Physical Interface Options

	DPU 2000R	DPU2000	DPU 1500R	Notes
COM 0	RS232 Non Isolated	RS232 Isolated	RS232 Non Isolated	Front Port Standard 10 Byte
COM 1	RS232 Non Isolated		RS232 Non Isolated	Standard 10 Byte Only
COM 2	RS232 Non Isolated		RS232 Non Isolated	Standard 10 Byte Only
COM 3	RS232 Isolated/RS485 Isolated or Modbus Plus	RS232 Isolated	RS232 Isolated/RS485 Isolated or Modbus Plus	DPU2000R – Communication Option Card Determines Physical Interface
AUX COM	10 base FL port and ethernet copper connection OR RS485 (Isolated) and/or INCOM	RS485 (Isolated) and/or INCOM	RS485 (Isolated) and/or INCOM	Physical Interface Dependent on Communication Option Card Interface Selected. Only one port is operationaldepending on the slide switch position on the card. (Note: Differs between ethernet capable hardware “E” option and serial board only.

RS232 Interface Connectivity

RS232 is perhaps the most utilized and least understood communication interface in use. RS232 is sometimes misinterpreted to be a protocol; it is in fact a physical interface. A physical interface is the hardware and network physical media used to propagate a signal between devices. Examples of physical interfaces are RS232 serial link, printer parallel port, current loop, V. 24, IEEE Bus… Examples of network media are, twisted copper pair, coaxial cable, free air…

RS232 gained widespread acceptance due to its ability to connect to another RS232 device or modem. A modem is a device, which takes a communication signal and modulates it into another form. Common forms of modems include telephone, fiber optic, microwave, and radio frequency. Modem connectivity allows attachment of multiple devices on a communication network or allows extension of communication distances in a network with two nodes. Physical connection of two devices or more than two devices require differing approaches. Figure 3-1 illustrates a topology using two devices (point to point topology). Figure 3-2 illustrates a multi-drop topology between many nodes. RS232 was designed to allow two devices to communicate without using intermediate devices.

Port Isolation

Network installation within a substation requires special considerations. A substation environment is harsh in that high levels of electromagnetic interference are present. Additional ground currents are present in such installations. RS232 is an unbalanced network in that all signals are referenced to a common ground. On longer cable runs, the potential of the signals at the sending device can be significantly lower than at the receiving end due to electrical interference and induced ground current. This increases with long runs of cable and use of

unshielded cable. ABB's Substation Automation and Protection Division recommends the length of RS232 cable be less than 10 feet (3 meters) for an un-isolated port and that the cable be shielded. Internal to a typical device, the RS232 transceivers are referenced to the electronic components internal ground. Any electrical interference could be coupled through the chip set and fed back to the device. Typical isolation ratings of a non-isolated port could be as low as 1 volt. Such a port could allow electrical feedback of noise to the electronics for any signal interference over 1 volt.

Coms 0 through 2 on DPU/TPU/GPU units are non–isolated. However an RS232 implementation on Com 3 uses opto-isolation technology which increases electrical isolation from the port to the devices internal circuitry to 2.3 kV. It is highly desirable to utilize this port in connection to devices in longer cable runs and dedicated communication networks. RS232 isolated ports are limited in connection distance for a maximum of fifty feet.

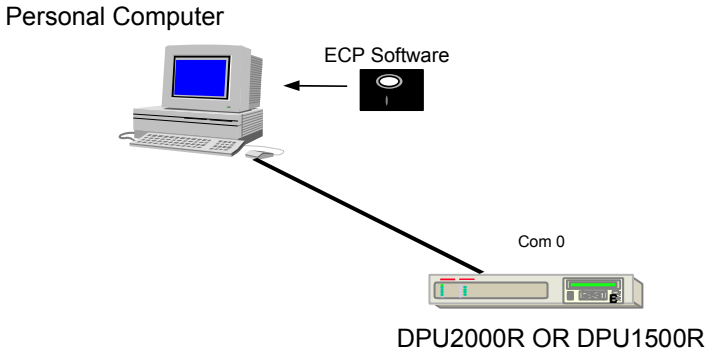


Figure 3-1. Point to Point Architecture Using RS232

RS232 Handshaking Defined

Handshaking is the ability of the device to control the flow of data between devices. There are two types of "handshaking", hardware and software. Hardware handshaking involves the manipulation of the RTS (Request to Send) and CTS (Clear to Send) card control signal lines allowing data communication direction and data flow rates to be controlled by the DTE device. Also the flow is controlled by the DTR (Data Terminal Ready) signal which allows the DCE operation.

Software handshaking involves the data flow control by sending specific characters in the data streams. To enable transmission, the XON character is transmitted. To disable reception of data, the transmitting device sends an XOFF character. If the XOFF character is imbedded within the data stream as information, the receiving node automatically turns off. This is the main weakness of software handshaking, inadvertent operation due to control characters being imbedded within data streams. Software handshaking is usually used in printer control.

The DPU2000, DPU1500R and DPU2000R devices do not incorporate handshaking, therefore, the control lines may be ignored as illustrated in Figure 3-3. However, some PC software utilizes handshaking, thus the port on the personal computer may require a special hardware configuration of the cable to the port. Consult with the software vendor to determine RS232 control and buffering requirements and the need for signal jumpers required in RS232 cabling.

The ports on the DPU/TPU/GPU have been tested for operation up to a speed of 19,200 baud. 19,200 baud is the typical data rate applicable for the operation of an asynchronous communication connection over RS232 without the use of additional timing lines.

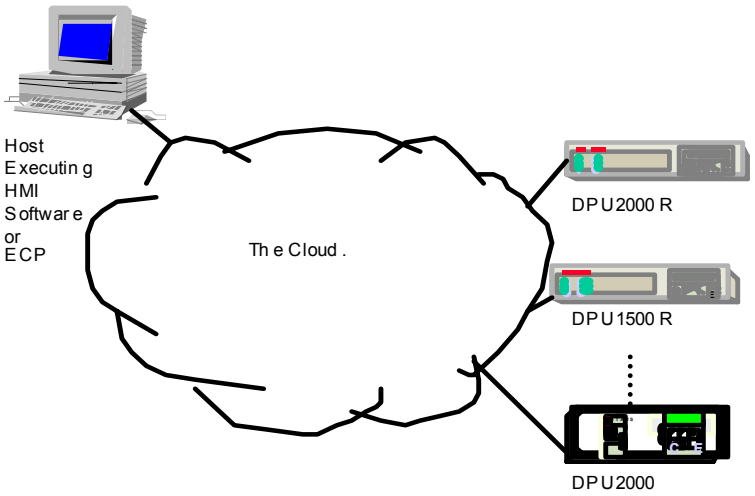


Figure 3-2. Multi-Drop Topology Using RS232

RS232 Cable Connectivity

A cable diagram is illustrated in Figure 3-3 and 3-4. Figure 3-3 shows the direction of communication signal transmission and the gender of the connectors used in constructing a communication cable. IT IS IMPORTANT TO REALIZE THAT THE ENHANCED PANEL OCI COM 0 INTERFACE OFFERS A DCE CONNECTION WHEREAS THE TRADITIONAL FRONT PANEL INTERFACE OFFERS A DCE CONNECTION. IT IS ALSO IMPORTANT TO REALIZE THAT BOTH MODELS OFFER COM.

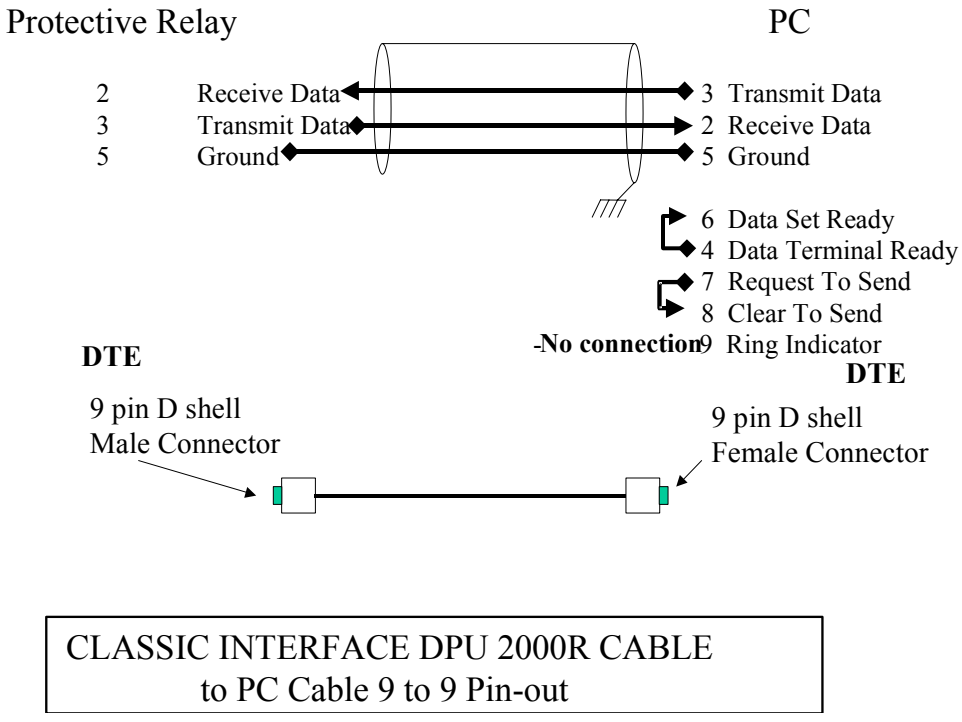


Figure 3-3. Classic DPU 2000R DB9 RS 232 Cable Diagram

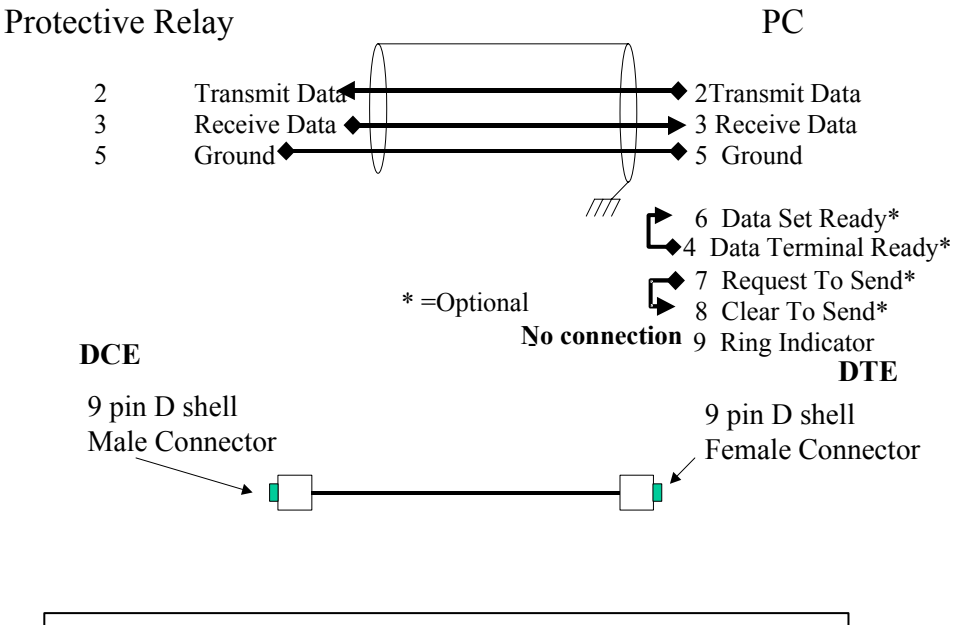


Figure 3-4. Enhanced OCI DPU 2000R DB 9 RS 232 Cable Diagram

An RS 232 interface was designed to simplify the interconnection of devices. Definition of terms may demystify issues concerning RS 232 interconnection. Two types of RS 232 devices are available, DTE and DCE. DTE stands for **D**ata **T**erminal **E**quipment whereas DCE stands for **D**ata **C**ommunication **E**quipment. These definitions categorize whether the device originates/receives the data (DTE) or electrically modifies and transfers data from location to location (DCE). Personal Computers are generally DTE devices while line drivers/modems/converters are DCE devices. DPU/TPU/GPU devices have RS 232 DTE implementation. Generally, with a few exceptions, a "straight through cable" (a cable with each pin being passed through the cable without jumpering or modification) will allow a DTE device to communicate to a DCE device.

Connection of a PC to a DPU2000 or DPU 2000R requires cable modification since the interconnected devices are both DTE. The same cabling would be utilized if one would connect two DCE devices. The classifications of DTE/DCE devices allow the implementers to determine which device generates the signal and which device receives the signal. Studying Figure 3-4, Pins 2 and 3 are data signals, pin 5 is ground whereas pins 1, 6, 7, 8, 9 are control signals. The arrows illustrate signal direction in a DTE device. The DPU 2000 and DPU 2000R series of protective devices do not incorporate hardware or software "handshaking".

If a host device has an RS 232 physical interface with a DB 25 connector, reference Figure 3-5 for the correct wiring interconnection.

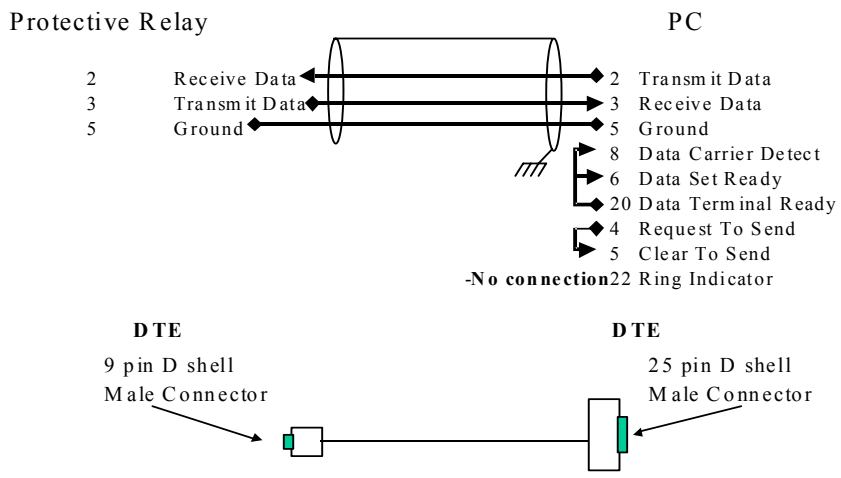


Figure 3-5. Connection of a DB 25 Connector to a DPU 2000 or DPU 2000R Classic Interface

It must be noted that the RS 232 port resident on the COM 3 interface port is not operational. It is used only for internal diagnostics and factory testing. Only COM 0 (Front Panel Interface Port) is operational when the UCA card is inserted in the device.

Ethernet Connectivity

There are two interfaces on the Ethernet card type "E" option when it is inserted in the unit. The two interfaces are available on the device are a 10 BASE T copper interface and a 10 BASE FL fiber optic interface. As illustrated in Figure 3-6 a slide switch is available to enable one of the two interfaces on the card. Slide the switch towards the card edge connectors to enable the FIBER OPTIC interface, slide the switch away from the card edge connector to enable the COPPER interface.

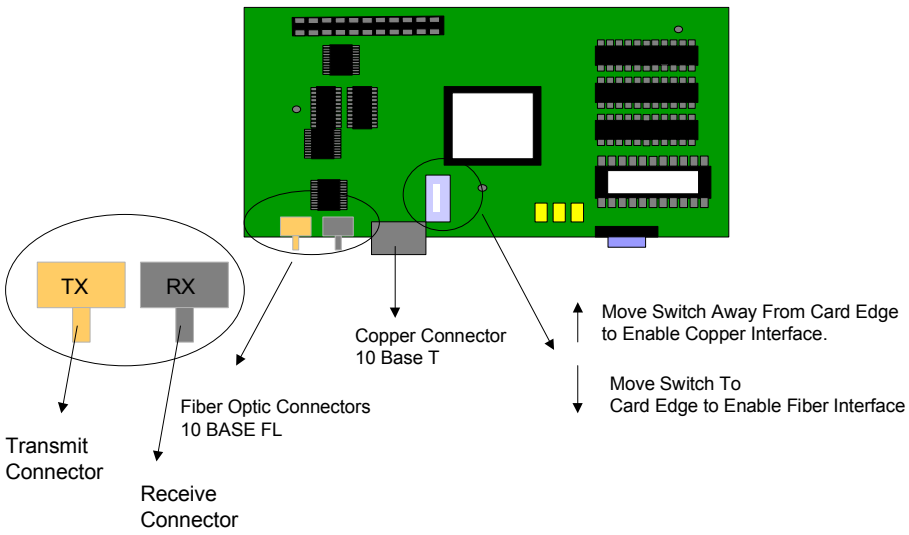


Figure 3-6. Connection Diagram for Copper/Fiber Interfaces

Ethernet connectivity is based upon a star topology connection. The Ethernet card operates with an Ethernet Hub or Switch to effectuate operation. The topology diagrams are illustrated in Figure 3-7 of this document illustrating the topology of the device.

If an Ethernet switch is used, reference the manufacturer's documentation for setup of the device.

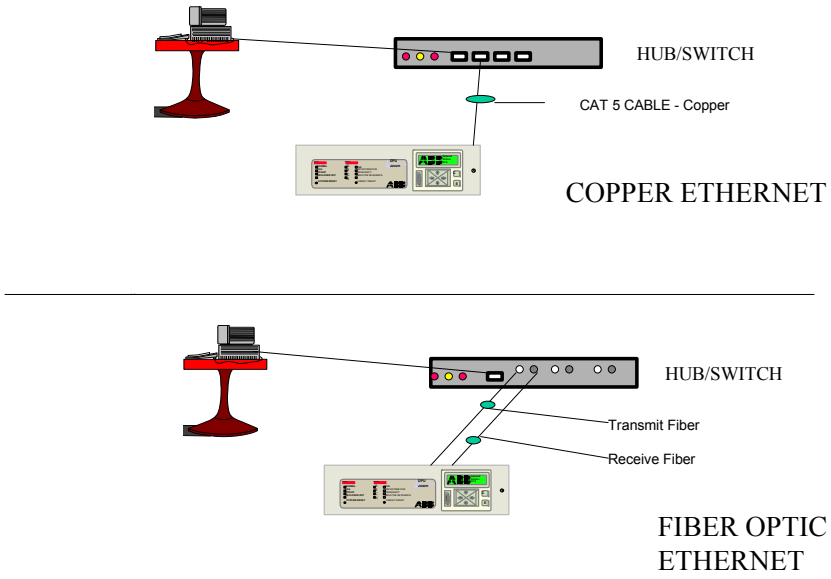


Figure 3-7. Typical Hub/Switch Connection Using Fiber or Copper Ethernet

Fiber Optic Specifications

THE COPPER PORT IS NOT ISOLATED. IT IS ONLY RECOMMENDED THAT THIS PORT BE USED FOR LABORATORY USES AND IN CASES WHERE ISOLATION OF THE RELAY IS NOT AN ISSUE.

The recommended cable type is an 890 nanometer (nM)/62.5 micrometer (µM) multimode cable with an ST connector on the DPU 2000R Ethernet card connector end must be used for the application. The other end must have an end connector corresponding to the connector style used on the hub/switch module.

The chipset used in the Fiber Optic section of the Ethernet card uses an Agilent HFBR-1414T for Transmission and an Agilent HFBR2416 for reception of the message.

Copper Ethernet Specifications

Copper Twisted Pair can be used to interconnect the DPU 2000R with the hub or switch. The cable must be a CAT-5 Cable with an RJ45 cable. The cable is commonly referred to as a "STRAIGHT THROUGH CABLE". DO NOT USE A "CROSS PINNED" CAT 5 copper cable.

RS485 Device Connectivity with the DPU2000 and DPU2000R

RS485 is one of the more popular physical interfaces in use today. It was developed as an enhancement of the RS422 physical interface. Its inherent strength is its ability to transmit a message over a twisted pair copper medium of 3000 feet in length. An RS485 interface is able to transmit and receive a message over such a distance because it is a balanced interface. That is, it does not reference the signal to the system's electrical

ground, as is the case in an RS232 interface. RS485 references the communication voltage levels to a pair of wires isolated from system ground. Depending on the manufacturer's implementation, isolation may be optical or electronic. RS485 has two variants, two wires and four-wire. In the two-wire format, communication occurs over one single wire pair. In four-wire format, communication occurs over two wire pairs, transmit and receive. The two-wire format is the most common in use. The DPU2000, DPU1500R and DPU2000R support half duplex two-wire format only. The RS485 port is also optically isolated to provide for 3000 V of isolation.

The RS485 network supported and recommended by ABB requires the use of three conductor shielded cable. Suggested RS485 cable and the respective manufacturer's wire numbers are:

- ALPHA 58902
- Belden 9729
- Belden 9829
- Carol 58902

ABB does not support deviations from the specified cables. The selected cable types listed are of the type which have the appropriate physical and electrical characteristics for installation in substation environments.

A multi-drop RS485 connection is illustrated in Figure 3-2. Three wires, Positive (Terminal 9), Negative (Terminal 8) and Ground (Terminal 10). RS485 requires a termination resistor at each end of the communication cable. The resistance shall be from 90 to 120 ohms. Additionally, depending upon the RS485 physical interface converter used, a pull-up and pull-down resistor may be added to bias the line to decrease the amount of induced noise coupled onto the line when no communications are occurring. Internal to the DPU2000, DPU1500R and DPU2000R are jumpers which when inserted in the proper position (as referenced in Figure 3-5), bias the line by inserting the proper pull-up, pull-down, and termination resistors. To configure the Jumpers J6, J7, and J8, execute the following procedure:

- Refer to Tables 1 to 2-7 and Figures 2-4 or 2-5 depending upon the model of Distribution Protection Unit which is installed.
- Refer to Figure 3-6 illustrating the placement of J6, J7 and J8 (or J16, J17, or J18 on a type 8 card enabling RS 485 for COM 3). J6 (or J16 for COM 3) inserts a 120 ohm resistor between transmit and receive lines. J7 or (J17 for COM 3) and J8 or (J18 for COM 3) inserts a pull-up and pull-down resistor. The IN position inserts the associated resistor in to the circuit. The OUT position removes the resistor from the circuit.
- Insert the DPU2000 and DPU2000R unit into the chassis as per the instructions associated with Figures 2-4 or 2-5.
- Tighten the knurled screws at the front of the unit.
- **IT IS advisable to place a sticker on the front of DPU2000 AND DPU2000R/DPU1500R indicating that it is a terminated end of line unit.** This makes maintenance of installed units easier.

The following example illustrates an interconnection of the DPU2000 and DPU2000R with a host device through a UNICOM physical interface connection using a 3-wire connection method. It should be noted that the RS485 design on ABB relay products incorporates isolation. That is, the RS485 ground is electrically isolated from the internal circuitry thereby assuring minimal interference from the extreme noise environments found in a substation. Care should be used when installing an RS485 communication network. The recommended configuration must be followed as shown in Figure 3-8, 3-9, 3-10, and 3-11. Jumpers J6, J7, and J8 should be inserted to provide termination and pull-up at the DPU2000 and DPU2000R end. Although not shown, a 120 ohm resistor should be inserted between the TX/RX+ and TX/RX- pairs to provide for termination at the transmission end.

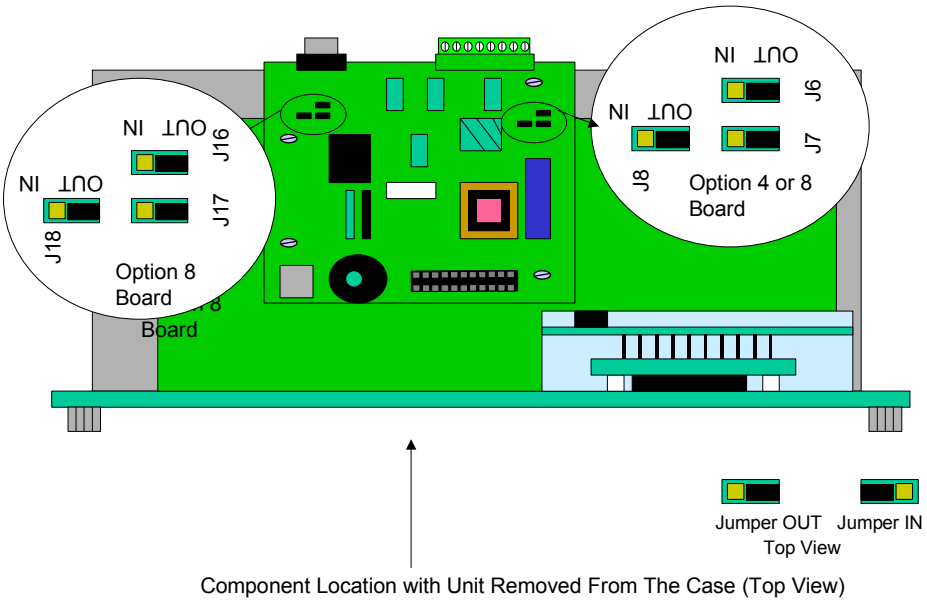


Figure 3-8. Location of RS485 Resistor Configuration Jumpers in the DPU2000R/DPU1500R

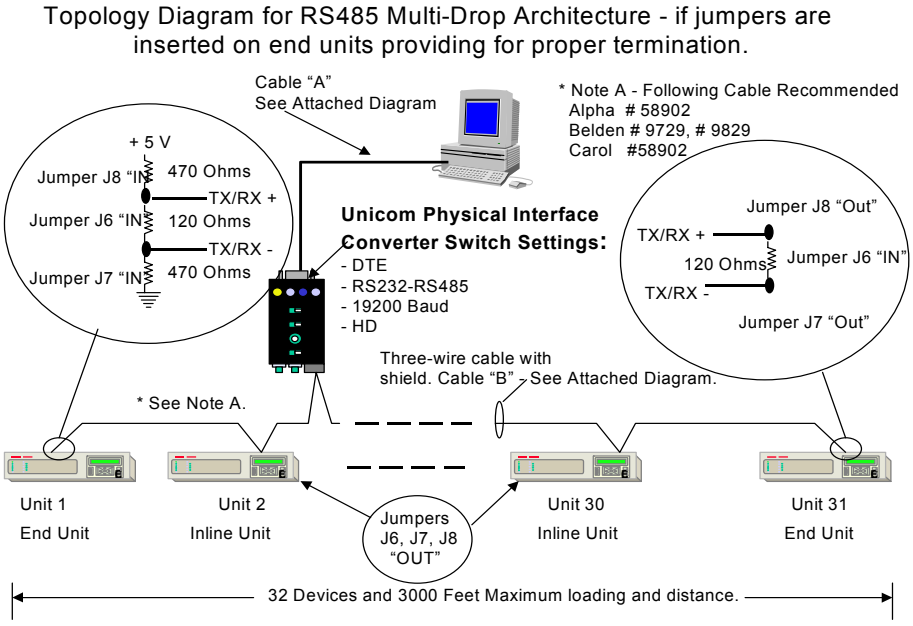


Figure 3-9. RS485 Topology Configuration for the DPU2000R

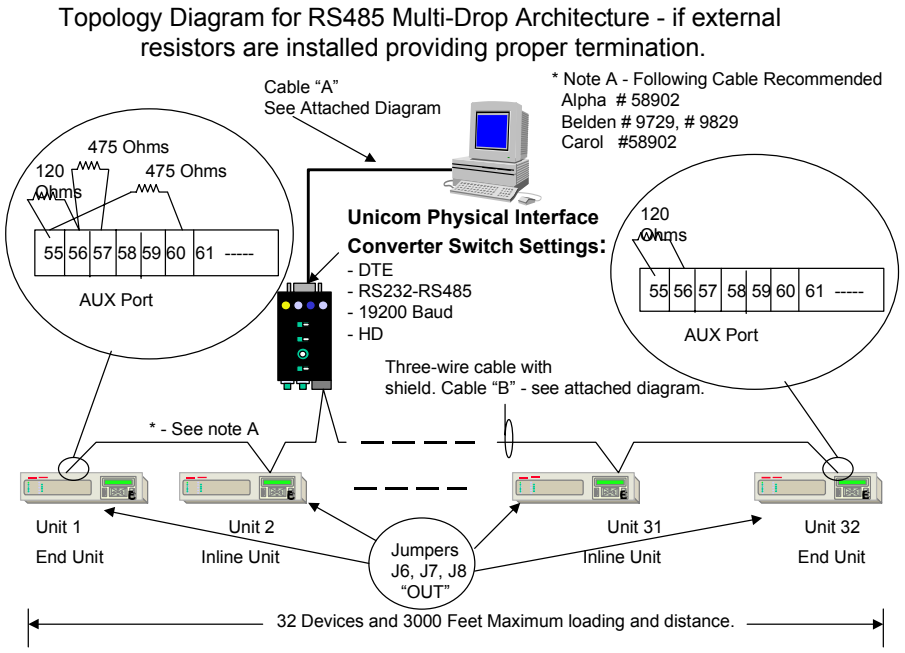


Figure 3-10. Alternate External Resistor Placement for the DPU2000R

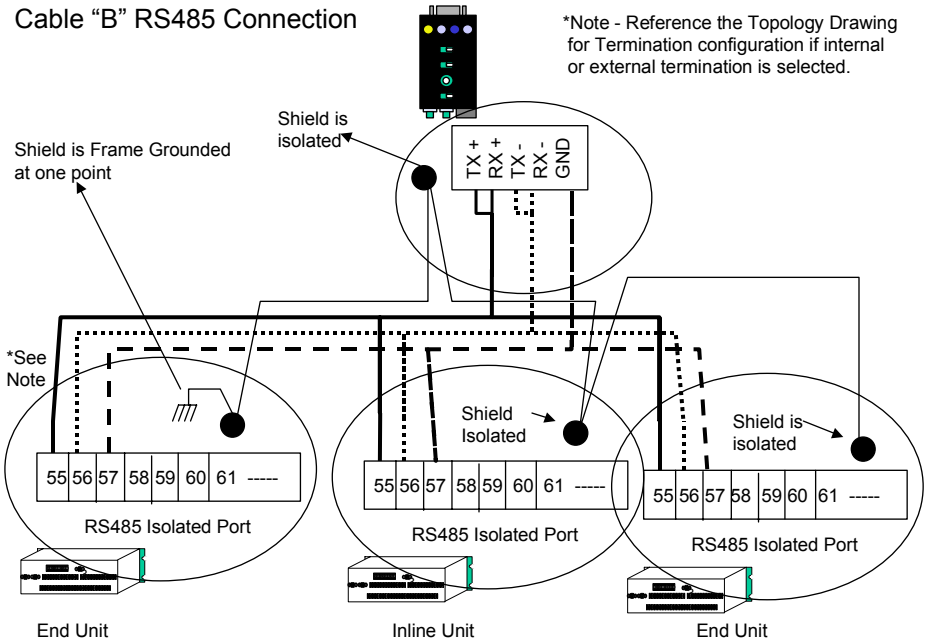


Figure 3-11. RS485 Communication Cabling (DPU2000R)

The DPU2000 has the two wire RS485 communication connectivity terminals located in a different position than that for the DPU2000R/DPU1500R. Table 3-2 lists the AUX COM connector signal assignments for the DPU2000.

Table 3-2. DPU2000 AUX COM Signal Assignments

Pin Number	Pin Definition
65	IRIG B Minus
66	IRIG B Plus
67	INCOM
68	INCOM
69	+5 VDC (100 mA max)
70	Reserved
71	Reserved
72	RS485 Common/(Return)
73	RS485 Minus
74	RS485 Plus

Therefore, connection of several DPU2000 units on a communication network would yield the wiring as depicted in Figure 3-9. DPU2000 and DPU2000R/DPU1500R units may be interconnected on the same network as long as this signal position difference is noted and signal polarity is followed. ABB offers a special in-line connector for the TYPE 8 RS 485 COM 3 connection. This special connector allows the COM 3 DB 9 connector to be converted into a 9 position PHOENIX connector allowing easy in-line wiring. The part number for this connector is 602133-009. Please contact your ABB distributor or representative for price and ordering information for this product.

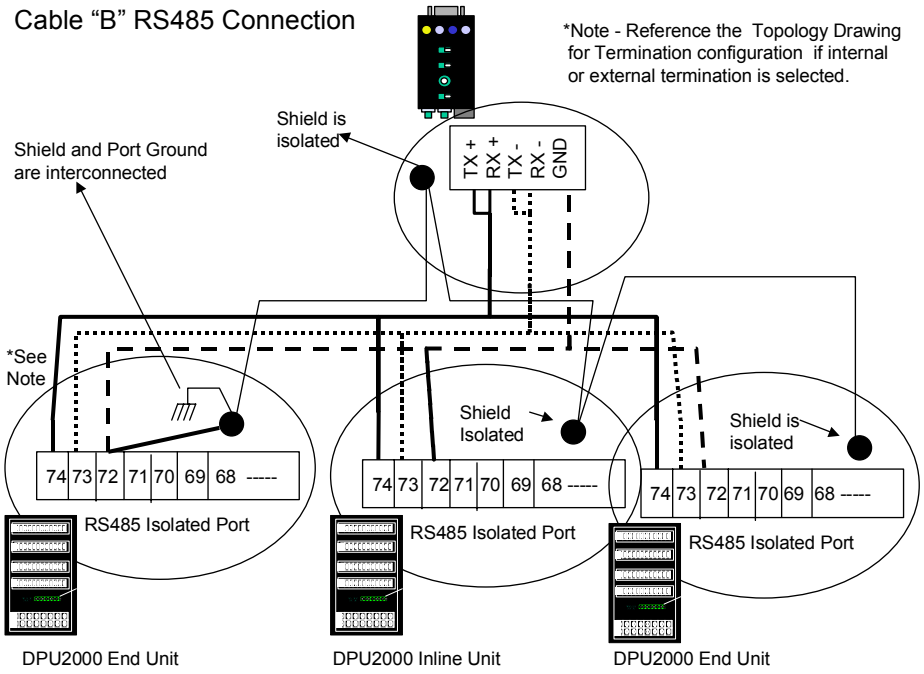


Figure 3-12. DPU2000 RS485 Wiring Diagram

Section 4 - DPU2000 and DPU2000R Device Parameterization

Establishing DPU 2000R communication depends upon correct parameterization of the communication menus within the unit. Parameterization may occur via the unit's front panel interface of through ECP (External Communication Program) or WIN ECP (WINdows External Communication Program). Modbus, Modbus Plus and DNP require certain parameterizations. Even COM 0 requires certain parameterization to communication with the configuration program.

COM 0 Port (Front Port Configuration)

In order to attach a configuration program to the DPU 2000R, the correct parameters must be set up within the unit. The supported parameters are listed in Table 4-1 below. The protocol for the unit is addressable Standard 10 Byte. To view the communication port parameters it is advised that they should be veiwed via the unit's front panel interface. If the DPU 2000R does not have a front panel interface, the parameters should be marked on the front panel sticker with the port's parameters.

The keystrokes required for visualizing the communication port parameters from the metering display are:

1. Depress the "E" pushbutton.
2. Depress the "↓" key once to select the SETTINGS menu and then depress the "E" pushbutton.
3. Depress the "E" pushbutton to select the SHOW SETTINGS menu selection.
4. Depress the "↓" key six times to select the COMMUNICATIONS menu and then depress the "E" pushbutton.
5. Under the SHOW COM SETTINGS MENU, the following shall be displayed for the Front Panel RS 232 port (FP).
   - Unit Node Address (Address displayed in HEX)
   - FP RS 232 Baud
   - FP RS 232 Frame

Other parameters shall be shown. The parameters listed shall vary in accordance with the communication card inserted within the unit. However, the FP displayed parameters must match with the parameters configured in the Standard Ten Byte section of the ECP package.

One may change parameters via the front panel interface. The selections for each parameter required in Front Panel Port configuration is shown in Table 4-1.

Table 4-1. DPU 2000R Com Port 0 Front Panel Interface Parameters

Option	Selection	Notes
Unit Node Address	1 to FFF (1 = default setting)	1 to 2048 decimal node address
FP RS 232 Baud	300	Selectable Baud Rates for the Standard Ten Byte Front Panel Port.
	1200	
	2400	
	4800	
	9600 (default setting)	
FP RS 232 Frame	N – 8 – 1 (default setting)	No Parity 8 Data Bits 1 Stop Bit
	N – 8 – 2	No Parity 8 Data Bits 2 Stop Bits

Modification of the Front Panel Parameters for a CLASSIC DPU 2000R, change of the settings is accomplished via the following keystrokes:

1. From the metering menu depress the "E" key.
2. Depress the "↓" key once to select the SETTINGS menu and then depress the "E" pushbutton.
3. Depress the "↓" key once to select the SHOW SETTINGS menu selection. Depress the "E" pushbutton.
4. Depress the "↓" key seven times to select the COMMUNICATIONS menu and then depress the "E" pushbutton.
5. Enter the unit's password, one digit at a time. The default password is four spaces. Depress the "E" pushbutton once.

6. The CHANGE COMMUNICATION SETTINGS menu shall be displayed. With the cursor at the Unit Address field, depress "E". The unit address can be modified. The address selected in this field will configure the address for the entire node. Use the "↓" and "↑" arrow keys to select the password digit entry. Use the "→" and "←" keys to select the digit to configure. Depress "E" to save the digits. Depress "C" to return to the root menu.
7. Once returned to the main menu, depress the "↓" key once to select the FRONT RS 232 BAUD RATE menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the root menu.
8. Once returned to the main menu, depress the "↓" key once to select the FRONT RS 232 FRAME menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the root menu.
9. To Save the selections configured in the previous steps depress the "C" pushbutton. A query will be presented to the operator "Enter YES to save settings <NO>. Use the "→" and "←" keys to select the option YES and depress "E" to save the settings.

If one has an Enhanced Operator Interface on a DPU 2000R, the following procedure allows for the modification and the viewing of the COM 0 port parameters.

1. Depress F1 <MENU>
2. Depress F2 <MAIN MENU>
3. Depress F3 <SHOW SETTINGS MENU>
4. Depress F6 <PAGE DOWN>
5. Depress F4 <COMMUNICATION MENU>
6. The selections for UNIT ADDRESS, and FP RS 232 Baud, as well as FP RS 232 Framing is visible.

To change the settings for the front panel port, follow the following keystroke sequence for the Enhanced Version of the DPU 2000R.

1. Depress F1 <MENU>
2. Depress F2 <MAIN MENU>
3. Depress F4 <CHANGE SETTINGS MENU>
4. Depress F6 <PAGE DOWN>
5. Depress F5 <COMMUNICATION MENU>
6. Enter the PASSWORD using the F2, F3, and F4 keys . The default password is four spaces.
7. Depress F6 to enter the password. If it is accepted, one shall be able to change the following parameters:
   F2 UNIT ADDRESS
   F3 FP RS 232 BAUD
   F4 FR RS 232 FRAME
8. Once the appropriate parameters have been entered for the DPU 2000R, then depress F6 END OF COMM to enter the screen to save the parameters.
9. Depress F1 <ESC>.One shall be prompted for SAVE SETTINGS? Depressing F4 – YES, F5 NO.

If the unit does not have a front panel interface, it is advisable that the communication port parameters be marked on the front of the unit. If the parameters are not known, please contact ABB Technical Support to obtain the procedure to determine the parameters or take the unit out of service and reset the port parameters.

Figure 4-1 illustrates the parameterization screen in WIN ECP which must be parameterized allowing communication between the configuration unit and the DPU 2000R. The WIN ECP VERSION for parameterization of the UCA or Modbus TCP/IP board must be version 4.3 or greater.

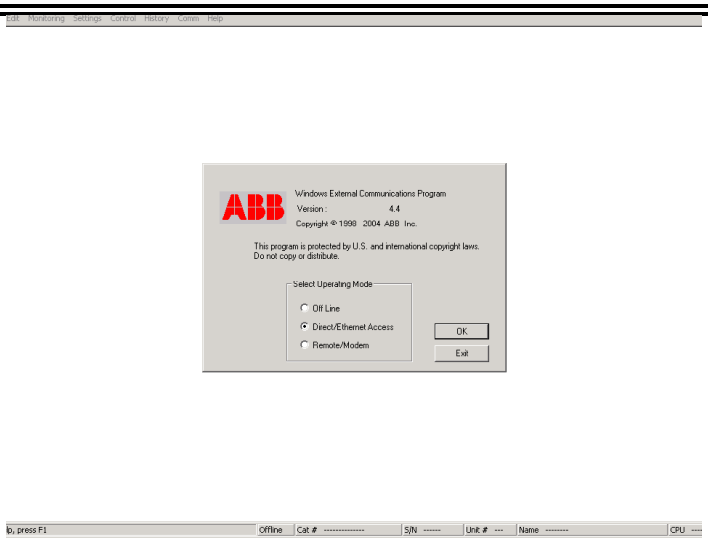


Figure 4-1. Initial WIN ECP Communication Configuration Screen

A direct connect is selected in this instance allowing retrieval and configuration of the relay parameters. Notice that the connection may be accomplished via Serial connection or Ethernet if available in the DPU 2000R. Once the OK button is depressed, the screen shown in Figure 4-2 is presented to the operator.

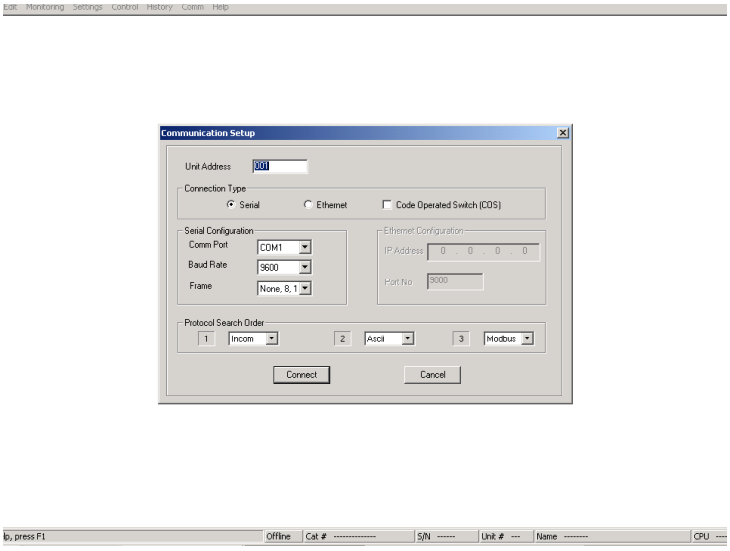


Figure 4-2a. Communication Port Setup Screen for Serial or Ethernet Communication

The selections in WIN ECP are illustrated in Table 4-2. The settings must agree with those configured in the DPU 2000 and DPU 2000R. Radio Buttons are available to connect the configuration terminal to the DPU 2000R depending upon the protocol and interface used. The DPU 2000R also allows for programming using Modbus, or Standard 10 Byte protocols.

Table 4-2. WIN ECP Communication Port Settings

Option	Selection	Notes
COM PORT	COM 1	Personal Computer Port Selection for ECP to DPU 2000R connection.
	COM 2	
	COM 3	
	COM 4	
BAUD RATE	**300**	Baud Rates Offered for DPU 2000R connection to the WIN ECP RS 232 port connection
	1200	
	2400	
	4800	
	9600 (default setting)	
	19200	
Frame	**None – 8 – 1 (default setting)**	No Parity 8 Data Bits 1 Stop Bit
	None– 8 – 2	No Parity 8 Data Bits 2 Stop Bits
	Even – 8 – 1	Even Parity 8 Data Bits 1 Stop Bit
	Odd – 8 – 1	Odd Parity 8 Data Bits 1 Stop Bit
	Even – 7- 1	Even Parity 7 Data Bits 1 Stop Bit
	None – 7 – 2	Even Parity 7 Data Bits 2 Stop Bits
	Odd – 7 – 1	Odd Parity 7 Data Bits 1 Stop Bit
Unit Address	1 – FFF (1 = Default)	Unit Address in HEX
Ethernet	IP 4 Version Addressing	4 decimal Octets
NOTE : Bold indicates Selections Supported by WIN ECP AND DPU 2000 / DPU 2000R		

COM Port 1 Option Settings (DPU 2000R ONLY) [Catalog 587 XXX00-XXX0 or 587 XXX50-XXX0]

If the unit does not have a front panel interface, the rear port is on the DPU 2000R is active. The Configuration screens through WIN ECP are shown in Figure 4-3 for reference. The communication options may not be configured via the front panel interface since this port is only active if the unit does not have a front panel communication port interface (see Section 3 of this document for further information). The communication protocol supported on this port is Standard Ten Byte Only.

Table 4-3 illustrates the port configuration options available for this COM PORT 1. Figure 4-3 illustrates the WIN ECP screen used to configure Communication Port 1 in the DPU 2000R.

Table 4-3. COM Port 1 and COM Port 2 WIN ECP Port Settings

Option	Selection	Notes
BAUD RATE	300	Com Port Baud Rate Selections Via WIN ECP
	1200	
	2400	
	4800	
	9600 (default setting)	
	19200	
	38400	
Frame	None – 8 – 1 (default setting)	No Parity 8 Data Bits 1 Stop Bit
	None– 8 – 2	No Parity 8 Data Bits 2 Stop Bits
	Even – 8 – 1	Even Parity 8 Data Bits 1 Stop Bit
	Odd – 8 - 1	Odd Parity 8 Data Bits 1 Stop Bit

	Even – 7- 1	Even Parity 7 Data Bits 1 Stop Bit
	None – 7 – 2	Even Parity 7 Data Bits 2 Stop Bits
	Odd – 7 - 1	Odd Parity 7 Data Bits 1 Stop Bit

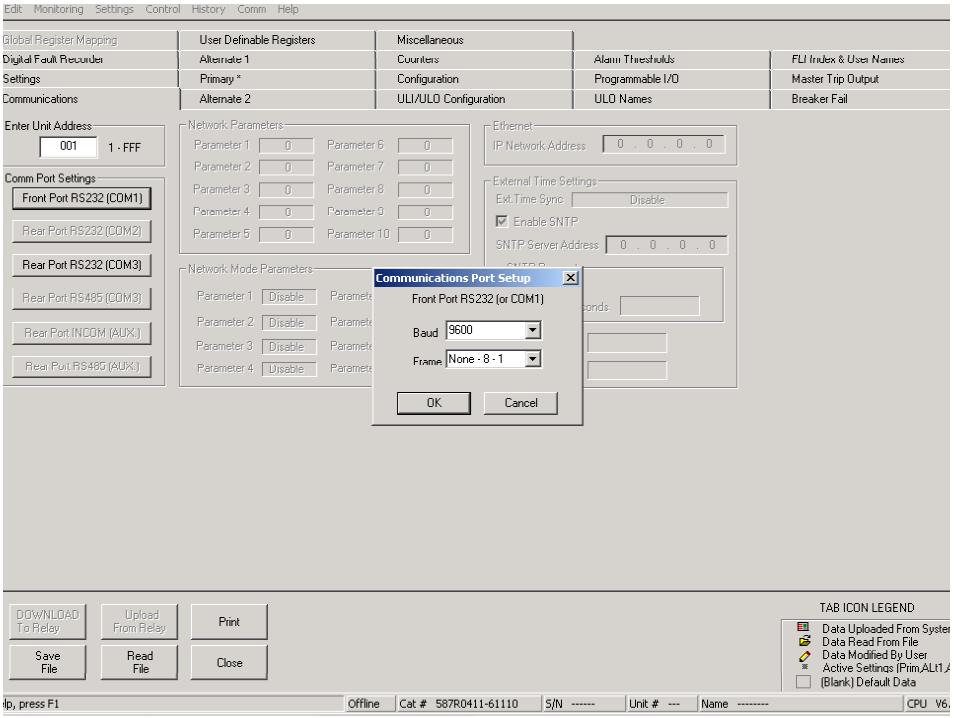


Figure 4-3. COM Port 1 WinECP Setting Screen

COM Port 2 Option Settings (DPU1500R or DPU2000R Only) [Catalog 587 XXXX0-XXX0 or 587 XXXX6-XXX4] or [Catalog 577 XXXX0-XXX0]

There are two option boards, which enable communication port 2 for the DPU2000R/DPU1500R. Figure 4-4 illustrates the configuration screen for the COM Port 2 options when viewed on WinECP.

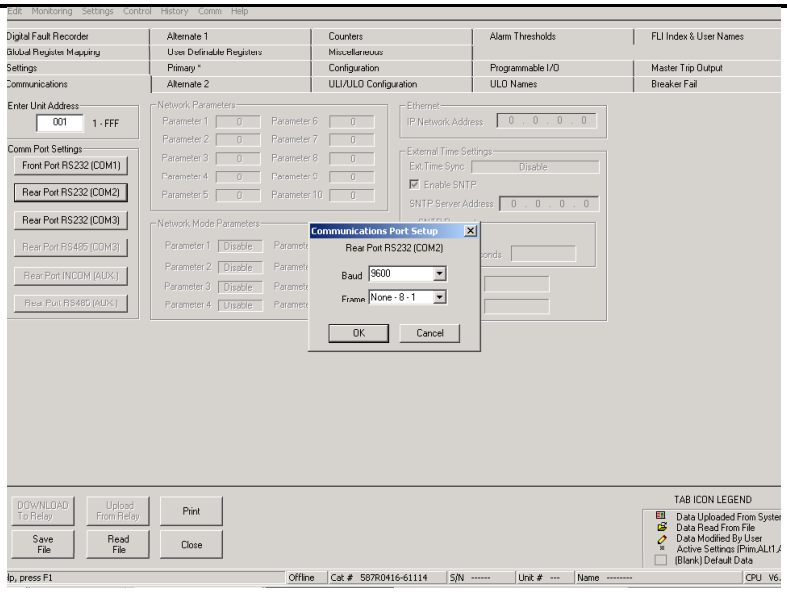


Figure 4-4. WinECP COM Port 2 Communication Screen

The options for configuration are listed in Table 4-3.

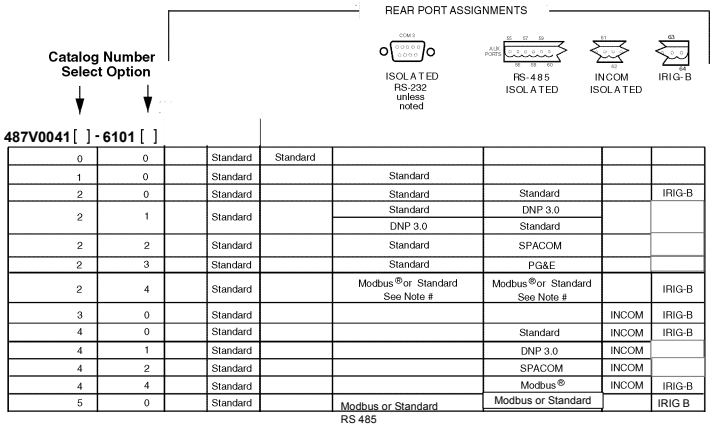
COM Port 3 and AUX COM Configuration

The DPU2000, DPU1500R, and DPU2000R share the same commonality in that two rear ports may be available depending upon the hardware inserted in the units. The configuration techniques vary in that the configuration depends upon the protocol included on the board itself. Figure 4-5 lists the combinations for the DPU2000R. Figure 4-6 lists the communication option combinations for the DPU2000. Figure 4-7 lists the option for the DPU1500R.

REAR PORT ASSIGNMENTS

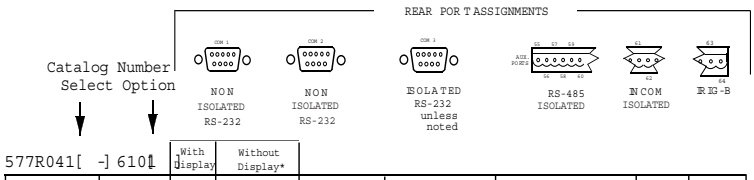
Catalog Number Select Option								
				NON ISOLATED RS-232	NON ISOLATED RS-232	ISOLATED RS-232 unless noted	RS-485 ISOLATED	INCOM ISOLATED	IRIG- B
587R041[ ] - 6101[ ]		With Display	Without Display*						
0	0		ABB Ten Byte	ABB Ten Byte					
1	0		ABB Ten Byte			ABB Ten Byte			
2	0		ABB Ten Byte			ABB Ten Byte	ABB Ten Byte		IRIG-B
2	1		ABB Ten Byte			ABB Ten Byte	DNP 3.0		
						DNP 3.0	ABB Ten Byte		
2	4		ABB Ten Byte			Modbus® or ABB Ten Byte See Note #	Modbus® or ABB Ten Byte See Note #		IRIG-B
3	0		ABB Ten Byte					INCOM	IRIG-B
4	0		ABB Ten Byte				ABB Ten Byte	INCOM	IRIG-B
4	1		ABB Ten Byte				DNP 3.0	INCOM	
4	4		ABB Ten Byte				Modbus®	INCOM	IRIG-B
5	0		ABB Ten Byte				ABB Ten Byte		
6	4		ABB Ten Byte	ABB Ten Byte		Modbus Plus™			
7	4		ABB Ten Byte			Modbus Plus™	ABB Ten Byte		
8	0		ABB Ten Byte			ABB Ten Byte (RS 485)	ABB Ten Byte		IRIG-B
8	1		ABB Ten Byte			ABB Ten Byte (RS 485)	DNP 3.0 (RS 485)		
						DNP 3.0 (RS 485)	ABB Ten Byte (RS 485)		
8	4		ABB Ten Byte			Modbus® or ABB Ten Byte (RS-485) See Note #	Modbus® or ABB Ten Byte See Note #		IRIG-B

Figure 4-5. DPU2000R Communication Capability Chart



0	0		Standard	Standard				
1	0		Standard		Standard			
2	0		Standard		Standard	Standard		IRIG-B
2	1		Standard		Standard	DNP 3.0		
					DNP 3.0	Standard		
2	2		Standard		Standard	SPACOM		
2	3		Standard		Standard	PG&E		
2	4		Standard		Modbus®or Standard See Note #	Modbus®or Standard See Note #		IRIG-B
3	0		Standard				INCOM	IRIG-B
4	0		Standard			Standard	INCOM	IRIG-B
4	1		Standard			DNP 3.0	INCOM	
4	2		Standard			SPACOM	INCOM	
4	4		Standard			Modbus®	INCOM	IRIG-B
5	0		Standard		Modbus or Standard RS 485	Modbus or Standard		IRIG B

Figure 4-6. DPU2000 Communication Capability Chart



		With Display	Without Display*					
0	0		ABB Ten Byte	ABB Ten Byte				
1	0		ABB Ten Byte		ABB Ten Byte			
2	1		ABB Ten Byte		ABB Ten Byte	DNP 3.0		
					DNP 3.0	ABB Ten Byte		
2	4		ABB Ten Byte		Modbus®	ABB Ten Byte		IRIG-B
					ABB Ten Byte	Modbus® or ABB Ten Byte		
3	0		ABB Ten Byte				INCOM	IRIG-B
4	1		ABB Ten Byte			DNP 3.0	INCOM	
4	4		ABB Ten Byte			Modbus®	INCOM	IRIG-B
						ABB Ten Byte		
5	0		ABB Ten Byte			ABB Ten Byte		

Figure 4-7. DPU1500R Communication Capability Chart

Serial Modbus Protocol Selection and Configuration for Port 3 and AUX COM

Serial Modbus requires parameterization above that of the unit number, baud rate, and frame selection. The philosophy is that (if the hardware is provided on the card) one or both ports may be configured with Standard Ten Byte or Modbus (ASCII or RTU). Ethernet Modbus parameterization does not require emulation selection. The parameterization requires entry of constants in the Parameter Section of the Communication configuration menu tab (Via WinECP) or Configuration Menu (via the Front Panel Interface). If as per the above tables, the Modbus card is to be configured via software (WinECP), the following must be configured via the front panel interface or via WinECP.

The following table represents Option 2 Serial Port Communications Settings:

Parameter 1	Mode Parameter 1	Mode Parameter 2	(COM 3)	RS485 (AUX)
0	Disabled	Disabled	STD	STD
1	Disabled	Disabled	Modbus RTU	STD
1	Enabled	Disabled	Modbus ASCII	STD
2	Disabled	Disabled	STD	Modbus RTU
2	Disabled	Enabled	STD	Modbus ASCII
3	Disabled	Disabled	Modbus RTU	Modbus RTU
3	Enabled	Disabled	Modbus ASCII	Modbus RTU
3	Disabled	Enabled	Modbus RTU	Modbus ASCII
3	Enabled	Enabled	Modbus ASCII	Modbus ASCII

NOTE: STD is Standard Ten Byte Protocol Selected.

If a Modbus capable card is inserted into the unit, the configuration screen appears as shown in Figure 4-8. The Baud and Frame Options allowable for RTU and ASCII communication are shown in Table 4-4

Table 4-4. Valid Parameter Selections for Standard Ten Byte and Modbus Serial Protocols

Protocol Selected	Baud Rate Selections	Frame Selections
Modbus ASCII	300,1200, 2400, 4800, 9600, 19200	• Odd Parity, 7 Data Bits, One Stop Bit • Odd Parity , 7 Data Bits, Two Stop Bits • Even Parity, 7 Data Bits, One Stop Bit • Even Parity, 7 Data Bits, Two Stop Bits
Modbus RTU	300,1200, 2400, 4800, 9600, 19200	• Even Parity, 8 Data Bits, One Stop Bit • No Parity, 8 Data Bits, One Stop Bit • Odd Parity, 8 Data Bits, One Stop Bit • No Parity, 8 Data Bits, Two Stop Bits
Standard Ten Byte	300,1200, 2400, 4800, 9600, 19200	• Odd Parity, 7 Data Bits, One Stop Bit • Odd Parity , 7 Data Bits, Two Stop Bits • Even Parity, 7 Data Bits, One Stop Bit • Even Parity, 7 Data Bits, Two Stop Bits • Even Parity, 8 Data Bits, One Stop Bit • No Parity, 8 Data Bits, One Stop Bit • Odd Parity, 8 Data Bits, One Stop Bit • No Parity, 8 Data Bits, Two Stop Bits
Modbus TCP/IP	None	• None

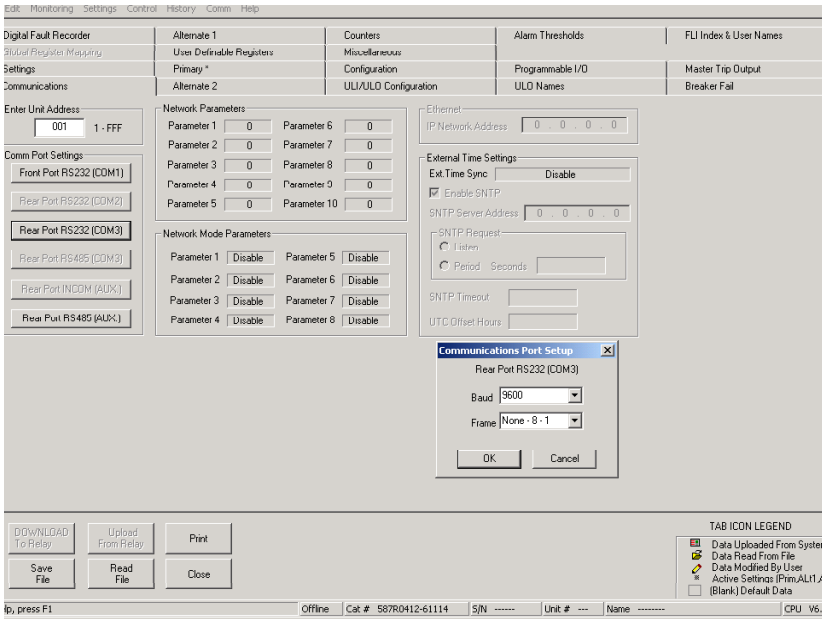


Figure 4-8. Modbus, DNP 3.0, SPACOM, and PG&E Port 3 Communication Screen

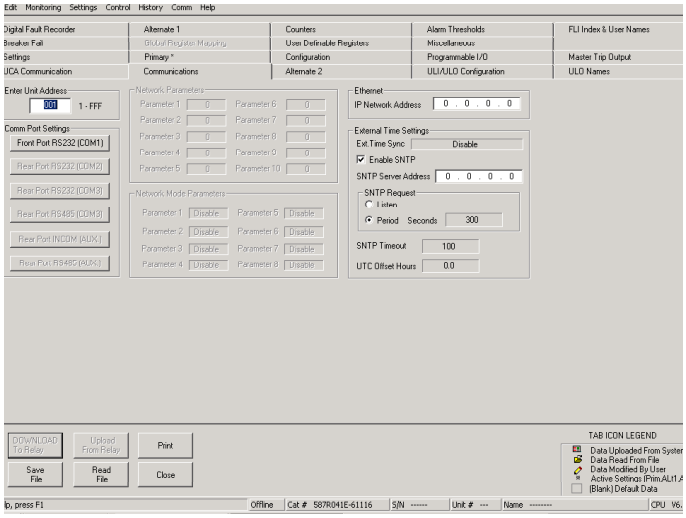


Figure 4-8a Modbus TCP/IP, UCA, or Standard 10 Byte TCP/IP Communication Screen For Ethernet.

One should notice that the Parameter Section and the Mode Parameter Section is not greyed if the relay selection for Modbus is enabled (as discerned from the relay part number).

If the card is associated with Option Card 2 (the digit before the dash number in the part number), both the RS232 port and RS485 (AUX COM), the WinECP and Front Panel Interface will be represented in the query for configuration. This is illustrated in Figure 4-8 above.

If the card is associated with Option Card 8 (COM 3 and AUX COM being RS485), the configuration software program and the front panel interface shall indicate that COM 3 is RS485 in that the query will indicate RP 485. This is illustrated in Figure 4-8 above.

If the communication card option is an “E” then no selection will be visible for the COM 3 port option since no protocol is supported for that platform. This is illustrated in Figure 4-8a above.

The Front Panel Interface configuration procedure is as follows:

Modification of the Front Panel Parameter for the "classic" DPU FPIsettings is accomplished via the following keystrokes for serial protocols offered on the Type 2 or Type 8 boards:

1. From the metering screen depress the "E" key.
2. Depress the "↓" key once to select the SETTINGS Menu and then depress the "E" pushbutton.
3. Depress the "↓" key once to select the CHANGE SETTINGS Menu selection. Depress the "E" pushbutton.
4. Depress the "↓" key seven times to select the COMMUNICATIONS Menu and then depress the "E" pushbutton.
5. Enter the unit's password, one digit at a time. The default password is four spaces. Depress the "E" pushbutton once.
6. The CHANGE COMMUNICATION SETTINGS Menu shall be displayed. With the cursor at the Unit Address field, depress "E". The unit address can be modified. The address selected in this field will configure the address for the entire node. Use the "↓" and "↑" arrow keys to select the password digit entry. Use the "→" and "←" keys to select the digit to configure. Depress "E" to save the digits. Depress "C" to return to the Root Menu.
7. Once returned to the Main Menu, depress the "↓" key four times to select the RP RS232 BAUD RATE (See Note 1) Menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
8. Once returned to the Main Menu, depress the "↓" key once to select the RP RS232 FRAME (See Note 2) Menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
9. Once returned to the Main Menu, depress the "↓" key once to select the RP RS485 BAUD RATE (See Note 3) menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
10. Once returned to the Main Menu, depress the "↓" key once to select the RP RS485 FRAME (See Note 4) menu and then depress the "E" pushbutton. The selections for the menu are listed in Table 4-1. Use the "→" and "←" keys to select the baud rates for the port. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
11. Once returned to the Main Menu, depress the "↓" key once to select the RP IRIG B selection. Refer to Section 5 to determine the configuration for the IRIG B of the unit.
12. Once returned to the Main Menu, depress the "↓" key once to select the PARAMETER 1 Menu and then depress the "E" pushbutton. The selections for this field may range from 0 to 255. Use the "→" and "←" keys to select appropriate entry for Parameter 1 as described above. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
13. Once returned to the Main Menu, depress the "↓" key twelve times to select the MODE PARAMETER 1 Menu item and then depress the "E" pushbutton. The selections for this field are enable and disable. Use the "→" and "←" keys to select appropriate entry for MODE PARAMETER 1 as described above. Depress "E" to select the entry. Depress "C" to return to the Root Menu.
14. Once returned to the Main Menu, depress the "↓" key once to select the MODE PARAMETER 2 Menu item and then depress the "E" pushbutton. The selections for this field are enable and disable. Use the "→" and "←" keys to select appropriate entry for MODE PARAMETER 1 as described above. Depress "E" to select the entry. Depress "C" to return to the Root Menu.

15. To Save the selections configured in the previous steps depress the “C” pushbutton. A query will be presented to the operator “Enter YES to save settings <NO>”. Use the “→” and “←” keys to select the option YES and depress “E” to save the settings.

    NOTE 1: If the DUAL RS485 Board (Option 8) is selected, the query shall be modified as: RS485 – 1 Baud. If the hardware does not support COM 3, this query shall be omitted.
    NOTE 2: If the DUAL RS485 Board (Option 8) is selected, the query shall be modified as RS485 – 1 Frame. If the hardware does not support COM 3, this query shall be omitted.
    NOTE 3: If the DUAL RS485 Board (Option 8) is selected, the query shall be modified to RS485 – 2 Baud.
    NOTE 4: If the DUAL RS485 Board (Option 8) is selected, the query shall be modified to RS485 – 2 Frame.

Note that Ethernet parameterization cannot be accomplished via the front panel interface and can only be accomplished via WIN ECP.

Modbus Plus Port Configuration [COM 3 on Selected Units] (DPU2000R Only)

Only the DPU2000R supports Modbus Plus. The DPU2000R recognizes if the communication card supports Modbus Plus. Only the Unit Address field within the communication port parameter screen is used via Modbus Plus. One should refer to Section 5 for further explanation of the Modbus Plus addressing scheme for accessing relay information.

TIME SYNCHRONIZATION SELECTION

All Modbus Cards in the DPU 2000R allow for time synchronization. The DPU 2000R with serial Modbus protocols allow for device Time Synchronization using IRIG B. DPU 2000R devices with Modbus TCP/IP Ethernet option cards installed allow for time synchronization using SNTP (Simple Network Time Protocol) using Ethernet.

IRIG B TIME SYNCHRONIZATION

Although not a protocol, IRIG B time synchronization is included on the communication cards within the DPU2000 and DPU2000R. The following section describes the theory, connection and configuration options present within the DPU2000 and DPU2000R/DPU1500R. IRIG B is available on all Modbus serial board options (Type 2 or 8). IRIG B is not available on Type”E” ethernet option boards.

IRIG B is a time code, which allows devices across the world to synchronize with a common time source to a resolution of one millisecond. IRIG B allows each device to synchronize with the frame received by an IRIG B receiver. ABB’s DPU/TPU/GPU2000/R relays (herein referred to as an IED) offer IRIG B time synchronization capabilities.

Figure 4-9 illustrates a typical IRIG B installation. An IRIG B time receiver accepts the RF signal and transforms it into a one second time synch frame. IEDs in the substation use the one second time synch frame to govern their internal clocks and event recorders.

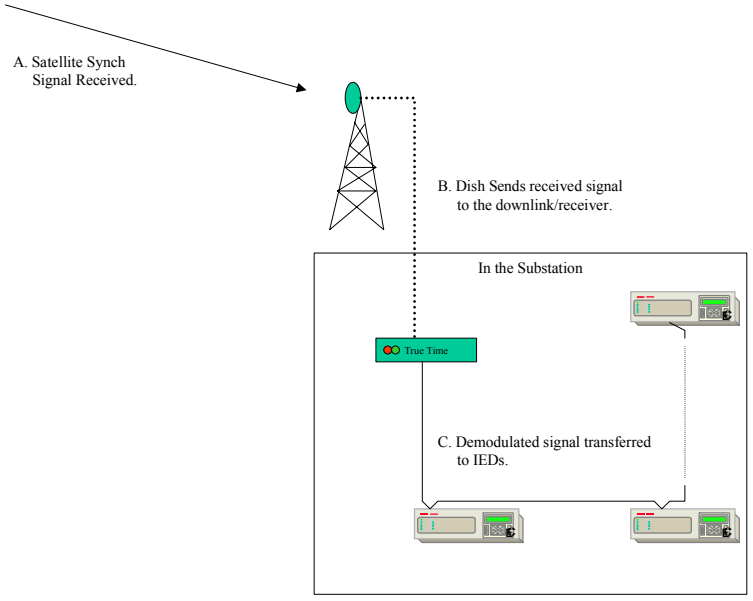


Figure 4-9. Typical IRIG B Architecture

IRIG B receivers/converters can format the IRIG B synchronization frames as a TTL-level pulse width, Manchester Encoded or Modulated Carrier Frequency signal. TTL-level signals are pulse DC with a voltage range of 0 to 5V. Modulated Carrier Frequency signals are pulse coded AM signals with modulation (tone bursts).

IRIG B is a general designation for time synchronization. There are many subsets to the IRIG B format. These were developed to provide functionality primarily for military applications dealing with missile and spacecraft tracking, telemetry systems, and data handling systems. IRIG B was embraced by the utility industry to answer a need to provide a sequence of events capability between a group of substations. Care must be exercised to match the device demodulating the signal from the satellite (downlink converter) with the IED's requiring specific IRIG B code formats.

DPU/TPU/GPU products support Pulse Width Code (X= 0), whereas, REL 3XX products having an IRIG B Poni Card support Pulse Width Code and Sine Wave Amplitude Modulated, and REL5XX products support Sine Wave Amplitude Modulated IRIG. If the IRIG signal supplied to the device is one in which the attached device cannot decode, the IED shall not synchronize with the signal and IED will not calculate time correctly.

The IRIG B time code has a one second time frame. Every frame contains 30 bits of Binary Coded Decimal time information representing seconds, minutes, hours, days and a second 17 bit straight binary time-of-day. The frame has internal time markers, which insure time-stamping accuracy to the millisecond. An eight millisecond frame reference marker appears during the first ten milliseconds of each frame. Another eight millisecond position identifier appears during the ninetieth millisecond of each one hundred millisecond period mark. The 30 bit Binary Coded Decimal time data occurs in the first one hundred millisecond of each 1 second frame. Optional control functions are sometimes encoded in the data stream. These functions control deletion commands and allow different data groupings within the synchronization strings. Decoding an IRIG B pulse is quite a complex undertaking. A typical 1 second time frame is illustrated in Figure 4-10. It is interesting to note that the year is not included within the IRIG B frame. If the Control Function frame (CF) or Straight Binary Time of Day frame (SBT) is not used, the bits defined within those fields are to be set as a string of zeroes and sent to the IED IRIG B receiver.

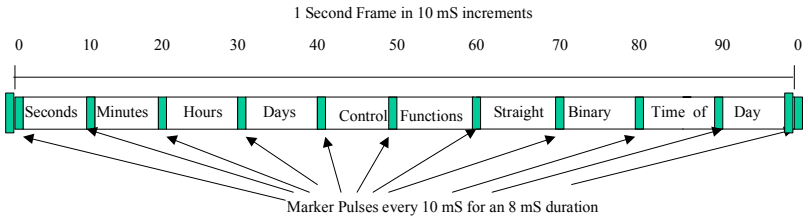


Figure 4-10. IRIG B Frame Construction

IRIG B is defined for code format sets identified by a three digit format number. Permissible format numbers for the IRIG B subsets are:

IRIG B XYZ Where:
The first field "X" identifies the encoding type of the IRIG B signal. DPU/TPU/GPU products support Pulse Width Code (X= 0), whereas, REL 3XX products having an IRIG B PONI Card support Pulse Width Code and Sine Wave Amplitude Modulated, and REL5XX products support Sine Wave Amplitude Modulated IRIG. Manchester Modulated code was added in IRIG Standard 200-98 Dated May 1998. It is not supported in the ABB protective relay products which are IRIG B capable.

The second field "Y" determines if a carrier is included within IRIG B Data format.

The third field "Z" determines if a combination of the BCD time/Control Function/Straight Binary Time is included within the IRIG B time frame. The inclusion or exclusion of any of the fields may cause errors in receivers not designed for the field's inclusion/ exclusion.

The following combinations may seem daunting, but only a subset of the listed formats are actually defined within the specification.

IF X =
0 = Pulse Width Code
1 = Sine Wave Amplitude Modulated
2 = Manchester Modulated Code

IF Y =
0 = No Carrier
2 =1Khz , 1mS
3 =10Khz, 0.1 mS
4 =100 Khz, 10 mS
5 =1Mhz, 1mS

IF Z=
0 =BCD Time,Control Function, Straight Binary Seconds
1 =Binary Coded Decimal Time, Control Function
2 =Binary Coded Decimal Time
3 =Binary Coded Decimal Time, Straight Binary Seconds

For the TPU/GPU/DPU2000/2000R products, IRIG B 000 and 002 formats are supported. Consult the IRIG B generator manufacturer so that the correct IRIG B code format is supplied to the receiving devices.

Hardware Configuration

IRIG B time synchronization is available for the products listed in Tables 4-6 and 4-7. Generally, three types of protective relays do not offer IRIG B, units without a communication card, units with Modbus Plus communication cards, and units with DNP 3.0 communication cards.

Each of these units uses the AUX COM port located at the rear of the relay to accept the TTL IRIG B signal. The DPU/TPU/GPU2000R and DPU1500R use Pins 63 and 64 to accept the IRIG B negative polarity and IRIG B positive polarity signals respectively, as illustrated in Figure 4-11. The DPU/TPU2000(R) and DPU1500R use pins 65 and 66 as illustrated in Figure 4-12.

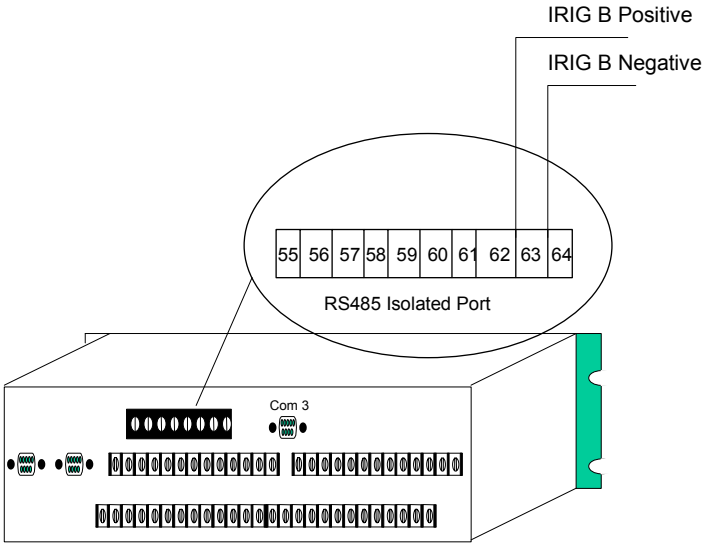


Figure 4-11. DPU/TPU/GPU2000R and DPU1500R IRIG B Connector Placement

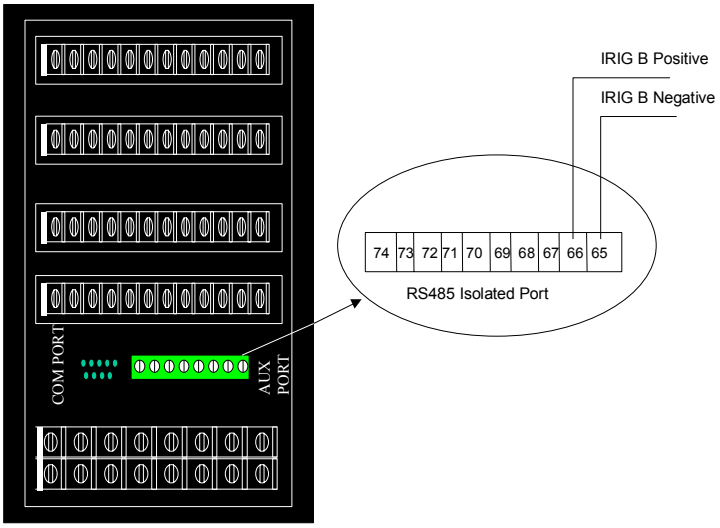


Figure 4-12. DPU/TPU2000 IRIG B Connector Placement

ABB's implementation of IRIG B requires that the signal be daisy-chained to each device. Each device in the IRIG B network presents a load to the IRIG B receiver/converter. Daisy-chained inputs are simple parallel circuits. A sample calculation is shown for the example illustrated in Figure 4-13.

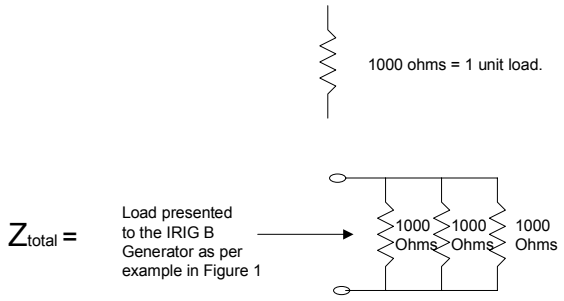
If the input impedance of each DPU/TPU/GPU2000/R is measured at its IRIG B connection, the impedance would be 1000 ohms. Each IRIG B input requires less than one mA to drive it.

Calculating the load impedance presented to the IRIG B source generator is illustrated in Figure 4-14. Each IED load on the IRIG B link presents a parallel impedance to the source. The general equation for parallel impedance is:

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \ldots$$

$$I_{Total} = I_1 + I_2 + I_3 + \ldots$$

This impedance equation simplifies to the form in Figure 4-14 when all IED loads are identical. If the loads are not identical, the general equation listed above must be used to calculate the load.



$Z_{total} = 1/(N*(1/1000))$ where N = number of DPU/GPU/TPU 2000/R Units.
$Z_{total} = 1/(3*(1/1000))$
$Z_{total} = 333.33$ ohms.

Thus the Source must be capable of driving a 333.33 ohm load.

Figure 4-13. Load Impedance Calculation

The calculated load impedance for the architecture presented in Figure 4-14 is 333.33 ohms. In this example the IRIG B receiver/converter must be capable of sending a three milli-amp TTL-level signal to a 333.33 ohm load. If the source is not matched with the load impedance, IRIG B will not operate correctly.

The cable recommended to connect the IRIG B devices shall have the following characteristics:

Capacitance: less than 40 pF per foot line to shield
Construction: 2-wire twisted pair shielded with PVC jacket

The maximum lead length of the entire relay is to be no more than 1000 feet. Cable types and vendors recommended and supported by ABB to interconnect the IRIG B devices are: The required IRIG signal voltage is 5V with a minimum required current drain of 4 mA per device added to the network.

BELDEN 9841, BELDEN YM29560, or equivalent

An example of the terminal to terminal daisychain interconnection of three units is illustrated in Figure 4-15.

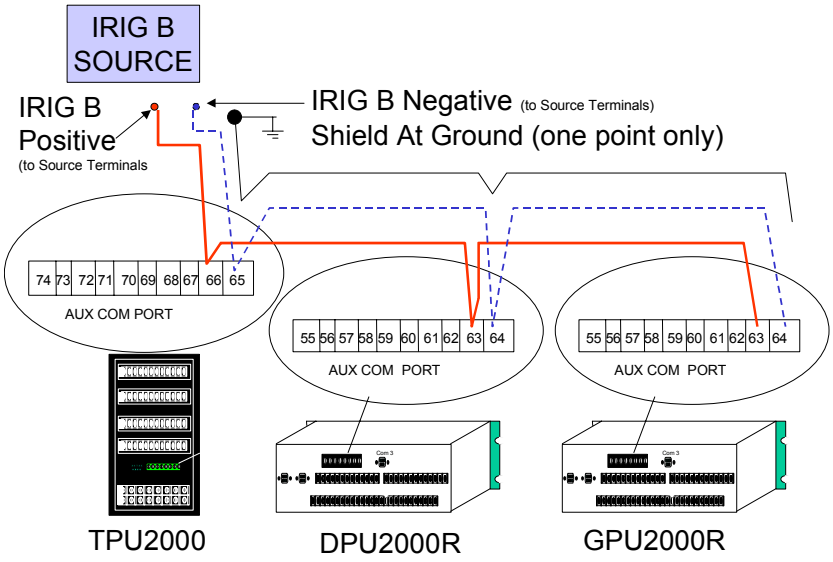


Figure 4-14. Pin to Pin Illustration of ABB Protective Daisychain Link for IRIG B

SIMPLE NETWORK TIME PROTOCOL

Simple Network Time Protocol (SNTP) is a UDP (User Datagram Protocol) for Ethernet allowing accurate and synchronized time across a TCP/IP (Ethernet) connection. SNTP is derived from a more complex NTP protocol (Network Time Protocol. SNTP differs from NTP in that some server-based time synchronization algorithms are not imbedded which would be more applicable for server applications. Simple Network Time Protocol can operate in a few ways:

- Client Server Basis, Unicast
- Peer To Peer Mode
- Broadcast/Multicast Basis (address 224.0.1.1 for SNTP and NTP)

SNTP is based upon the international time standard UTC (Universal Time Coordinated) which is an official and international standard for workd time. UTC is an evolved form of GMT (Greenwich Mean Time) which was a world standard. UTC is used because from a single universal time, one can convert the UTC to a local time by adding or subtracting hours based upon a local time zone.

SNTP is based upon RFC 2030 which replaced similar obsolete RFC's 1305, and 1769. SNTP uses UDP port 9000. If the DPU 2000R is updated with Version 1.20 COM ROM Firmware (Ethernet Option) and Version 6.00 CPU Version Firmware, SNTP time synchronization will be available.

Time Synchronization Parameterization Using WINECP Software Configuration

Physical interconnection of the devices is only one part of the procedure to allow Time Synchronization via IRIG B or SNTP. The ABB protective relays must be configured to enable Time Synchronization. The procedure follows:

1. Start WinECP for the appropriate device being configured.
2. Highlight the Change Settings Menu.
3. Highlight and Select the Communications Menu. Depending upon the DPU 2000R or 2000 IED, the screens depicted in Figure 4-15 or 4-16 will be depicted.

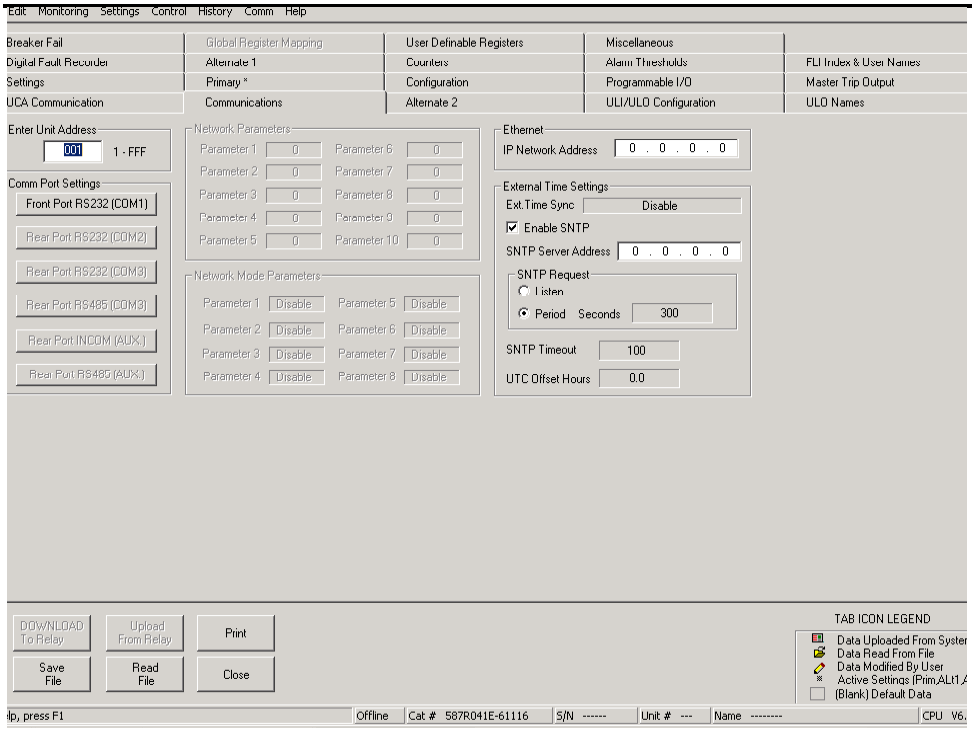


FIGURE 4-15: TIME SYNCHRONIZATION CONFIGURATION SCREEN (SNTP)

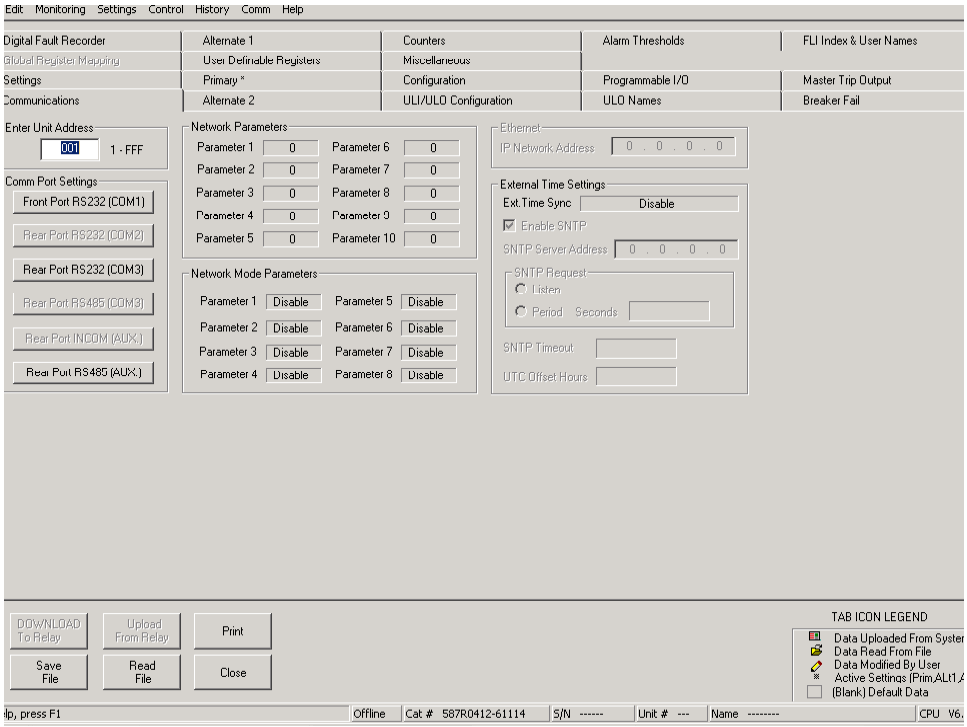


FIGURE 4-16: TIME SYNCHRONIZATION CONFIGURATION SCREEN (SERIAL PROTOCOLS)

If the protocol card supports Ethernet communication, SNTP is available. As per FIGURE 4-15, all protocol formats are available. A simple explanation of the configuration fields follows:

- EXTERNAL TIME SYNCH – This field applies for SNTP or Serial Protocols. The field ENABLES or DISABLES external Time Synchronization. If Time Synchronization is enabled, the selection from the pull-down menu also determines the reporting format and resolution of the internal time stamp. Table 4-5 describes the selectons and Figure 4-17 illustrates the pull down menu for selection.

- ENABLE SNTP – If this box is checked, SNTP is enabled and the fields illustrated in Figure 4-15 are enabled for configuration.
- SNTP Address – The SNTP host address is entered in this field. The field is available for configuration if the ENABLE SNTP box is checked and the DPU 2000R hardware is selected.
- SNTP Request - Two Radio Buttons are available for selection of SNTP update type. The selections are:
  - LISTEN – The DPU 2000R listens to the host and receives the time synchronization as the host sends it.
  - PERIOD: Seconds- The DPU 2000R requests Time Synchronization from the SNTP Host at specific time intervals. The time interval is specified in seconds.
- SNTP TIMEOUT – This value is defined in milliseconds in which the synchronized time packet must be received by the host server. If the time is not received in this time period, the DPU internal clock is not synchronized.
- UTC OFFSET HOURS: This value is enters in hours (format +/-XX.X) and is used to offset the received UTC time so that local time can be displayed

If the DPU only supports serial time synchronization via IRIG B, then only the selections listed in Table 4-5 will be available for configuration.

TIME SYNCHRONIZATION MEHTOD	WINECP TIME SYNCH VALUE	SNTP BOX	DESCRIPTION
NONE	DISABLE	Not Applicable	Internal DPU Clock Not Synchronized with External Source.
IRIG B	ENABLE –cc Or ENABLE- mmm	Unchecked	Internal DPU Clock Synchronized with External IRIG B signal. MMM – Reported in Milliseconds from Midnight with most significant bit set. CC- Reported in Deciseconds
Simple Network Time Protocol	ENABLE –cc Or ENABLE- mmm	Checked	Internal DPU Clock Synchronized with External IRIG B signal. MMM – Reported in Milliseconds from Midnight with most significant bit set. CC- Reported in Deciseconds
IRIG B	Enable mmm for MMI and COM.		Time synchronization reported in format of hours, minutes, seconds, milliseconds.

TABLE 4-5 : TIME SYNCHRONIZATION OPTIONS AND CONFIGURATION VALUES

Example: The following (IRIGB mmm) time is received from the DPU2000R:

82C6F096, where hour contains 82, minute contains C6 etc.

This would represent the following time in hours minutes seconds milliseconds in milliseconds from midnight:

12:56:13:150

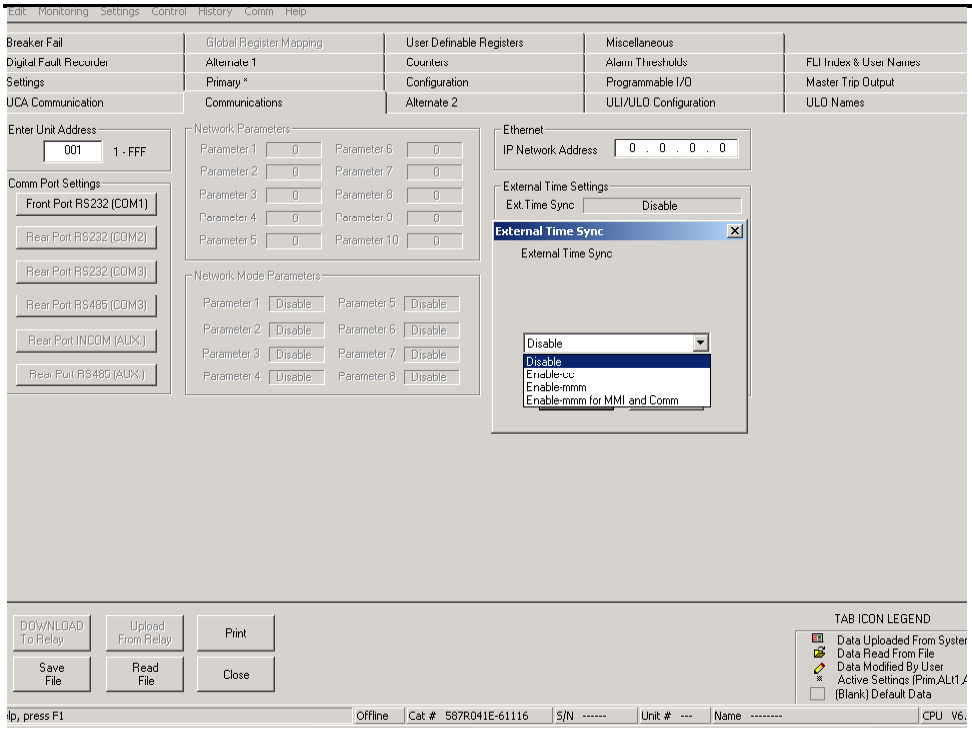


FIGURE 4-17: TIME SYNCHRONIZATION PARAMETERIZATION OPTIONS

Section 5 - Modbus

Modbus is capable of being transported over three different types of physical interfaces. The port emulation types are:

Serial
Modbus Plus
Ethernet TCP/IP

Modbus Serial is a traditional mode of providing protocol connectivity. There are two different emulations of Serial Modbus. The two emulations are, Modbus RTU or Modbus ASCII. All Modbus (Serial, Plus, or TCP/IP) contain the common command set. Only the protocol presentation differs between them. Section 5 contains an explanation of each protocol emulation theory so that the implementor may understand the differing technology and its impact on the configuration, performance, and capability of the selected emulation.

Serial Modbus is available in two emulation's, Modbus RTU and Modbus ASCII. Modbus RTU is a bit oriented protocol (normally referred to as Synchronous), and Modbus ASCII is a byte oriented protocol (normally referred to as Asynchronous). Both emulations support the same command set. **Networked nodes cannot communicate unless the same emulation of the Modbus protocol is interpreted.** This is an extremely important issue. The DPU2000, DPU2000R, and DPU1500Rsupports the Modbus ASCII and RTU protocol emulations.

Serial Modbus

Serial Modbus operates in the following fashion. A host device transmits a command, and one of the attached device(s) respond. Each device has a unique address assigned to it. Each device is configured for the same protocol emulation of Modbus. Figure 5-1 illustrates the polling sequence.

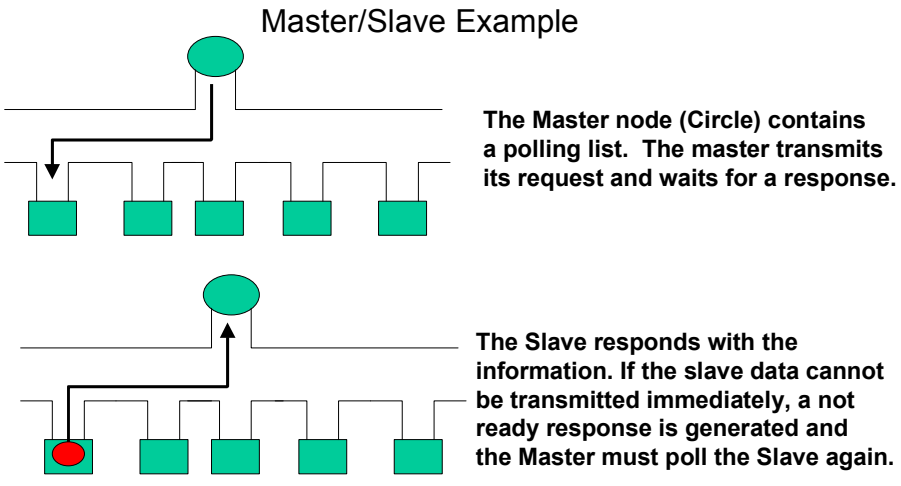


Figure 5-1. Modbus Polling Sequence

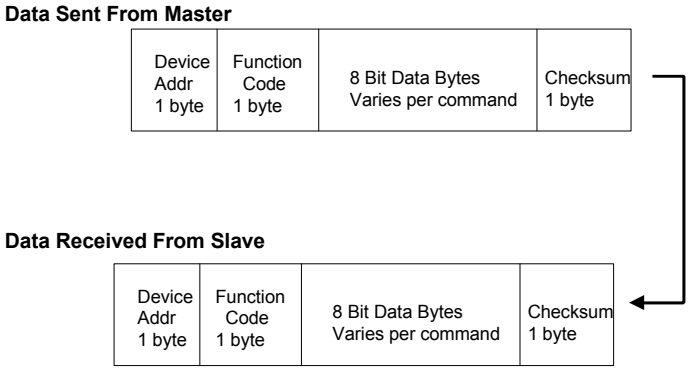
The DPU2000, DPU2000R, and DPU1500R are designed as Modbus slave emulation devices. That is, a device, a host, (illustrated in Figure 5-1) must be able to generate Master Requests in a Modbus format so that the slave, (DPU2000 or DPU2000R is able to receive the commands.

Modbus ASCII Emulation

An ASCII character is defined as 7 data bits. A character is represented as a number from 00 HEX to 7F HEX. Appendix B contains an ASCII character conversion chart. If a 0 is transmitted, it must be decoded to an ASCII representation to be interpreted by the receiving device. 0 decimal is 30 hex for an ASCII representation. The

frame format for Modbus is represented in Figure 5-2. The device address, function code and checksum is part of the transmitted frame. The Checksum is a Longitudinal Redundancy Check (LRC). Its calculation shall be described later in this guide.

The generic Modbus Frame is analyzed in Figure 5-3. The start of an ASCII frame is always a colon (: = 3A HEX) and a termination of the command is a line feed and carriage return (If cr = 0D 0A). The format is the same for the host transmitting the frame and the slave node responding to the host's transmission. The device address is imbedded within the frame along with the Modbus command function code. A checksum is appended to the entire command. The checksum is a Longitudinal Redundancy Checksum. The LRC checksum combined with parity and internal field length detection determination, provides good security in detection of data packet errors. LRC is easily calculated by many devices which results in ASCII emulation's popularity.



(Device Address = 0 (Null Command), 1 - 247, 255 (Broadcast)

Figure 5-2. Modbus ASCII Transmitted and Received Frame Formats

START	ADDRESS	FUNCTION	DATA	LRC	END
1 Char :	2 Chars	2 Chars	N Chars	2 Chars	2 Chars CR LF

Figure 5-3. Modbus ASCII Frame Format

The Modbus characters are encoded with a variety of frame sizes. An analysis of each frame is illustrated in Figure 5-4. When selecting a common frame size, (as explained in the configuration setup examples), parity, word length, and stop bits are selected to form a 10 bit data frame (1 start bit + 7 data bits + 1 stop bit + 1 Parity bit "OR" 1 start bit + 2 stop bits + 7 data bits + NO Parity = 10 bits per frame). It is important to note this distinction since if DPU2000, DPU2000R, and DPU1500R device attachment is to occur through a device, the device must support 10 bit asynchronous data framing.

Least Significant Bit ……Most Significant Bit

START	1	2	3	4	5	6	7	PARITY	STOP

With Parity Checking

START	1	2	3	4	5	6	7	STOP	STOP

Without Parity Checking

Figure 5-4. Modbus ASCII Frame Analysis

The DPU2000, DPU2000R, and DPU1500R offers a variety of frame sizes. If the frame size, 8N1 is selected (8 Data Bits, No Parity, 1 Stop Bit), then an additional stop bit is inserted. The frame format follows that of Figure 5-4 “Without Parity Checking”. However, when using ASCII protocol with many other devices, the data is limited to 7 bits. Selection of 8 bits for the data frame will automatically require that the device receive/transmit RTU mode. The ABB DPU2000, DPU2000R, or DPU1500R does not allow for this override, however several programmable logic controller manufacturers allow for this.

The receiving device determines that a frame is on the network by sensing the first character (: colon) and then determining that the message address is the same as that assigned to itself. If the Modbus device does not receive a carriage return line feed (lf cf 0A 0D) within an appreciable amount of time, the host will timeout. The length of characters in the message determines Timeout. Modbus ASCII will timeout is the time delay between each character exceeds 1 second delay between each character’s transmission. If 100 characters are required to transmit a complete Modbus ASCII frame, then the timeout for the message could be in excess of 100 seconds for that specific exchange.

Modbus RTU Emulation

In contrast to the ASCII representation, Modbus allows for no encoding of the transmitted or received data message. If a data byte of 00 (zero zero) is sent to an IED from a Host, the data would be sent as a single byte of data (binary 0000 0000). If data would be sent as an ASCII data string the data would be composed of the encoded ASCII string 30 30 hex (binary 0011 0000 0011 0000). The Modbus RTU emulation is twice as efficient as Modbus ASCII mode.

START	ADDRESS	FUNCTION	DATA	LRC	END
4 Char Delays	8 Bits	8 Bits	N * 8 bits	16 Bits	4 Char Delays

Figure 5-5. Modbus RTU Format

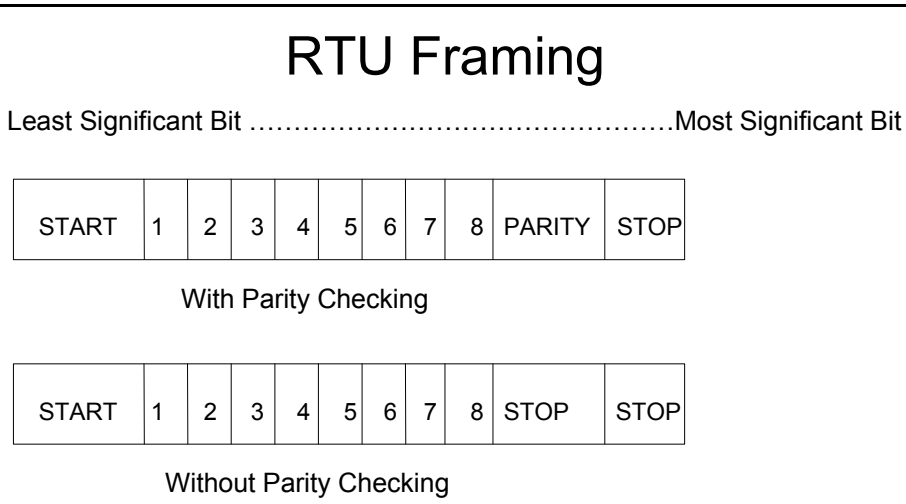


Figure 5-6. RTU Frame Format

Figures 5-5 and 5-6 illustrate the format of the Modbus RTU emulation. An analysis of each frame is illustrated in Figure 5-6. When selecting a common frame size, (as explained in the configuration setup examples), parity, word length, and stop bits are selected to form a 11 bit data frame (1 start bit + 8 data bits + 1 stop bit + 1 Parity bit "OR" 1 start bit + 2 stop bits + 8 data bits + NO Parity = 11 bits per frame). It is important to note this distinction since if DPU2000, DPU2000R, and DPU1500R device attachment is to occur through a device, the device must support 11 bit asynchronous data framing.

Modbus ASCII protocol synchronizes host to IED messaging through monitoring the leading character (: colon). Modbus RTU synchronizes the host to IED messaging through time delays. Modbus RTU emulation. Modbus RTU timeout depends on the following rules.

- If delay between transmissions is < 3.5 Character Times, the message is received.
- If delay < 3.5 character times, receiving device appends characters to last message.
- If delay is sensed > 1.5 message times, receiving device flushes the buffer. Next character is new message.

The Modbus RTU emulation senses timeouts quicker than the Modbus ASCII emulation. The Modbus RTU emulation also uses a CRC –16 checksum in contrast to the Modbus ASCII using a LRC (Longitudinal Redundancy Check). The CRC –16 is a much more robust checksum. With parity, internal protocol message length field checks and the CRC-16, the error detection is exceptional.

> **IMPLEMENTATION TIP-**When commissioning a Modbus system, it is always advisable to connect a communication analyzer in-line with the host. It is always uncertain whether the host is sending the command correctly. Within the DPU2000 and DPU2000R, an incorrect address request will always generate an exception response from the relay. If an exception response is generated, many host devices will not display the Modbus exception response generated by the unit. A communication analyzer allows for rapid troubleshooting of a malfunctioning network connection.

Modbus Plus (Available on the DPU2000R Only)

Modbus capabilities were expanded in a significant way during the late 1980's. The base command set was not changed from the Modbus protocol, however, the protocol access method was modified. The limitations of Modbus exposed themselves in a few areas:

- The throughput was dependent upon the physical interface (RS232 and 485) which limited the speed of data transfer.
- The Modbus protocol did not efficiently manage its bandwidth. Exorbitant amounts of time could be spent waiting for the slave device to respond with data or timeout.
- The Modbus protocol only allowed connection of a single host (or multiple hosts with the addition of hardware multiplexers) to up to 247 IEDs.

The originator of the protocol Modicon AEG, had devised a way to use the Modbus protocol and present it to the attached nodes to eliminate the deficiencies found in large Modbus installations.

Modbus Plus was developed using a proprietary physical interface allowing communication over a twisted shielded pair medium. The baud rate of the network was fixed at 1 megabaud. If this had been the only change from Modbus to Modbus Plus, the network's introduction would not have been significant. The Modbus repackaging into a Modbus Plus format afforded the following significant benefits:

- Up to 34 simultaneous conversations may occur on a network.
- Each device on a Modbus network is capable of being a host.
- Each device may broadcast a data, which is received by all other nodes on the network.
- Node to node network throughput time may be deterministically calculated.

The Modbus Plus interface was afforded though the manufacturer entering into a "MODCONNECT AGREEMENT" allowing sharing of technology between the IED implementers and Modicon AEG. The IED implementers received Modbus Plus chipsets and technology allowing network implementation. Once the implementation was completed, a certification process ensued and upon the IED's successful test of the implementation, certification was bestowed upon the IED.

Modbus Plus Theory of Operation

Modbus Plus is a token passing network based upon an HDLC like protocol implementation. The frame structure of the protocol is illustrated in Figure 1-8. As illustrated, the Modbus command structure is imbedded in the Modbus Plus structure. Thus, all Modbus commands are used for Modbus Plus. The manufacturer of the protocol supplies drivers allowing DOS, Windows [3.1, 95 or 98] to communicate with the Modbus Plus hardware. The implicit understanding of Modbus Plus protocol frames is not needed by the operator. This discussion is meant to inform the reader of the commonality between Modbus and Modbus Plus.

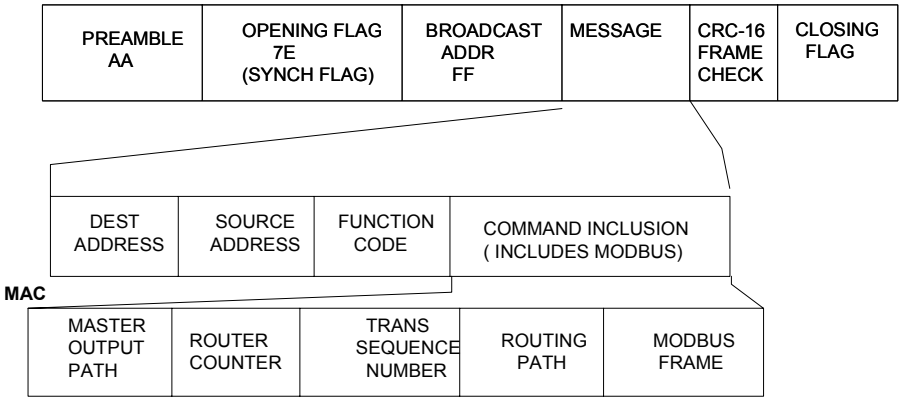
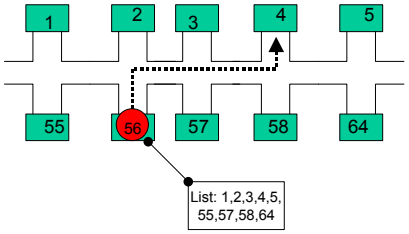


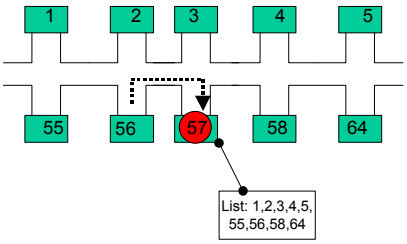
Figure 5-7. Modbus Plus Message Frame Structure

Modbus Plus is a “token passing” network in that upon startup, a token is generated. The node with the token acts as a host device. The node holds a token for a period of time and passes the token to the next node on the network. The token rotation scheme is described in Figures 5-8a through 5-8c.

PEER TO PEER EXAMPLE

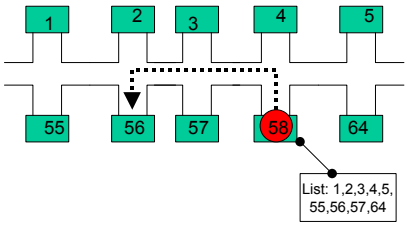


Each node on the Network has a list of all other node addresses on the network. Upon Startup a token is generated. The node in possession of the token (Red Spot) may transmit.

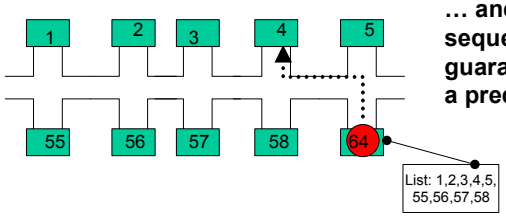


When the node has finished transmitting, it passes the token to the next node. This node may, for instance, may not wish to transmit.. The token will be passed to the next node in the list before its time has expired.

Figure 5-8a. Modbus Plus Token Rotation Explanation

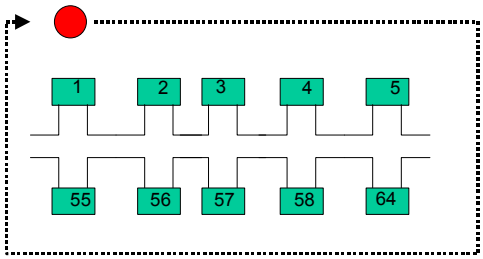


If so the token is passed to the next node, which sends a message...



… and so on in a fixed sequence so that every node is guaranteed network access within a predetermined time slice.

Figure 5-8b. Modbus Plus Token Rotation Explanation



When the token has been passed through all nodes on the network, one token rotation has occurred. This is a measurable and deterministic time slice.

Figure 5-8c. Modbus Plus Token Rotation Explanation

Modbus Plus allows interconnection of up to 5 networks of devices. Each Modbus Plus network may be comprised of up to 64 nodes of IED's distributed over 6000 feet of cable. Physical interface cabling is discussed in Section 3 of this document. Each network is interconnected with a bridge device. The Modbus Plus Bridge is obtainable through Schneider Electric or Square D Company. The Modbus Plus Bridge is an addressable device with each port being assigned an address particular to the network to which it is attached. Figure 5-9 illustrates the network configuration.

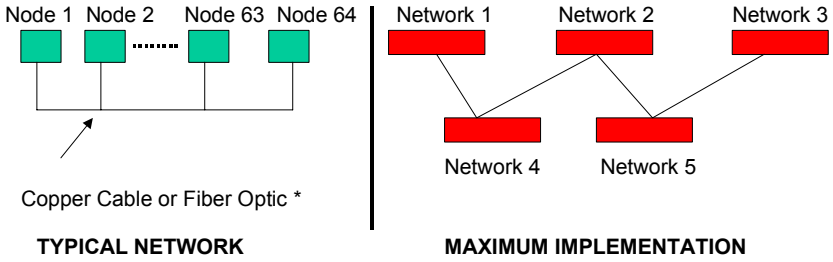


Figure 5-9. Modbus Plus Network Topology

Understanding the concept of Modbus Plus Paths is critical for assignment of a node address and calculating network throughput. Figure 5-10 illustrates the maximum path implementation for Modbus Plus. The maximum path implementation for a Modbus Plus Node is shown in Figure 5-10.

- 8 Program Master Paths (Programmable Logic Controller Only)
  - Used by Programmable Logic controllers to Transfer Master Data From Node to Node (Unavailable to Modconnect Partner IED's)
- 8 Program Slave Paths (Programmable Logic Controller Only)
  - Used by Programmable Logic controller to Receive Master Data From Node to Node (Unavailable to Modconnect Partner IED's)
- 8 Data Slave Paths
  - Used by Nodes to Receive Slave Data (Available to Modconnect Partner IED's)
- 8 Data Master Paths
  - Used by Slave Nodes to Transmit Slave Data to other Nodes (Available to Modconnect Partner IED's)
- 1 Global Input Data Path
  - Global Data Path to Receive Global Data from Other Modbus Plus Nodes (Available to Modconnect Partner IED's)
- 1 Global Output Data Path
  - Global Data Path to allow the node to Transmit Global Data to other Modbus Plus Nodes (Available to Modconnect Partner IED's)

Global Data is a Modbus Plus capability allowing each node to place up to 32 – 16 bit words of data on the network. Each word of Global Data is retrievable by any node on that segment of the Modbus Plus Network.

GLOBAL DATA IS NOT RETRIEVABLE THROUGH A MODBUS PLUS BRIDGE OR BRIDGE MULTIPLEXER DEVICE.

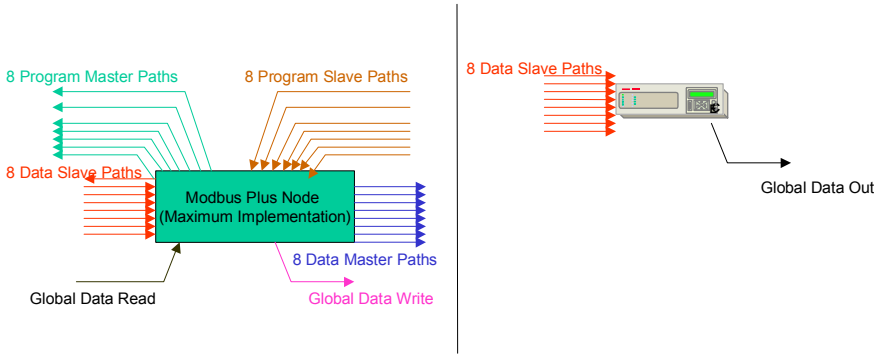


Figure 5-10. Modbus Plus Path Designation

The DPU2000R implementation of Modbus Plus shows the data path implementation. The DPU2000R Modbus Plus implementation allows:

- The DPU2000R to receive information requests from a device acting as a host along one of its 8 data slave paths.
- The DPU2000R to place up to 32 registers of data on the Global Out Data Path. The data sent on the Global Out Path is configurable through ECP or WinECP. The Configuration Method is described in Section 4.

The DPU2000R implements Modbus PLUS as a HOST device. The Modbus Plus address assignment required depends upon the understanding of the path assignment discussion. Figure 5-11 illustrates the addressing required when a device (such as a programmable logic controller or a host device with a Modbus Plus SA 85 card) must access a DPU2000R via Modbus Plus. An application note is included in Appendix C describing the process for Programmable Logic Controller attachment with a DPU2000R.

As per Figure 5-11, if a host device X is to request data from an ABB DPU2000R, the node address (configured via the front panel interface, ECP, or WinECP) is the first address node entry in the data path for the address Routing Path 1. In the case with the nodes sharing the same network, the Routing Path 2 entry is the slave path address communicated with. The Route address for the slave path is 1 through 8.

Routing Addr 1	*Routing Addr 2*	*Routing Addr 3*	*Routing Addr 4*	*Routing Addr 5*
5	1	0	0	0

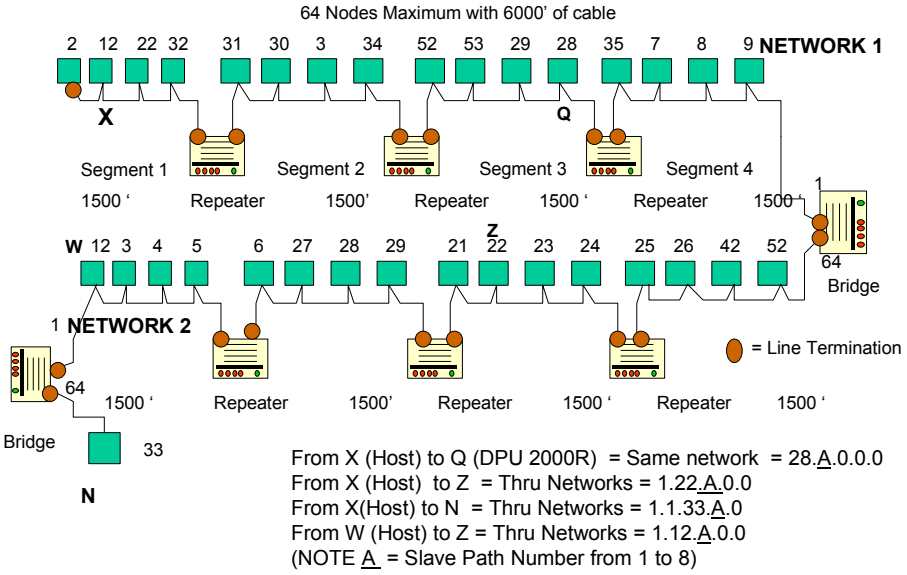


Figure 5-11. Modbus Plus Addressing Example

If a node had to cross a network boundary through a Bridge, the examples illustrate how node access addressing would be affected.

Modbus and Modbus Plus General Notes

Modbus is an exceptional protocol for bridging a majority of vendor devices to communicate to each other. The generation of each protocol, throughput, robust capabilities and troubleshooting techniques shall be covered in later sections. The understanding of each of these principles shall aid the implement in exploiting the capabilities within their own automation system.

Modbus ASCII, Modbus RTU, and Modbus Plus have the following capacities implemented within the DPU2000, DPU2000R and DPU1500R.

- 01 - Read 0X Coil Status
- 02 - Read 1X Contact Status
- 03 - Read 4X Holding Registers
- 16 - Write 4X Holding Registers
- 08 - Diagnostics
- 23 - Write 4X and Read 4X Holding Registers
- 20 - Read 6X Extended Registers
- 21 - Write 6X Extended Registers

The DPU2000 and DPU2000R emulates a slave device. Any other Modbus command sent to the DPU2000 and DPU2000R shall result in a Modbus exception code being sent to the transmitting device. The following sections will further describe the Modbus functionality within the DPU2000 and DPU2000R.

IMPLEMENTATION TIP-Although the DPU2000 and DPU2000R allows configuration of Modbus for a Frame of N-8-1, some implementations will interpret this emulation of Modbus to be RTU Mode. The DPU2000 and DPU2000R does not support this mode. It is advisable to contact the manufacturer of the host and host software to determine the interpretation of the command string. For example, the Modicon XMIT and COMM BLOCK allowing the PLC to emulate a host device only allows block frame size designation of 7 data bits.

TCP/IP MODBUS

Modbus TCP/IP is based on the same serial Modbus command set as the serial implementations. The TCP/IP implementation follows the standards set in the RFC 791 Internet protocol specified by DARPA.

The DPU 2000R TCP/IP implementation sets aside 4 sockets for Modbus TCP/IP and 1 socket available for FTP protocol. If the Ethernet implementation includes UCA (as in the Type E-XXXXX6 board), then 1 additional socket is set aside for UCA.

A socket allocation allows the Ethernet board to have multiple sessions. Therefore if 4 sockets are allocated, then up to four devices may simultaneously request information from the DPU. The DPU is a Server node in that it receives a request from the Client to supply information. The DPU responds to the request.

The DPU 2000R uses the allocated Port number of 502 for Modbus IP protocol. The implementation of Modbus has been defined for Ethernet 802.3.

The Modbus TCP/IP packet is comprised of several Layers, the Ethernet Preamble, Ethernet Header, TCP Header, Interleaved Protocol Packet. Figure 5-A illustrates the packet structure. The Modbus header is defined as the

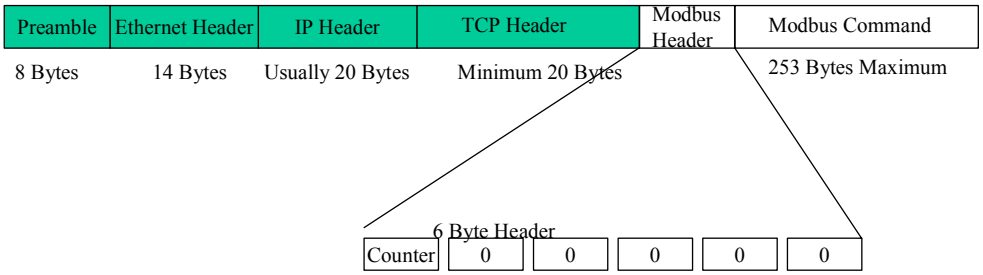


FIGURE 5-A : Modbus TCP/IP PACKET

The Modbus command set is explained for each data element. Section 6 explains the data set for each. As illustrated, the Modbus command set is imbedded within the Ethernet packet. The ABB DPU 2000R is designed with high data throughput in mind and can process the command requests quickly for maximum data throughput

Section 6 - Modbus/Modbus Plus Register Map

0X Discrete Coils

Discrete Modbus Coil status is available via a function 01 request via Modbus. Figure 6-1 illustrates a typical command sequence. The Host polls the DPU2000/DPU2000R/DPU1500R for the Data. The DPU2000/2000R/1500R receives the request and responds with the expected data. The Host then interprets the command response, checks the checksum (LRC if ASCII, CRC 16 if RTU mode)and then displays the interpreted data. Additional information is available in Modicon's protocol manual references listed at the beginning of this document.

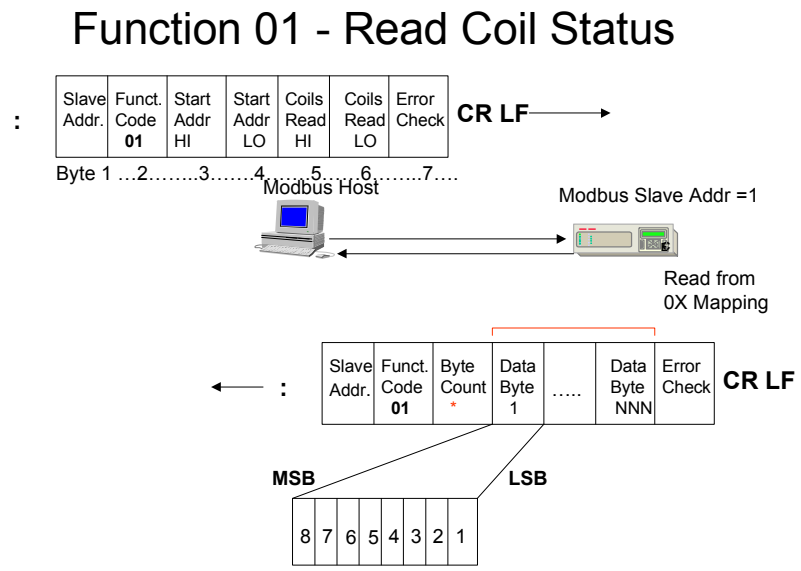


Figure 6-1. Modbus Protocol Function 01 Frame Format

Function Code 1 (Read Coil Status) – Read Only Data

The 0X read command allows for access of Logical and Physical Input data. The information listed in Tables 6-1, 6-2, and 6-3 is that which is reported in real time. In other words, if the bits are polled as per the table, the status of each data bit is reported at the time the data is requested. If the data is momentary in nature, then access of status is dependent upon reading the information at the time the function or signal is present.

Table 6-1 lists the Logical Output Single Bit Data. The data listed within the table includes real time status bits, which may be briefly reported status bits. In other words, they follow the real time status of the point. Other points reported in the table are latched.

A Latched point (sometimes referred to as Sealed In Output Point). These points stay energized until they are reset by a group control function. The function is reset via the method described in the 4X control explanation and an example is shown in Figure 6-2.

Momentary data reporting is available at the present time. Some bit statuses are brief in reporting nature. Modbus and Modbus Plus do not have a method of timestamping events, nor is there a "protocol defined" method to ensure that an event is not lost. ABB incorporates a method called "Momentary Bit Status Reporting" allowing a host to poll a protective device at any time and ensure that a contact change notification occurs. The method shall be explained later in this document.

If data is requested from memory addresses not defined within this document, a Modbus Exception Code shall be generated Figures 6-2 and 6-3 illustrate a simple example of a host requesting data from a DPU2000R relay where Physical Relay Coil Status is requested of the DPU2000/DPU2000R/DPU1500R. The example illustrates

that data is requested in the Modbus RTU frame format illustrated in Figure 6-2. The individual status bits are parsed by the host as illustrated in Figure 6-3.

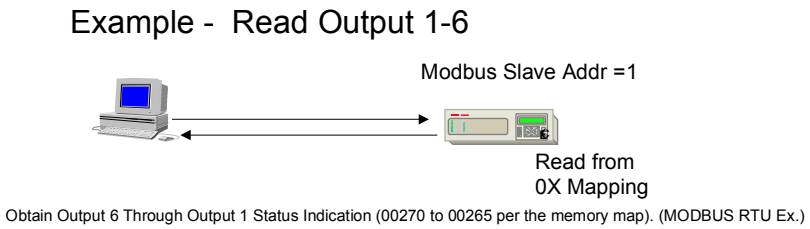


Figure 6-2. Example Transaction Request for Eight Physical Output Coils

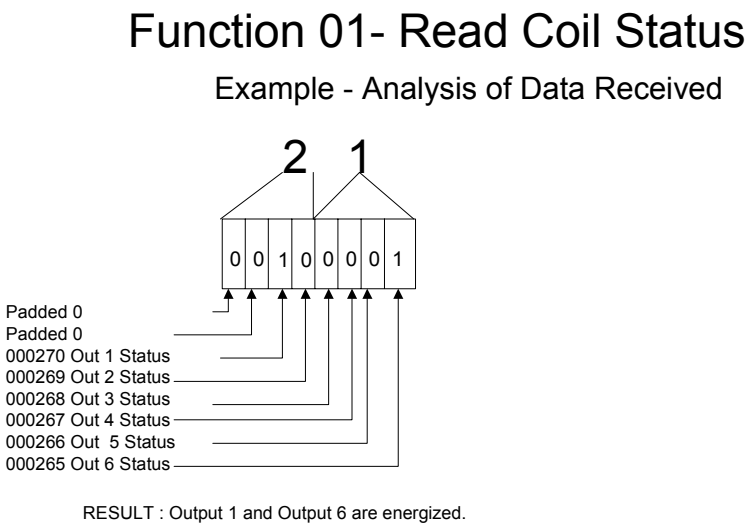


Figure 6-3. Example of Raw Data Decode

Modbus 0X Implementation Features

Modbus is a protocol often used in the industrial sector. The protocol was developed to operate between hosts and programmable logic controllers. The controlling device, in most cases was a PLC (Programmable Logic Controller), which had the capability of detecting and storing fast events and indicating to the polling device that an event had occurred. The change detect feature was not part of the protocol, but part of the monitoring device (namely the Modicon PLC).

Utility devices require that no event is to be missed in the field IED. ABB has incorporated two methods in which a device is notified that events have occurred in the field IED between host polls. The two methods employed for 0x data (Modbus Function Code 01) are:

- MOMENTARY CHANGE DETECT
- LATCHED ELEMENT RETENTION

MOMENTARY CHANGE DETECT and LATCHED ELEMENT RETENTION are independent of the protocol. These ABB innovations allow Modbus protocol to address and satisfy the concerns common to a utility installation. The two functionality's are those in excess of the real time status access that Modbus function code 01 affords.

Momentary Change Detect status is incorporated using two bits to indicate present status and momentary indication status. The odd bit is the status bit and the even bit is the momentary bit. The status bit indicates the present state of the element accessed. The momentary bit indicates element transitioning more than once between IED reads. The momentary bit is set to a "1" if the element has transitioned more than once. The bit is reset upon a host access. Addresses 00513 through 01056 are allocated for momentary change bit detect status detection. NOTE: MOMENTARY BITS MUST BE READ IN PAIRS.

An example of momentary change detect is illustrated in Figure 6-4. Suppose a host device monitors DPU2000/DPU2000R/DPU1500R physical output bit 1. Figure 6-4 illustrates the physical output transitions of output 1. At each output rising edge/falling edge transition, the status of the Modbus coil 0x addresses are listed. The dotted line arrows indicate the poll received by the DPU2000/DPU2000R/DPU1500R and the state of both the status bit and the momentary indication bit. Note that the even bit (momentary change detect) resets itself to a zero state after a host read.

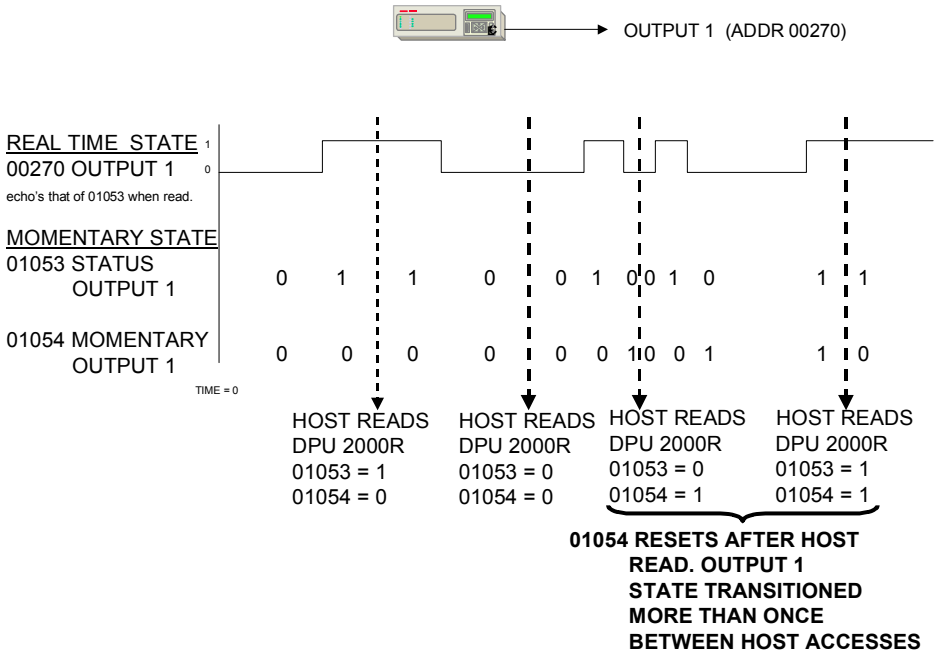


Figure 6-4. Momentary Change Detect Example

Latched Element Retention is a method by which when an element has transitions from a 0 (inactive), to a 1 (active) status, the element is set to "1". The element stays at a status of 1 until the operator executes a reset sequence. The reset of latched points may occur:

- The operator may depress the "SYSTEM RESET" pushbutton at the faceplate of the DPU2000R
- Depress the "C", "E", and "↑" (UP ARROW), keys simultaneously on the membrane keypad (DPU2000R and DPU2000)
- Initiate a supervisory bit reset sequence for the individual bits requiring reset. Reference Section 11 of this guide for a detailed explanation of the reset procedure.

Figure 6-5 illustrates the operation of a latched bit sequence. The LATCHED elements are denoted with the symbol (L) within the tables. Example latched elements are addresses 0050 through 0069 in Table 6-1 of this document.

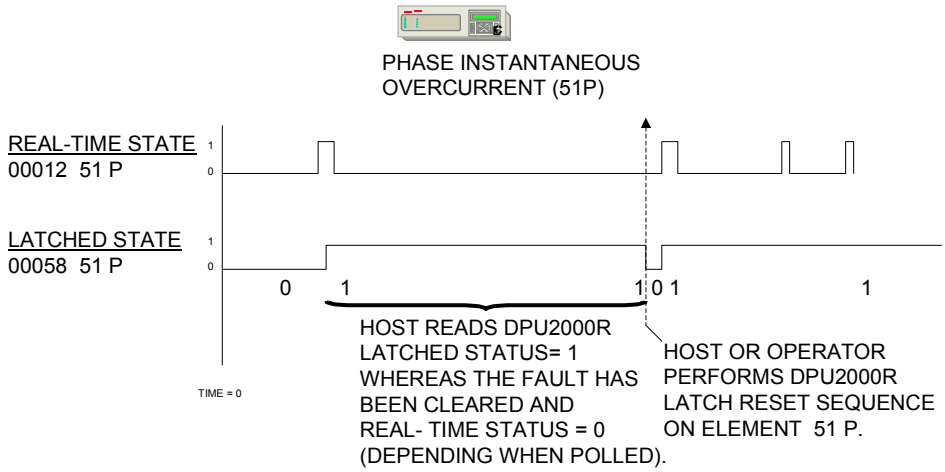


Figure 6-5. Latched Element Status Example

Logical Output Block (Single Bit Data) – 177 Discrete Coils (177 Elements Defined)

Relay Element Status as described in Table 6-1. Additional coil status has been added in the latest version of DPU2000/DPU2000R/DPU1500R executive firmware. Consult the symbol keys in the table for revision level feature inclusion.

The status information reported in Table 6-1 is reported as real time status bits. For example if the breaker is the process of tripping the status of 0009 and 00010 shall report the breaker action. If the status of 00009 or 00010 is polled after the trip or close has been completed, the status of these bits shall report a status of 0.

> **IMPLEMENTATION TIP-** If breaker status is to be required after the event occurs, it is advisable to read the seal-in bits described in Table 6-5 (Address 00255 and 00256). Seal-in bit capability is available in DPU2000/DPU2000R/DPU1500R Firmware Version 1.70. If one has an earlier version of DPU2000/DPU2000R/DPU1500R, Address 10006 and 10007 could be polled to monitor the actual state of 52a and 52b. The polled state may then be saved and compared to the earlier values to determine whether a trip or close has occurred between device polls.

Table 6-1. Logical Output Modbus Address Map Definition

	Register Address	Item	Description
	00001	TRIP	Breaker is Tripping
	00002	CLOSE	Breaker is Closing
	00003	ALARM	DPU is in Alarm
	00004	27	Undervoltage Trip
	00005	46	Negative Sequence Overcurrent Trip
	00006	50P1	Phase Instantaneous Overcurrent Trip
	00007	50N1	Neutral Instantaneous Overcurrent Trip
	00008	50P2	Phase Instantaneous Overcurrent Trip
	00009	50N2	Neutral Instantaneous Overcurrent Trip
	00010	50P3	Phase Instantaneous Overcurrent Trip
	00011	50N3	Neutral Instantaneous Overcurrent Trip
	00012	51P	Phase Time Overcurrent Enabled
	00013	51N	Neutral Time Overcurrent Enabled
1	00014	59	Overvoltage Trip
1	00015	67P	Direct Overcurrent Trip Positive Sequence

	Register Address	Item	Description
1	00016	67N	Direct Overcurrent Trip Negative Sequence
	00017	81S-1	Frequency Shed (1st Stage)
	00018	81R-1	Frequency Restore (1st Stage)
	00019	PATA	Phase A Target Alarm Energized
	00020	PATB	Phase B Target Alarm Energized
	00021	PATC	Phase C Target Alarm Energized
	00022	TCFA	Trip Coil Failure Alarm Energized
	00023	TCC	Tap Changer Cutoff Energized
	00024	79DA	Reclosing Disabled Alarm Energized
	00025	PUA	Pick Up Alarm
	00026	79LOA	Recloser Lock Out Alarm Energized
	00027	BFA	Breaker Fail Alarm Energized
	00028	PDA	Physical Demand Current Alarm Energized
	00029	NDA	Neutral Demand Current Alarm Energized
	00030	BFUA	Blown Fuse Alarm Energized
	00031	KSI	Kiloamperes Symmetrical Inverted Alarm Energized
	00032	79CA1	Recloser Counter Alarm 1 Energized
	00033	HPFA	High Power Factor Alarm Energized
	00034	LPFA	Low Power Factor Alarm Energized
	00035	OCTC	Overcurrent Trip Counter Alarm Energized
	00036	50-1D	1st Instantaneous Overcurrent Distance Alarm Energized
	00037	50-2D	2nd Instantaneous Overcurrent Distance Alarm Energized
	00038	STC	Settings Table Change Alarm Energized
	00039	ZSC	Zone Sequence Control Alarm Energized
	00040	PH3-D	Phase Overcurrent Disabled Alarm Energized
	00041	GRD-D	Ground Overcurrent Disabled Alarm Energized
1	00042	32 PA	(67P) Positive Sequence Direct Overcurrent Trip Alarm Energized
1	00043	32 PN	(67N) Negative Sequence Direct Overcurrent Trip Alarm Energized
	00044	27-3P	Three Phase Undervoltage Trip Energized
	00045	VARDA	3 Phase KVAR Demand Alarm Energized
	00046	79CA2	Recloser Counter Alarm 2 Energized
	00047	TRIP A	Single Phase Trip (Phase A)
	00048	TRIP B	Single Phase Trip (Phase B)
	00049	TRIP C	Single Phase Trip (Phase C)
(L)	00050	27	Undervoltage Trip
(L)	00051	46	Negative Sequence Overcurrent Trip
(L)	00052	50P1	Phase Instantaneous Overcurrent Trip
(L)	00053	50N1	Neutral Instantaneous Overcurrent Trip
(L)	00054	50P2	Phase Instantaneous Overcurrent Trip
(L)	00055	50N2	Neutral Instantaneous Overcurrent Trip
(L)	00056	50P3	Phase Instantaneous Overcurrent Trip
(L)	00057	50N3	Neutral Instantaneous Overcurrent Trip
(L)	00058	51P	Phase Time Overcurrent Enabled
(L)	00059	51N	Neutral Time Overcurrent Enabled
(L) 1	00060	59	Overvoltage Trip
(L) 1	00061	67P	Direct Overcurrent Trip Positive Sequence
(L) 1	00062	67N	Direct Overcurrent Trip Negative Sequence
(L) 1	00063	81S-1	Frequency Shed (1st Stage)
(L) 1	00064	81R-1	Frequency Restore (1st Stage)
(L) 1	00065	81O-1	Overfrequency (1st Stage)
(L)	00066	27-3P	Three Phase Undervoltage Trip Energized
(L)	00067	TRIP A	Single Phase Trip (Phase A)
(L)	00068	TRIP B	Single Phase Trip (Phase B)

	Register Address	Item	Description
(L)	00069	TRIP C	Single Phase Trip (Phase C)
1	00070	ULO 1	User Logical Output 1
1	00071	ULO 2	User Logical Output 2
1	00072	ULO 3	User Logical Output 3
1	00073	ULO 4	User Logical Output 4
1	00074	ULO 5	User Logical Output 5
1	00075	ULO 6	User Logical Output 6
1	00076	ULO 7	User Logical Output 7
1	00077	ULO 8	User Logical Output 8
1	00078	ULO 9	User Logical Output 9
	00079	PVARA	Positive 3 Phase KVAR Alarm Energized
	00080	NVARA	Negative 3 Phase KVAR Alarm Energized
	00081	LOADA	Load Current Alarm Energized
1	00082	81O-1	Overfrequency (1st Stage)
1	00083	81O-2	Overfrequency (2nd Stage)
1	00084	81S-2	Frequency Shed (2nd Stage)
1	00085	81R-2	Frequency Restore (2nd Stage)
1	00086	81O-2	Overfrequency (2nd Stage)
1	00087	81S-2	Frequency Shed (2nd Stage)
1	00088	81R-2	Frequency Restore (2nd Stage)
	00089	CLTA	Cold Load Timer Alarm
	00090	Watt 1	Positive Watt Alarm 1
	00091	Watt 2	Positive Watt Alarm 2
(L)	00092	79CA 1	Reclose Counter Alarm 1
(L)	00093	79CA 2	Reclose Counter Alarm 2
(L)	00094	SEF	Sensitive Earth Fault
*	00095	SEF Alarm	Sensitive Earth Fault Alarm Energized
*	00096	PUA w/o SEF	Pickup Alarm Without Sensitive Earth Fault Enabled
* 1	00097	BF Trip	Breaker Fail Trip
* 1	00098	BF Retrip	Breaker Fail Retrip
(L) * 1	00099	BF Trip	Breaker Fail Trip
(L) * 1	00100	BF Retrip	Breaker Fail Retrip
** 1	00101	32P	Phase Power Directional Alarm (positive sequence)
** 1	00102	32N	Phase Power Directional Alarm (negative sequence)
(L) ** 1	00103	32P	Phase Power Directional Alarm (positive sequence)
(L) ** 1	00104	32N	Phase Power Directional Alarm (negative sequence)
(L) ** 1	00105	BFA	Breaker Failure Alarm
(L) *** 1	00106	25	Synch Check Function
*** 1	00107	25	Synch Check Function Operating
***	00108	SBA	Slow Breaker Alarm
*	00109	79V Block	Low Voltage Block Reclose
*	00110	Reclose Initiated	Reclose Initiated
@	00111	59G	Ground Voltage
@ (L)	00112	59G	Ground Voltage Latched
@	00113	LO1	Latching Output 1
@	00114	LO2	Latching Output 2
@	00115	LO3	Latching Output 3
@	00116	LO4	Latchitng Output 4
@	00117	LO5	Latching Output 5
@	00118	LO6	Latching Output 6
@	00119	LO7	Latching Output 7
@	00120	LO8	Latching Output 8

	Register Address	Item	Description
@	00121	TR ON	Tagging Relay ON
@	00122	TR OFF	Tagging Relay OFF
@	00123	TR TAG	Tagging Relay TAGGED
&	00124	3PH 59	3 Phase Overvoltage
& (L)	00125	3PH 59	3 Phase Overvoltage Latched
&	00126	47	Negative Sequence Overvoltage
& (L)	00127	47	Negative Sequence Overvoltage Latched
@	00128	SPARE	RESERVED
&	00129	21-P1	Phase Distance Zone 1
& (L)	00130	21-P1	Phase Distance Zone 1 Latched
&	00131	21-P2	Phase Distance Zone 2
& (L)	00132	21-P2	Phase Distance Zone 2 Latched
&	00133	21-P3	Phase Distance Zone 3
& (L)	00134	21-P3	Phase Distance Zone 3 Latched
&	00135	21-P4	Phase Distance Zone 4
& (L)	00136	21-P4	Phase Distance Zone 4 Latched
E &	00137:	C1 (Control Button 1)	Control Button Status 1= Energized, 0 = De Energized
E &	00138:	C2 (Control Button 2)	Control Button Status 1= Energized, 0 = De Energized
E &	00139:	C3 (Control Button 3)	Control Button Status 1= Energized, 0 = De Energized
E &	00140:	C4 (Control Button 4)	Control Button Status 1= Energized, 0 = De Energized
E &	00141:	C5 (Control Button 5)	Control Button Status 1= Energized, 0 = De Energized
E &	00142:	C6 (Control Button 6)	Control Button Status 1= Energized, 0 = De Energized
&	00143:	TripT	Trip Target Energized
&	00144:	NTA	Neutral Target Alarm
&	00145:	TimeT	Time Target Energized
&	00146:	InstT	Instantaneous Target Energized
&	00147:	NegSeqT	Negative Sequence Target Energized
&	00148:	FreqT	Frequency Target Energized
&	00149:	DirT	Directional Target Energized
&	00150:	VoltT	Voltage Target Energized
&	00151:	DistT	Distance Target Energized
&	00152:	SEFT	Sensitive Earth Fault Target Energized
&	00153	ULO10	User Logical Output 10 Status
&	00154	ULO11	User Logical Output 11 Status
&	00155	ULO12	User Logical Output 12 Status
&	00156	ULO13	User Logical Output 13 Status
&	00157	ULO14	User Logical Output 14 Status
&	00158	ULO15	User Logical Output 15 Status
&	00159	ULO16	User Logical Output 16 Status
&	00160	LBLL	Live Bus Live Line Status
&	00161	LBDL	Live Bus Dead Line Status
&	00162	DBLL	Live Bus Live Line Status
&	00163	DBDL	Dead Bus Dead Line Status
&	00164	46A	Negative Sequence Time Overcurrent Trip Alarm
& (L)	00165	46A*	Negative Sequence Time Overcurrent Trip Alarm (Latched)
&	00166	REMOTE – D	Local Remote Disabled Status
&&	00167	Prim Sett Active	Primary Settings are Active

	Register Address	Item	Description
	00168	ALT1 Sett Active	Alternate Setting Group 1 is Active
&&	00169	ALT2 Sett Active	Alternate Setting Group 2 is Active
&&	00170	SHIFTA-1	TEST SHIFTER A is in Position 1
&&	00171	SHIFTA-2	TEST SHIFTER A is in Position 2
&&	00172	SHIFTA-3	TEST SHIFTER A is in Position 3
&&	00173	SHIFTA-4	TEST SHIFTER A is in Position 4
&&	00174	SHIFTB-1	TEST SHIFTER B is in Position 1
&&	00175	SHIFTB-2	TEST SHIFTER B is in Position 2
&&	00176	SHIFTB-3	TEST SHIFTER B is in Position 3
&&	00177	SHIFTB-4	TEST SHIFTER B is in Position 4
Notes:	(L) = Seal In Latch Alarm DPU 2000R Only * = CPU Version 1.60 or later ** = CPU Version 1.80 or later. *** = CPU Version 1.93 or later. @ = CPU Version 3.30 or later & = CPU VERSION 5.0 or Later DPU 2000R Only. E = Enhanced Front Panel Interface Only. && = CPU VERSION 6.0 or Later DPU 2000R Only.		

Physical Output Block (Single Bit Data) – 16 Discrete Coils (10 Elements Defined)

Output status is described in Table 6-4. The state of the addresses 00257 through 00272 follow the state of the physical output hardware contacts located at the rear screw terminals of the relay. It should be noted that some of the Physical Output contact status information is not available in the DPU2000R. Table 4 notes the elements, which are undefined in the DPU2000R. The DPU2000R has six physical output contacts, which are map-able via ECP software. The DPU2000R has a single dedicated physical output contact defined as TRIP. The DPU2000 has eight map-able physical output contacts (1 through 8) and a dedicated TRIP and CLOSE contact. The status of the element mirrors that of the physical contact and that reported through the DPU2000/2000R/1500R front panel interface of through the ECP or WinECP configuration program.

Table 6-2. Physical Output Contact Mapping Defined

	DISCRETE ADDRESS	ITEM	DESCRIPTION
	00257	Spare	Reserved
	00258	Spare	Reserved
	00259	Spare	Reserved
	00260	Spare	Reserved
	00261	Spare	Reserved
	00262	Spare	Reserved
D	00263	OUT 8	Physical Output Contact 8
D	00264	OUT 7	Physical Output Contact 7
	00265	OUT 6	Physical Output Contact 6
	00266	OUT 5	Physical Output Contact 5
	00267	OUT 4	Physical Output Contact 4
	00268	OUT 3	Physical Output Contact 3
	00269	OUT 2	Physical Output Contact 2
	00270	OUT 1	Physical Output Contact 1
D	00271	CLOSE	Breaker Close Physical Output Contact
	00272	TRIP	Breaker Trip Physical Output Contact
	D = DPU2000 Only Reserved in DPU2000R		

Logical Output Block (Two Bit Data with Momentary Change Detection): Not available on DPU2000 (354 Elements Defined)

Modbus does not support features commonly required within the utility industry. However, the protocol may easily be adapted to support features required. It is most important that no event is to be missed by a polling host when a device is not accessed. To this end, a feature has been developed which ensures that the status of the data change is always reported. Table 6-3 lists the Momentary Logical Output Mapping.

Table 6-3. Momentary Change Detect Data Definition

	Register Address	Item	Description
	00513	TRIP Status	Breaker is Tripping
	00514	TRIP Momentary	Breaker Tripped Since Last Read
	00515	CLOSE Status	Breaker is Closing
	00516	CLOSE Momentary	Breaker Closed Since Last Read
	00517	ALARM Status	DPU is in Alarm
	00518	ALARM Momentary	Alarm Since Last Read
	00519	27 Status	Undervoltage Trip
	00520	27 Momentary	Undervoltage Trip Since Last Read
	00521	46 Status	Negative Sequence Overcurrent Trip
	00522	46 Momentary	Negative Sequence Overcurrent Trip Since Last Read
	00523	50P1Status	Phase Instantaneous Overcurrent Trip Since Last Read
	00524	50P1 Momentary	Phase Instantaneous Overcurrent Trip
	00525	50N1 Status	Neutral Instantaneous Overcurrent Trip
	00526	50N1 Momentary	Neutral Instantaneous Overcurrent Trip Since Last Read
	00527	50P2 Status	Phase Instantaneous Overcurrent Trip
	00528	50P2 Momentary	Phase Instantaneous Overcurrent Trip Since Last Read
	00529	50N2 Status	Neutral Instantaneous Overcurrent Trip
	00530	50N2 Momentary	Neutral Instantaneous Overcurrent Trip Since Last Read
	00531	50P3 Status	Phase Instantaneous Overcurrent Trip
	00532	50P3 Momentary	Phase Instantaneous Overcurrent Trip Change Since Last Read
	00533	50N3 Status	Neutral Instantaneous Overcurrent Trip
	00534	50N3 Momentary	Neutral Instantaneous Overcurrent Trip Change Since Last Read
	00535	51P Status	Phase Time Overcurrent Enabled
	00536	51P Momentary	Phase Time Overcurrent Enabled Change Since Last Read
	00537	51N Status	Neutral Time Overcurrent Enabled
	00538	51N Momentary	Neutral Time Overcurrent Enabled Change Since Last Read
1	00539	59 Status	Overvoltage Trip
1	00540	59 Momentary	Overvoltage Trip Change Since Last Read
1	00541	67P Status	Direct Overcurrent Trip Positive Sequence
1	00542	67P Momentary	Direct Overcurrent Trip Positive Sequence Change Since Last Read
1	00543	67N Status	Direct Overcurrent Trip Negative Sequence
1	00544	67N Momentary	Direct Overcurrent Trip Negative Sequence Change Since Last Read
1	00545	81S-1 Status	Frequency Shed (1st Stage)
1	00546	81S-1 Momentary	Frequency Shed (1st Stage) Change Since Last Read
1	00547	81R-1 Status	Frequency Restore (1st Stage)
1	00548	81R-1 Momentary	Frequency Shed (1st Stage) Change Since Last Read
	00549	PATA Status	Phase A Target Alarm Energized
	00550	PATA Momentary	Phase A Target Alarm Energized Change Since Last Read
	00551	PATB Status	Phase B Target Alarm Energized
	00552	PATB Momentary	Phase B Target Alarm Energized Change Since Last Read

	Register Address	Item	Description
	00553	PATC Status	Phase C Target Alarm Energized
	00554	PATC Momentary	Phase C Target Alarm Energized Change Since Last Read
	00555	TCFA Status	Trip Coil Failure Alarm Energized
	00556	TCFA Momentary	Trip Coil Failure Alarm Energized Change Since Last Read
	00557	TCC Status	Tap Changer Cutoff Energized
	00558	TCC Momentary	Tap Changer Cutoff Energized Change Since Last Read
	00559	79DA Status	Reclosing Disabled Alarm Energized
	00560	79DA Momentary	Reclosing Disabled Alarm Energized Change Since Last Read
	00561	PUA Status	Pick Up Alarm Status
	00562	PUA Momentary	Pick Up Alarm Change Energized Since Last Read
	00563	79LOA Status	Recloser Lock Out Alarm Energized
	00564	79LOA Momentary	Recloser Lock Out Alarm Energized Change Since Last Read
	00565	BFA Status	Breaker Fail Alarm Energized
	00566	BFA Momentary	Breaker Fail Alarm Energized Change Since Last Read
	00567	PDA Status	Physical Demand Current Alarm Energized
	00568	PDA Momentary	Physical Demand Current Alarm Energized Change Since Last Read
	00569	NDA Status	Neutral Demand Current Alarm Energized
	00570	NDA Status	Neutral Demand Current Alarm Energized Change Since Last Read
	00571	BFUA Status	Blown Fuse Alarm Energized
	00572	BFUA Momentary	Blown Fuse Alarm Energized Change Since Last Read
	00573	KSI Status	Kiloamperes Symmetrical Inverted Alarm Energized
	00574	KSI Momentary	Kiloamperes Symmetrical Inverted Alarm Energized Change Since Last Read
	00575	79CA1 Status	Recloser Counter Alarm 1 Energized
	00576	79CA1 Momentary	Recloser Counter Alarm 1 Energized Change Since Last Read
	00577	HPFA Status	High Power Factor Alarm Energized
	00578	HPFA Momentary	High Power Factor Alarm Energized Change Since Last Read
	00579	LPFA Status	Low Power Factor Alarm Energized
	00580	LPFA Momentary	Low Power Factor Alarm Energized Change Since Last Read
	00581	OCTC Status	Overcurrent Trip Counter Alarm Energized
	00582	OCTC Momentary	Overcurrent Trip Counter Alarm Energized Change Since Last Read
	00583	50-1D Status	1st Instantaneous Overcurrent Distance Alarm Energized
	00584	50-1D Momentary	1st Instantaneous Overcurrent Distance Alarm Energized Change Since Last Read
	00585	50-2D Status	2nd Instantaneous Overcurrent Distance Alarm Energized
	00586	50-2D Momentary	2nd Instantaneous Overcurrent Distance Alarm Energized Change Since Last Read
	00587	STC Status	Settings Table Change Alarm Energized
	00588	STC Momentary	Settings Table Change Alarm Energized Change Since Last Read
	00589	ZSC Status	Zone Sequence Control Alarm Energized
	00590	ZSC Momentary	Zone Sequence Control Alarm Energized Change Since Last Read
	00591	PH3-D Status	Phase Overcurrent Disabled Alarm Energized
	00592	PH3-D Momentary	Phase Overcurrent Disabled Alarm Energized Change Since Last Read
	00593	GRD-D Status	Ground Overcurrent Disabled Alarm Energized
	00594	GRD-D Momentary	Ground Overcurrent Disabled Alarm Energized Change Since Last Read
1	00595	32 PA Status	(67P) Positive Sequence Direct Overcurrent Trip Alarm Energized

	Register Address	Item	Description
1	00596	32 PA Momentary	(67P) Positive Sequence Direct Overcurrent Trip Alarm Energized Change Since Last Read
1	00597	32 PN Status	(67N) Negative Sequence Direct Overcurrent Trip Alarm Energized
1	00598	32 PN Momentary	(67N) Negative Sequence Direct Overcurrent Trip Alarm Energized Change Since Last Read
	00599	27-3P Status	Three Phase Undervoltage Trip Energized
	00600	27-3P Momentary	Three Phase Undervoltage Trip Energized Change Since Last Read
	00601	VARDA Status	3 Phase KVAR Demand Alarm Energized
	00602	VARDA Momentary	3 Phase KVAR Demand Alarm Energized Change Since Last Read
	00603	79CA2 Status	Recloser Counter Alarm 2 Energized
	00604	79CA2 Momentary	Recloser Counter Alarm 2 Energized Change Since Last Read
	00605	TRIP A Status	Single Phase Trip (Phase A)
	00606	TRIP A Momentary	Single Phase Trip (Phase A) Change Since Last Read
	00607	TRIP B Status	Single Phase Trip (Phase B)
	00608	TRIP B Momentary	Single Phase Trip (Phase B) Change Since Last Read
	00609	TRIP C Status	Single Phase Trip (Phase C)
	00610	TRIP C Momentary	Single Phase Trip (Phase C) Change Since Last Read
(L) 1	00611	27 Status	Undervoltage Trip
(L) 1	00612	27 Momentary	Undervoltage Trip Change Since Last Read
(L)	00613	46 Status	Negative Sequence Overcurrent Trip
	00614	46 Momentary	Negative Sequence Overcurrent Trip Change Since Last Read
(L)	00615	50P1 Status	Phase Instantaneous Overcurrent Trip
	00616	50P1 Momentary	Phase Instantaneous Overcurrent Trip Change Since Last Read
(L)	00617	50N1 Status	Neutral Instantaneous Overcurrent Trip
	00618	50N1 Momentary	Neutral Instantaneous Overcurrent Trip Change Since Last Read
(L)	00619	50P2 Status	Phase Instantaneous Overcurrent Trip
	00620	50P2 Momentary	Phase Instantaneous Overcurrent Trip Change Since Last Read
(L)	00621	50N2 Status	Neutral Instantaneous Overcurrent Trip
	00622	50N2 Momentary	Neutral Instantaneous Overcurrent Trip Change Since Last Read
(L)	00623	50P3 Status	Phase Instantaneous Overcurrent Trip
	00624	50P3 Momentary	Phase Instantaneous Overcurrent Trip Change Since Last Read
(L)	00625	50N3 Status	Neutral Instantaneous Overcurrent Trip
	00626	50N3 Momentary	Neutral Instantaneous Overcurrent Trip Change Since Last Read
(L)	00627	51P Status	Phase Instantaneous Overcurrent Enabled
	00628	51P Momentary	Phase Instantaneous Overcurrent Enabled Change Since Last Read
(L)	00629	51N Status	Neutral Instantaneous Overcurrent Enabled Change Since Last Read
	00630	51N Momentary	Neutral Instantaneous Overcurrent
(L)	00631	59 Status	Overvoltage Trip
	00632	59 Momentary	Overvoltage Trip Change Since Last Read
(L)	00633	67P Status	Direct Overcurrent Trip Positive Sequence
	00634	67P Momentary	Direct Overcurrent Trip Positive Sequence Change Since Last Read
(L)	00635	67N Status	Direct Overcurrent Trip Negative Sequence
	00636	67N Momentary	Direct Overcurrent Trip Negative Sequence Change Since Last Read
(L)	00637	81S-1 Status	Frequency Shed (1st Stage)

	Register Address	Item	Description
	00638	81S-1 Momentary	Frequency Shed (1st Stage) Change Since Last Read
(L)	00639	81R-1 Status	Frequency Restore (1st Stage)
	00640	81R-1 Momentary	Frequency Restore (1st Stage) Change Since Last Read
(L)	00641	81O-1 Status	Overfrequency (1st Stage)
	00642	81O-1 Momentary	Overfrequency (1st Stage) Change Since Last Read
(L)	00643	27-3P Status	Three Phase Undervoltage Trip Energized
	00644	27-3P Momentary	Three Phase Undervoltage Trip Energized Change Since Last Read
(L)	00645	TRIP A Status	Single Phase Trip (Phase A)
	00646	TRIP A Momentary	Single Phase Trip (Phase A) Change Since Last Read
(L)	00647	TRIP B Status	Single Phase Trip (Phase B)
	00648	TRIP B Momentary	Single Phase Trip (Phase B) Change Since Last Read
(L)	00649	TRIP C Status	Single Phase Trip (Phase C)
	00650	TRIP C Momentary	Single Phase Trip (Phase C) Change Since Last Read
1	00651	ULO 1 Status	User Logical Output 1
1	00652	ULO 1 Momentary	User Logical Output 1 Change Since Last Read
1	00653	ULO 2 Status	User Logical Output 2
1	00654	ULO 2 Momentary	User Logical Output 2 Change Since Last Read
1	00655	ULO 3 Status	User Logical Output 3
1	00656	ULO 3 Momentary	User Logical Output 3 Change Since Last Read
1	00657	ULO 4 Status	User Logical Output 4
1	00658	ULO 4 Momentary	User Logical Output 4 Change Since Last Read
1	00659	ULO 5 Status	User Logical Output 5
1	00660	ULO 5 Momentary	User Logical Output 5 Change Since Last Read
1	00661	ULO 6 Status	User Logical Output 6
1	00662	ULO 6 Momentary	User Logical Output 6 Change Since Last Read
1	00663	ULO 7 Status	User Logical Output 7
1	00664	ULO 7 Momentary	User Logical Output 7 Change Since Last Read
1	00665	ULO 8 Status	User Logical Output 8
1	00666	ULO 8 Momentary	User Logical Output 8 Change Since Last Read
1	00667	ULO 9 Status	User Logical Output 9
1	00668	ULO 9 Momentary	User Logical Output 9 Change Since Last Read
	00669	PVARA Status	Positive 3 Phase KVAR Alarm Energized
	00670	PVARA Momentary	Positive 3 Phase KVAR Alarm Energized Change Since Last Read
	00671	NVARA Status	Negative 3 Phase KVAR Alarm Energized
	00672	NVARA Momentary	Negative 3 Phase KVAR Alarm Energized Change Since Last Read
	00673	LOADA Status	Load Current Alarm Energized
	00674	LOADA Momentary	Load Current Alarm Energized Change Since Last Read
	00675	81O-1 Status	Overfrequency (1st Stage)
1	00676	81O-1 Momentary	Overfrequency (1st Stage) Change Since Last Read
1	00677	81O-2 Status	Overfrequency (2nd Stage)
1	00678	81O-2 Momentary	Overfrequency (2nd Stage) Change Since Last Read
1	00679	81S-2 Status	Frequency Shed (2nd Stage)
1	00680	81S-2 Momentary	Frequency Shed (2nd Stage) Change Since Last Read
1	00681	81R-2 Status	Frequency Restore (2nd Stage)
1	00682	81R-2 Momentary	Frequency Restore (2nd Stage) Change Since Last Read
1	00683	81O-2 Status	Overfrequency (2nd Stage)
1	00684	81O-2 Momentary	Overfrequency (2nd Stage) Change Since Last Read
1	00685	81S-2 Status	Frequency Shed (2nd Stage)
1	00686	81S-2 Momentary	Frequency Shed (2nd Stage) Change Since Last Read
1	00687	81R-2 Status	Frequency Restore (2nd Stage)

	Register Address	Item	Description
1	00688	81R-2 Momentary	Frequency Restore (2nd Stage) Change Since Last Read
	00689	CLTA Status	Cold Load Timer Alarm
	00690	CLTA Momentary	Cold Load Timer Alarm Change Since Last Read
	00691	Watt 1 Status	Positive Watt Alarm 1
	00692	Watt 1 Momentary	Positive Watt Alarm 1 Change Since Last Read
	00693	Watt 2 Status	Positive Watt Alarm 2
	00694	Watt 2 Momentary	Positive Watt Alarm 2 Change Since Last Read
(L)	00695	79CA1 Status	Reclose Counter Alarm 1
	00696	79CA1 Momentary	Reclose Counter Alarm 1 Change Since Last Read
(L)	00697	79CA2 Status	Reclose Counter Alarm 2
	00698	79CA2 Momentary	Reclose Counter Alarm 2 Change Since Last Read
(L)	00699	SEF Status	Sensitive Earth Fault
	00700	SEF Momentary	Sensitive Earth Fault Change Since Last Read
	00701	SEF Alarm Status	Sensitive Earth Fault Alarm Energized
	00702	SEF Alarm Momentary	Sensitive Earth Fault Alarm Energized Change Since Last Read
	00703	PUA w/o SEF Status	Pickup Alarm Without Sensitive Earth Fault Enabled Change Since Last Read
	00704	PUA w/o SEF Momentary	Pickup Alarm Without Sensitive Earth Fault Enabled
	00705	BF Trip Status	Breaker Fail Trip
	00706	BF Trip Momentary	Breaker Fail Trip Change Since Last Read
	00707	BF Retrip Status	Breaker Fail Retrip
	00708	BF Retrip Momentary	Breaker Fail Retrip Change Since Last Read
(L)	00709	BF Trip Status	Breaker Fail Trip
	00710	BF Trip Momentary	Breaker Fail Trip Change Since Last Read
(L)	00711	BF Retrip Status	Breaker Fail Retrip
	00712	BF Retrip Momentary	Breaker Fail Retrip Change Since Last Read
1	00713	32P Status	Phase Power Directional Alarm (positive sequence)
1	00714	32P Momentary	Phase Power Directional Alarm (positive sequence) Change Since Last Read
1	00715	32N Status	Phase Power Directional Alarm (negative sequence)
1	00716	32N Momentary	Phase Power Directional Alarm (negative sequence)
(L) 1	00717	32P Status	Phase Power Directional Alarm (positive sequence) Change Since Last Read
1	00718	32P Momentary	Phase Power Directional Alarm (positive sequence)
(L) 1	00719	32N Status	Phase Power Directional Alarm (negative sequence) Change Since Last Read
1	00720	32N Momentary	Phase Power Directional Alarm (negative sequence) Change Since Last Read
(L)	00721	BFA Status	Breaker Failure Alarm
	00722	BFA Momentary	Breaker Failure Alarm Change Since Last Read
(L)	00723	25 Status	Sync Check Function
	00724	25 Momentary	Sync Check Function Change Since Last Read
1	00725	25 Status	Sync Check Function Operating
1	00726	25 Momentary	Sync Check Function Operating Change Since Last Read
	00727	SBA Status	Slow Breaker Alarm
	00728	SBA Momentary	Slow Breaker Alarm Change Since Last Read
*	00729	79V Block	Low Voltage Block Reclose
	00730	79V Block Momentary	Low Voltage Block Reclose Momentary
*	00731	Reclose Initiated	Reclose Initiated

	Register Address	Item	Description
	00732	Reclose Initiated Momentary	Reclose Initiated Momentary
**1	00733	59G	Ground Voltage
**1	00734	59G Momentary	Ground Voltage Momentary
** (L) 1	00735	59G	Ground Voltage Latched
*** (L) 1	00736	59G Momentary	Ground Voltage Latched Momentary
*** 1	00737	LO1	Latching Output 1
*** 1	00738	LO1 Momentary	Latching Output 1 Momentary
*** 1	00739	LO2	Latching Output 2
*** 1	00740	LO2 Momentary	Latching Output 2 Momentary
*** 1	00741	LO3	Latching Output 3
*** 1	00742	LO3 Momentary	Latching Output 3 Momentary
*** 1	00743	LO4	Latchitng Output 4
*** 1	00744	LO4 Momentary	Latchitng Output 4 Momentary
***1	00745	LO5	Latching Output 5
*** 1	00746	LO5 Momentary	Latching Output 5 Momentary
*** 1	00747	LO6	Latching Output 6
*** 1	00748	LO6 Momentary	Latching Output 6 Momentary
*** 1	00749	LO7	Latching Output 7
*** 1	00750	LO7 Momentary	Latching Output 7 Momentary
*** 1	00751	LO8	Latching Output 8
*** 1	00752	LO8 Momentary	Latching Output 8 Momentary
*** 1	00753	TR ON	Tagging Relay ON
*** 1	00754	TR ON Momentary	Tagging Relay ON Momentary
*** 1	00755	TR OFF	Tagging Relay OFF
*** 1	00756	TR OFF Momentary	Tagging Relay OFF Momentary
*** 1	00757	TR TAG	Tagging Relay TAGGED
*** 1	00758	TR TAG Momentary	Tagging Relay TAGGED Momentary
** 1	00759	3PH 59	3 Phase Overvoltage
**1	00760	3PH 59 Momentary	3 Phase Overvoltage Momentary
** 1 (L)	00761	3PH 59	3 Phase Overvoltage Latched
** 1 (L)	00762	3PH 59 Momentary	3 Phase Overvoltage Latched Momentary
** 1	00763	47	Negative Sequence Overvoltage
** 1	00764	47 Momentary	Negative Sequence Overvoltage Momentary
** 1 (L)	00765	47	Negative Sequence Overvoltage Latched
** 1 (L)	00766	47 Momentary	Negative Sequence Overvoltage Latched Momentary
&	00767	50- 3D	Instantaneous 3 Phase Overcurrent Alarm Disabled
&	00768	50-3D Momentary	Momentary Status
**1	00769	21-P1	Phase Distance Zone 1
**1	00770	21-P1 Momentary	Phase Distance Zone 1 Momentary
**1	00771	21-P1	Phase Distance Zone 1 Latched
**1	00772	21-P1 Momentary	Phase Distance Zone 1 Latched Momentary
** 1 (L)	00773	21-P2	Phase Distance Zone 2
** 1 (L)	00774	21-P2 Momentary	Phase Distance Zone 2 Momentary
** 1	00775	21-P2	Phase Distance Zone 2 Latched
** 1	00776	21-P2 Momentary	Phase Distance Zone 2 Latched Momentary
** 1 (L)	00777	21-P3	Phase Distance Zone 3
** 1 (L)	00778	21-P3 Momentary	Phase Distance Zone 3 Momentary
** 1	00779	21-P3	Phase Distance Zone 3 Latched
** 1	00780	21-P3 Momentary	Phase Distance Zone 3 Latched Momentary
** 1 (L)	00781	21-P4	Phase Distance Zone 4
** 1 (L)	00782	21-P4 Momentary	Phase Distance Zone 4 Momentary
** 1	00783	21-P4	Phase Distance Zone 4 Latched

	Register Address	Item	Description
** 1	00784	21-P4 Momentary	Phase Distance Zone 4 Latched Momentary
E &	00785	C1 (Control Button 1)	Control Button Status 1= Energized, 0 = De Energized
E &	00786	C1 (Control Button 1) Momentary	Momentary Status
E &	00787	C2 (Control Button 2)	Control Button Status 1= Energized, 0 = De Energized
E &	00788	C2 (Control Button 2) Momentary	Momentary Status
E &	00789	C3 (Control Button 3)	Control Button Status 1= Energized, 0 = De Energized
E &	00790	C3 (Control Button 3) Momentary	Momentary Status
E &	00791	C4 (Control Button 4)	Control Button Status 1= Energized, 0 = De Energized
E &	00792	C4 (Control Button 4) Momentary	Momentary Status
E &	00793	C5 (Control Button 5)	Control Button Status 1= Energized, 0 = De Energized
E &	00794	C5 (Control Button 5)Momentary	Momentary Status
E &	00795	C6 (Control Button 6)	Control Button Status 1= Energized, 0 = De Energized
E &	00796	C6 (Control Button 6)Momentary	Momentary Status
&	00797	TripT	Trip Target Energized
&	00798	TripT Momentary	Momentary Status
&	00799	NTA	Neutral Target Alarm
&	00800	NTA Momentary	Momentary Status
&	00801	TimeT	Time Target Energized
&	00802	Momentary	Momentary Status
&	00803	InstT	Instantaneous Target Energized
&	00804	InstT Momentary	Momentary Status
&	00805	NegSeqT	Negative Sequence Target Energized
&	00806	NegSeqT Momentary	Momentary Status
&	00807	FreqT	Frequency Target Energized
&	00808	FreqT Momentary	Momentary Status
&	00809	DirT	Directional Target Energized
&	00810	Momentary	Momentary Status
&	00811	VoltT	Voltage Target Energized
&	00812	VoltT Momentary	Momentary Status
&	00813	DistT	Distance Target Energized
&	00814	DistT Momentary	Momentary Status
&	00815	SEFT	Sensitive Earth Fault Target Energized
&	00816	SEFT Momentary	Momentary Status
&	00817	ULO10	User Logical Output 10 Status
&	00818	ULO10 Momentary	Momentary Status
&	00819	ULO11	User Logical Output 11 Status
&	00820	ULO11 Momentary	Momentary Status
&	00821	ULO12	User Logical Output 12 Status
&	00822	ULO12 Momentary	Momentary Status
&	00823	ULO13	User Logical Output 13 Status
&	00824	ULO13 Momentary	Momentary Status

	Register Address	Item	Description
&	00825	ULO14	User Logical Output 14 Status
&	00826	ULO14 Momentary	Momentary Status
&	00827	ULO15	User Logical Output 15 Status
&	00828	ULO15 Momentary	Momentary Status
&	00829	ULO16	User Logical Output 16 Status
&	00830	ULO16 Momentary	Momentary Status
&	00831	LBLL	Live Bus Live Line Status
&	00832	LBLL Momentary	Momentary Status
&	00833	LBDL	Live Bus Dead Line Status
&	00834	LBDL Momentary	Momentary Status
&	00835	DBLL	Live Bus Live Line Status
&	00836	DBLL Momentary	Momentary Status
&	00837	DBDL	Dead Bus Dead Line Status
&	00838	DBDL Momentary	Momentary Status
&	00839	46A	Negative Sequence Time Overcurrent Trip Alarm
&	00840	46A Momentary	Momentary Status
& (L)	00841	46A*	Negative Sequence Time Overcurrent Trip Alarm (Latched)
& (L)	00842	46A* Momentary	Momentary Status
&	00843	REMOTE – D	Local Remote Disabled Status
&	00844	REMOTE – D Momentary	Momentary Status
&&	00845	Prim Sett Active	Primary Settings Group Active Status
&&	00846	Prim Sett Active Momentary	Primary Settings Group Active Momentary Status
&&	00847	ALT1 Sett Active	Alternate Settings Group 1 Active Status
&&	00848	ALT1 Sett Active Momentary	Alternate Settings Group 1 Active Momentary Status
&&	00849	ALT2 Sett Active	Alternate Settings Group 2 Active Status
&&	00850	ALT2 Sett Active Momentary	Alternate Settings Group 2 Active Momentary Status
&&	00851	SHIFTA-1	TEST SHIFTER A is in Position 1
&&	00852	SHIFTA-1 Momentary	TEST SHIFTER A is in Position 1 Momentary Status
&&	00853	SHIFTA-2	TEST SHIFTER A is in Position 2
&&	00854	SHIFTA-2 Momentary	TEST SHIFTER A is in Position 2 Momentary Status
&&	00855	SHIFTA-3	TEST SHIFTER A is in Position 3
&&	00856	SHIFTA-3 Momentary	TEST SHIFTER A is in Position 3 Momentary Status
&&	00857	SHIFTA-4	TEST SHIFTER A is in Position 4
&&	00858	SHIFTA-4 Momentary	TEST SHIFTER A is in Position 4 Momentary Status
&&	00859	SHIFTB-1	TEST SHIFTER A is in Position 1
&&	00860	SHIFTB-1 Momentary	TEST SHIFTER A is in Position 1 Momentary Status
&&	00861	SHIFTB-2	TEST SHIFTER A is in Position 2
&&	00862	SHIFTB-2 Momentary	TEST SHIFTER A is in Position 2 Momentary Status
&&	00863	SHIFTB-3	TEST SHIFTER A is in Position 3
&&	00864	SHIFTB-3 Momentary	TEST SHIFTER A is in Position 3 Momentary Status
&&	00865	SHIFTB-4	TEST SHIFTER A is in Position 4
&&	00866	SHIFTB-4 Momentary	TEST SHIFTER A is in Position 4 Momentary Status

	Register Address	Item	Description
Notes:	(L) = Latched Bit Status * = Version CPU Version 1.60 or Greater ** = CPU Version 5.0 or Greater *** = CPU Version 3.20 or Greater 1 = DPU 2000R Only E = Enhanced Front Panel Interface Only. && = DPU 2000R VERSION 6.0 or Greater		

Physical Output Block (Two Bit Data with Momentary Change Detection): Not available on DPU2000

The DPU2000R allows for momentary bit change detect for all physical outputs on the protective device. The physical output devices. The status bit will reflect the same status as that of 00257 through 00272. The momentary bit shall detect a status change between reads of the element's data. As always, the bits must be read in pairs for accurate reporting of the element status. Table 6-4 lists the definitions of each defined 0X address.

Table 6-4. Modbus Physical Output Momentary Change Detect Address Allocation

Discrete Address	Item	Description
01025:	Spare Status	Reserved
01026	Spare Momentary	Reserved
01027	Spare Status	Reserved
01028	Spare Momentary	Reserved
01029	Spare Status	Reserved
01030	Spare Momentary	Reserved
01031	Spare Status	Reserved
01032	Spare Momentary	Reserved
01033	Spare Status	Reserved
01034	Spare Momentary	Reserved
01035	Spare Status	Reserved
01036	Spare Momentary	Reserved
01037	OUT 8	Physical Output Contact 8
01038	OUT 8	Physical Output Contact 8 Change Detect Between Scans
01039	OUT 7	Physical Output Contact 7
01040	OUT 7	Physical Output Contact 7 Change Detect Between Scans
01041	OUT 6	Physical Output Contact 6
01042	OUT 6	Physical Output Contact 6 Change Detect Between Scans
01043	OUT 5	Physical Output Contact 5
01044	OUT 5	Physical Output Contact 5 Change Detect Between Scans
01045	OUT 4	Physical Output Contact 4
01046	OUT 4	Physical Output Contact 4 Change Detect Between Scans
01047	OUT 3	Physical Output Contact 3
01048	OUT 3	Physical Output Contact 3 Change Detect Between Scans
01049	OUT 2	Physical Output Contact 2
01050	OUT 2	Physical Output Contact 2 Change Detect Between Scans
01051	OUT 1	Physical Output Contact 1
01052	OUT 1	Physical Output Contact 1 Change Detect Between Scans
01053	Spare Status	Reserved
01054	Spare Momentary	Reserved
01055	TRIP Status	Breaker Trip Physical Output Contact
01056	TRIP Momentary	Breaker Trip Physical Output Contact Change Detect Between Scans

Section 7 - 1X Discrete Contact Inputs (Not Available on the DPU2000)

Discrete physical input and relay element status are available via a function 02 request through Modbus. Figure 7-1 illustrates a typical command sequence. The Host polls the DPU2000R for the Data. The DPU2000R receives the request and responds with the expected data. The Host then interprets the command response, checks the LRC checksum in ASCII mode and then displays the interpreted data. If the node is configured for RTU Modbus, the start of message character is three character delays, and the end of message consists of a CRC-16 checksum and three character delays. Additional information is available in Modicon's protocol manual references listed at the beginning of this document. The same information is available through a 4X register read command, which allows a host without 1X data accesses capabilities to obtain physical input and relay element information. Tables 7-1 through 7-5 list the 1X discrete contact memory map as defined for Modbus RTU and ASCII.

Function Code 2 - Read Input Status (Read Only Data)

Figure 7-1 illustrates the command format required for execution of function code 2.

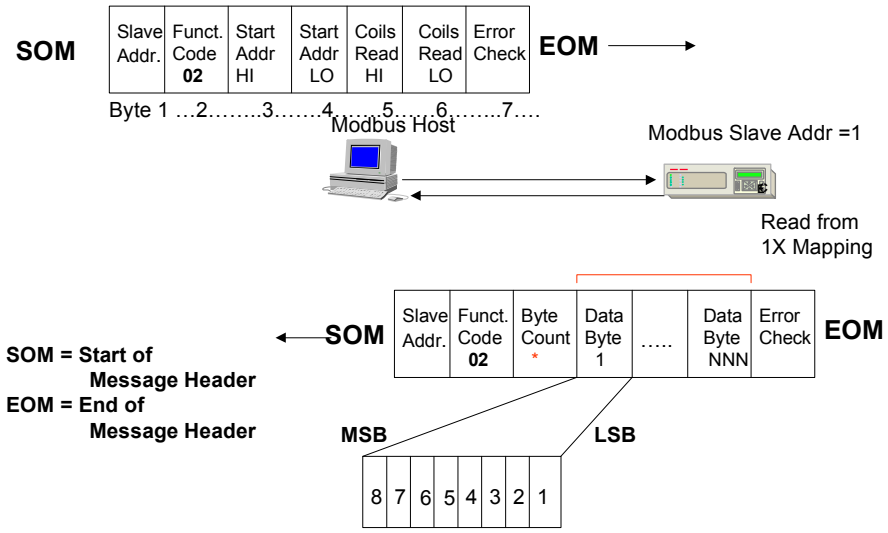


Figure 7-1. 1X Input Request Using Modbus Command 02

It should be noted that every DPU2000R allows real time status reporting when the unit is polled. If a status is momentary and is missed during the host poll, then the data is lost. Polling using the status Momentary Change Detect Feature insures that the host device does not miss the momentary change. It should also be noted that data requested from 1X data address ranges not defined within this document generates Modbus exception codes.

Utility devices require that no event is to be missed in the field IED. ABB has incorporated two methods in which a device is notified that events have occurred in the field IED between host polls. The two methods employed for 1x data (Modbus Function Code 02) are:

- MOMENTARY CHANGE DETECT

MOMENTARY CHANGE DETECT is independent of the protocol. These ABB innovations allow Modbus protocol to address and satisfy the concerns common to a utility installation. The two functionality's are those in excess of the real time status access that Modbus function code 02 affords.

Momentary Change Detect status is incorporated using two bits to indicate present status and momentary indication status. The odd bit is the status bit and the even bit is the momentary bit. The status bit indicates the present state of the element accessed. The momentary bit indicates element transitioning more than once between IED reads. The momentary bit is set to a "1" if the element has transitioned more than once. The bit is

reset upon a host access Addresses 10513 through 11056 are allocated for momentary change bit detect status detection. NOTE: MOMENTARY BITS MUST BE READ IN PAIRS.

An example of momentary change detect is illustrated in Figure 7-2. Suppose a host device monitors DPU2000R physical input bit 1. Figure 7-1 illustrates the physical input transitions of input 1. At each field voltage rising edge/falling edge transition, the status of the Modbus contact 1x addresses are listed. The dotted line arrows indicate the poll received by the DPU2000R and the state of both the status bit and the momentary indication bit. Note that the even bit (momentary change detect) resets itself to a zero state after a host read.

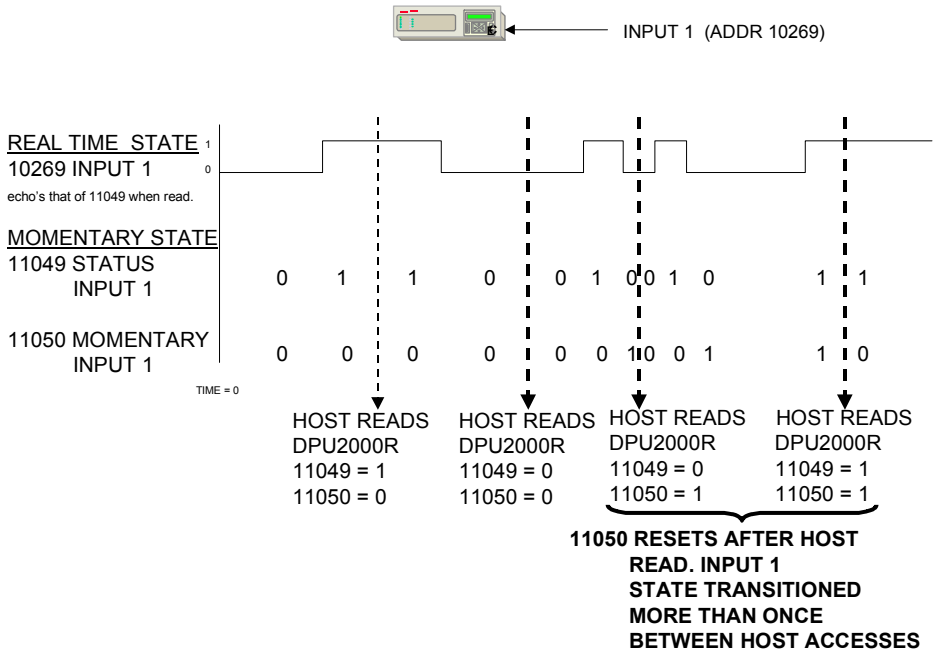


Figure 7-2. Momentary Change Detect Example

Logical Inputs (73 Elements Defined)

This section of relay information allows access of relay element data. Some of the status bit information reported in 1X discrete response is available as 0X-register definition table. All of the individual information is available in the 4X-register definition table (Modbus Function Code 03). Table 7-1 lists the discrete point address assignment for physical inputs and control elements within the DPU2000R.

52a and 52b status may be mapped and wired to the Physical Inputs provided at the rear of the DPU2000R. However, 2000R does not have these contacts wired to the 2000R physical input, status of 52a/52b, shall be reported as a function of sensed current flow. If 52a and 52b are unmapped, the DPU2000R shall report breaker status as such:

A closed breaker is determined when the input current is above 5% of the neutral nominal current rating of the relay. An open breaker (cleared breaker) is determined when the sensed current is above 5% of the neutral nominal current rating.

Table 7-1. Logical Input Modbus Address Map Definition

Note	Register Address	Item	Description
	10001	52a	Breaker Status (52a = 1 52b = 0 CB Open)
	10002	52b	Breaker Status (52a = 0 52b= 1 CB Closed)
	10003	43a	Enable Reclose Function Asserted
	10004	PH3	Enable Phase Overcurrent Protection for all Phase elements except 50-P3
	10005	GRD	Enable Ground Overcurrent Protection for all Ground elements except 50N-3
	10006	SCC	Spring Charging Contact Function Enabled
	10007	79S	Single Shot Reclosing Enabled
	10008	79M	Multiple Shot Reclosing Enabled
	10009	TCM	Trip Coil Monitoring Enabled
	10010	50-1	Enable 50P-1 and 50N-1
	10011	50-2	Enable 50P-2 and 50N-2
	10012	50-3	Enable 50P-3 and 50N-3
	10013	ALT1	Enable Alternate 1 Settings
	10014	ALT2	Enable Alternate 2 Settings
	10015	ECI1	Initiate Event Capture 1
	10016	ECI2	Initiate Event Capture 2
	10017	WCI	Waveform Capture Initiate
	10018	ZSC	Enable Zone Sequence Coordination
	10019	OPEN	Initiate Trip Output
	10020	CLOSE	Initiate Close Output
	10021	46	Enable Negative Sequence Time Overcurrent Function
&&	10022	67P	Enable Positive Sequence Directionally Controlled Phase Time Overcurrent Function
&&	10023	67N	Enable Negative Sequence Directionally Controlled Phase Time Overcurrent Function
&&	10024	ULI1	User Logical Input 1 Element Energized
&&	10025	ULI2	User Logical Input 2 Element Energized
&&	10026	ULI3	User Logical Input 3 Element Energized
&&	10027	ULI4	User Logical Input 4 Element Energized
&&	10028	ULI5	User Logical Input 5 Element Energized
&&	10029	ULI6	User Logical Input 6 Element Energized
&&	10030	ULI7	User Logical Input 7 Element Energized
&&	10031	ULI8	User Logical Input 8 Element Energized
&&	10032	ULI9	User Logical Input 9 Element Energized
	10033	CRI	Reclose and Overcurrent Counters Cleared
	10034	ARCI	Automatic Reclose Inhibit Enabled
	10035	TARC	Initiate Trip and Auto Reclose Function
	10036	SEF TC	Sensitive Earth Fault Enabled
&&	10037	ExtBFI	External Starter Input Initiated
&&	10038	BFI	Breaker Fail Initiate
	10040	UDI	User Defined Input
&&	10041	25	Sync Check Enable (Sync Check Model)
&&	10042	25 Bypass	Sync Check Bypass (Sync Check Model)
%%	10043	Local Enable	Local Control Enabled
%%	10044	SIA	Seal In Alarm
*	10045	LIS1	Latchecl Input 1 Set
*	10046	LIS2	Latchecl Input 2 Set
*	10047	LIS3	Latchecl Input 3 Set
*	10048	LIS4	Latchecl Input 4 Set
*	10049	LIS5	Latchecl Input 5 Set

Note	Register Address	Item	Description
*	10050	LIS6	Latchecl Input 6 Set
*	10051	LIS7	Latchecl Input 7 Set
*	10052	LIS8	Latchecl Input 8 Set
*	10053	LIR1	Latchecl Input 1 Reset
*	10054	LIR2	Latchecl Input 2 Reset
*	10055	LIR3	Latchecl Input 3 Reset
*	10056	LIR4	Latchecl Input 4 Reset
*	10057	LIR5	Latchecl Input 5 Reset
*	10058	LIR6	Latchecl Input 6 Reset
*	10059	LIR7	Latchecl Input 7 Reset
*	10060	LIR8	Latchecl Input 8 Reset
*	10061	TR_SET	Tagging Relay Set
*	10062	TR_RST	Tagging Relay Reset
&	10063	ULI10	User Logical Input 10 Status
&	10064	ULI11	User Logical Input 11 Status
&	10065	ULI12	User Logical Input 12 Status
&	10066	ULI13	User Logical Input 13 Status
&	10067	ULI14	User Logical Input 14 Status
&	10068	ULI15	User Logical Input 15 Status
&	10069	ULI16	User Logical Input 16 Status
&	10070	46A	Negative Sequence Time Overcurrent Trip
&&	10071	SWSET	Switch Set Test Status
&&	10072	SHIFTA	Test Shift Register A Input Status
&&	10073	SHIFTB	Test Shift Register B Input Status
			%%= CPU Firmware 1.92 Required && = Excluded in DPU1500R Unit * = CPU Firmware Version 4.10 or Later And Excluded on the DPU 1500 & = CPU Version 5.20 or later &&= CPU Version 6.00 DPU 2000R or Later

Physical Inputs (16 Elements Defined)

Physical inputs are mappable for various functional inputs. One must take care since the address map designations change depending upon whether the product is a DPU2000R, DPU2000 or DPU1500R. Their status is available at the following addresses as illustrated in Table 7-2.

Table 7-2. Physical Input Modbus Address Map Definition

Notes	Register Address	Item	Description
	10257	IN13	Physical Input 13 (DPU2000 Only)
	10258	IN12	Physical Input 12 (DPU2000R Only)
	10259	IN11	Physical Input 11 (DPU2000R Only)
	10260	IN10	Physical Input 10 (DPU2000R Only)
	10261	IN9	Physical Input 9 (DPU2000R Only)
	10262	IN8 DPU2000R/ IN6 DPU1500R	Physical Input 8 (DPU2000R) Physical Input 6 (DPU1500R Only)
	10263	IN7 DPU2000R	Physical Input 7
	10264	IN6 DPU2000R	Physical Input 6
	10265	IN5	Physical Input 5
	10266	IN4	Physical Input 4
	10267	IN3	Physical Input 3
	10268	IN2	Physical Input 2
	10269	IN1	Physical Input 1

Notes	Register Address	Item	Description
D	10270	43a	Enable Reclosing
D	10271	52b	Breaker Input Position
D	10272	52a	Breaker Input Position
	D=DPU2000 Only		

Momentary Change Detect Logical Inputs (146 Elements Defined)

Whereas the information presented in Tables 7-1 and 7-2 illustrate the real time status of the designated data points, the status in Table 7-3 lists the data in Momentary Change Detect status. The momentary change detect decoding follows the same philosophy as that presented in Section 6 for the 0X logical and physical data presentation.

Table 7-3. Logical Input Status Momentary Change Detect Status

	Register Address	Item	Description
	10513	52a Status	Breaker Status (52a = 1 52b = 0 CB Open)
	10514	52a Momentary	Breaker Status (52a = 1 52b = 0 CB Open) Change Detected Between Scans
	10515	52b Status	Breaker Status (52a = 0 52b= 1 CB Closed)
	10516	52b Momentary	Breaker Status (52a = 1 52b = 0 CB Open) Change Detected Between Scans
	10517	43a Status	Enable Reclose Function Asserted
	10518	43a Momentary	Enable Reclose Function Asserted Change Detected Between Scans
	10519	PH3 Status	Enable Phase Overcurrent Protection for all Phase elements except 50-P3
	10520	PH3 Momentary	Enable Phase Overcurrent Protection for all Phase elements except 50-P3 Change Detected Between Scans
	10521	GRD Status	Enable Ground Overcurrent Protection for all Ground elements except 50N-3
	10522	GRD Momentary	Enable Ground Overcurrent Protection for all Ground elements except 50N-3 Change Detected Between Scans
	10523	SCC Status	Spring Charging Contact Function Enabled
	10524	SCC Momentary	Spring Charging Contact Function Enabled Change Detected Between Scans
	10525	79S Status	Single Shot Reclosing Enabled
	10526	79S Momentary	Single Shot Reclosing Enabled Change Detected Between Scans
	10527	79M Status	Multiple Shot Reclosing Enabled
	10528	79M Momentary	Multiple Shot Reclosing Enabled Change Detected Between Scans
	10529	TCM Status	Trip Coil Monitoring Enabled
	10530	TCM Momentary	Trip Coil Monitoring Enabled Change Detected Between Scans
	10531	50-1 Status	Enable 50P-1 and 50N-1
	10532	50-1 Momentary	Enable 50P-1 and 50N-1 Change Detected Between Scans
	10533	50-2 Status	Enable 50P-2 and 50N-2
	10534	50-2 Momentary	Enable 50P-2 and 50N-2 Change Detected Between Scans
	10535	50-3 Status	Enable 50P-3 and 50N-3
	10536	50-3 Momentary	Enable 50P-3 and 50N-3 Change Detected Between Scans
	10537	ALT1 Status	Enable Alternate 1 Settings
	10538	ALT1 Momentary	Enable Alternate 1 Settings Change Detected Between Scans
	10539	ALT2 Status	Enable Alternate 2 Settings
	10540	ALT2 Momentary	Enable Alternate 2 Settings Change Detected Between Scans
	10541	ECI1 Status	Initiate Event Capture 1

	Register Address	Item	Description
	10542	ECI1 Momentary	Initiate Event Capture 1 Change Detected Between Scans
	10543	ECI2 Status	Initiate Event Capture 2
	10544	ECI2 Momentary	Initiate Event Capture 2 Change Detected Between Scans
	10545	WCI Status	Waveform Capture Initiate
	10546	WCI Momentary	Waveform Capture Initiate Change Detected Between Scans
	10547	ZSC Status	Enable Zone Sequence Coordination
	10548	ZSC Momentary	Enable Zone Sequence Coordination Change Detected Between Scans
	10549	OPEN Status	Initiate Trip Output
	10550	OPEN Momentary	Initiate Trip Output Change Detected Between Scans
	10551	CLOSE Status	Initiate Close Output
	10552	CLOSE Momentary	Initiate Close Output Change Detected Between Scans
	10553	46 Status	Enable Negative Sequence Time Overcurrent Function
	10554	46 Momentary	Enable Negative Sequence Time Overcurrent Function Change Detected Between Scans
&&	10555	67P Status	Enable Positive Sequence Directionally Controlled Phase Time Overcurrent Function
&&	10556	67P Momentary	Enable Positive Sequence Directionally Controlled Phase Time Overcurrent Function Change Detected Between Scans
&&	10557	67N Status	Enable Negative Sequence Directrionally Controlled Phase Time Overcurrent Function
&&	10559	67N Momentary	Enable Negative Sequence Directrionally Controlled Phase Time Overcurrent Function Change Detected Between Scans
&&	10560	ULI1 Status	User Logical Input 1 Element Energized
&&	10561	ULI1 Momentary	User Logical Input 1 Element Energized Change Detected Between Scans
&&	10562	ULI2 Status	User Logical Input 2 Element Energized
&&	10563	ULI2 Momentary	User Logical Input 2 Element Energized Change Detected Between Scans
&&	10564	ULI3 Status	User Logical Input 3 Element Energized
&&	10565	ULI3 Momentary	User Logical Input 3 Element Energized Change Detected Between Scans
&&	10566	ULI4 Status	User Logical Input 4 Element Energized
&&	10567	ULI4 Momentary	User Logical Input 4 Element Energized Change Detected Between Scans
&&	10568	ULI5 Status	User Logical Input 5 Element Energized
&&	10569	ULI5 Momentary	User Logical Input 5 Element Energized Change Detected Between Scans
&&	10570	ULI6 Status	User Logical Input 6 Element Energized
&&	10571	ULI6 Momentary	User Logical Input 6 Element Energized Change Detected Between Scans
&&	10572	ULI7 Status	User Logical Input 7 Element Energized
&&	10573	ULI7 Momentary	User Logical Input 7 Element Energized Change Detected Between Scans
&&	10574	ULI8 Status	User Logical Input 8 Element Energized
&&	10575	ULI8 Momentary	User Logical Input 8 Element Energized Change Detected Between Scans
&&	10576	ULI9 Status	User Logical Input 9 Element Energized
&&	10577	ULI9 Momentary	User Logical Input 9 Element Energized Change Detected Between Scans
	10578	CRI Status	Reclose and Overcurrent Counters Cleared
	10579	CRI Momentary	Reclose and Overcurrent Counters Cleared Change Detected Between Scans
	10580	ARCI Status	Automatic Reclose Inhibit Enabled

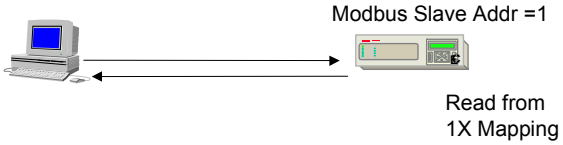
	Register Address	Item	Description
	10581	ARCI Momentary	Automatic Reclose Inhibit Enabled Change Detected Between Scans
	10582	TARC Status	Initiate Trip and Auto Reclose Function
	10583	TARC Momentary	Initiate Trip and Auto Reclose Function Change Detected Between Scans
	10584	SEF TC Status	Sensitive Earth Fault Enabled
	10585	SEF TC Momentary	Sensitive Earth Fault Enabled Change Detected Between Scans
	10586	ExtBFI Status	External Starter Input Intiated
	10587	ExtBFI Momentary	External Starter Input Intiated Change Detected Between Scans
	10588	BFI Status	Breaker Fail Initiate
	10589	BFI Momentary	Breaker Fail Initiate Change Detected Between Scans
	10590	UDI Status	User Defined Input
	10591	UDI Momentary	User Defined Inpu Change Detected Between Scans
&&	10592	25 Status	Sync Check Enable
&&	10593	25 Momentary	Sync Check Enable Change Detected Between Scans
&&	10594	25 Bypass Status	Sync Check Bypass
&&	10595	25 Bypass Momentary	Sync Check Bypass Change Detected Between Scans
%%	10596	Local Enable Status	Local Control Enabled
%%	10597	Local Enable Momentary	Local Control Enabled Change Detected Between Scans
%%	10598	SIA	Seal In Alarm
%%	10599	SIA Momentary	Seal In Alarm Momentary
*	10600	LIS1	Latched Input 1 Set
*	10601	LIS1 Momentary	Latchedl Input 1 Set Momentary
*	10602	LIS2	Latched Input 2 Set
*	10603	LIS2 Momentary	Latchedl Input 2 Set Momentary
*	10604	LIS3	Latched Input 3 Set
*	10605	LIS3 Momentary	Latched Input 3 Set Momentary
*	10606	LIS4	Latched Input 4 Set
*	10607	LIS4 Momentary	Latched Input 4 Set Momentary
*	10608	LIS5	Latched Input 5 Set
*	10609	LIS5 Momentary	Latched Input 5 Set Momentary
*	10610	LIS6	Latched Input 6 Set
*	10611	LIS6 Momentary	Latched Input 6 Set Momentary
*	10612	LIS7	Latched Input 7 Set
*	10613	LIS7 Momentary	Latched Input 7 Set Momentary
*	10614	LIS8	Latched Input 8 Set
*	10615	LIS8 Momentary	Latched Input 8 Set Momentary
*	10616	LIR1	Latched Input 1 Reset
*	10617	LIR1 Momentary	Latched Input 1 Reset Momentary
*	10618	LIR2	Latched Input 2 Reset
*	10619	LIR2 Momentary	Latched Input 2 Reset Momentary
*	10620	LIR3	Latched Input 3 Reset
*	10621	LIR3 Momentary	Latched Input 3 Reset Momentary
*	10622	LIR4	Latched Input 4 Reset
*	10623	LIR4 Momentary	Latched Input 4 Reset Momentary
*	10624	LIR5	Latched Input 5 Reset
*	10625	LIR5 Momentary	Latched Input 5 Reset Momentary
*	10626	LIR6	Latched Input 6 Reset
*	10627	LIR6 Momentary	Latched Input 6 Reset Momentary
*	10628	LIR7	Latched Input 7 Reset
*	10629	LIR7 Momentary	Latched Input 7 Reset Momentary
*	10630	LIR8	Latched Input 8 Reset

	Register Address	Item	Description
*	10632	LIR8 Momentary	Latched Input 8 Reset Momentary
*	10633	TR_SET	Tagging Relay Set
*	10634	TR_SET Momentary	Tagging Relay Set Momentary
*	10635	TR_RST	Tagging Relay Reset
*	10636	TR_RST Momentary	Tagging Relay Reset Momentary
&	10637:	ULI10	User Logical Input 10 Status
&	10638:	ULI10 Momentary	Momentary Status
&	10639:	ULI11	User Logical Input 11 Status
&	10640:	ULI11 Momentary	Momentary Status
&	10641:	ULI12	User Logical Input 12 Status
&	10642:	ULI12 Momentary	Momentary Status
&	10643:	ULI13	User Logical Input 13 Status
&	10644:	ULI13 Momentary	Momentary Status
&	10645:	ULI14	User Logical Input 14 Status
&	10646:	ULI14 Momentary	Momentary Status
&	10647:	ULI15	User Logical Input 15 Status
&	10648:	ULI15 Momentary	Momentary Status
&	10649:	ULI16	User Logical Input 16 Status
&	10650:	ULI16 Momentary	Momentary Status
&	10651:	46A	Negative Sequence Time Overcurrent Trip
&	10652:	46A Momentary	Momentary Status
**	10653:	SWSET	Switch Set Test Status
**	10654:	SWSET Momentary	Switch Set Test Momentary Status
**	10655:	SHIFTA	Test Shift Register A Input Status
**	10656:	SHIFTA Momentary	Test Shift Register A Input Momentary Status
**	10657:	SHIFTB	Test Shift Register B Input Status
**	10658:	SHIFTB Momentary	Test Shift Register B Input Momentary Status
			%%= CPU Firmware 1.92 Required && = Excluded in DPU1500R Unit * = CPU Firmware Version 4.10 or Greater and DPU 2000R Only & = CPU Version 5.20 or later ** = CPU Version 6.00 or later.

Application Example: Obtain the Breaker Status from DP2000/2000R Address 1. The relay status is available from inputs 10513 through 10156 using Momentary Change Detect Bits. Figures 7-3 and 7-4 illustrate the polling sequence and raw data returned over the network utilizing function code 02 using Momentary change detect notification.

Function 02 - Read Input Status

Example - Read Breaker Status 52a and 52b.
Although only 4 data bits are needed, 16 shall be read.

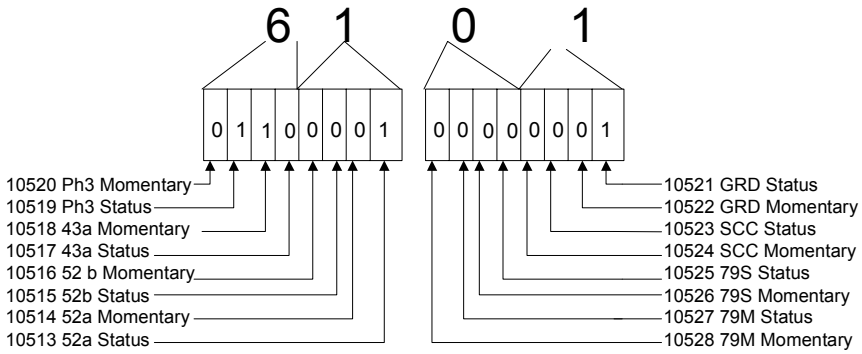


Host Sends : 01 02 02 00 00 10 78 7E Modbus RTU Mode Used
Node Addr = 01
Function = 02
Data Address = 512 (which is 513 [Modbus is offset by 1] in hex =0200)
Amount of Data Requested = 16 Inputs
CRC-16 Checksum = 78 7E
Relay Responds: 01 02 02 61 01 51 E8
Addr = 01
Function = 02
Data Bytes Received = 2
Data Received = 61 01
CRC - 16 Checksum = 51 E8

Figure 7-3. Read Input Breaker Status Example

Function 02- Read Input Status

Example - Analysis of Data Received



RESULT : Reclosing has changed status twice between scans.(43a) It is now Disabled GRD and PH3 is Enabled (Phase and Ground Overcurrent) and has not changed twice between scans. The breaker is open and it has not changed twice between scans. 79M, SCC, and 79S are disabled and have not changed twice between scans.

Figure 7-4. Decode of Raw Data Bits as seen on Data Scope Analyser

Physical Input Momentary Change Detect (32 Elements Defined)

Physical inputs are mappable for various functional inputs. One must take care since the address map designations change depending upon whether the product is a DPU2000R, DPU2000 or DPU1500R. Their status is available at the following addresses as illustrated in Table 7-5. The status information is similar to that presented in Table 7-2, however momentary status is provided in this block.

Table 7-5. Physical Input Momentary Change Detect Register Map

	Address	Item	Description
	11025	Reserved	Reserved
	11026	Reserved	Reserved
	11027	Reserved	Reserved
	11028	Reserved	Reserved
	11029	Reserved	Reserved
	11030	Reserved	Reserved
	11031	Reserved	Reserved
	11032	Reserved	Reserved
	11033	Reserved	Reserved
	11034	Reserved	Reserved
	11035	IN8 (2000R)/IN6 (1500R) Status	Physical Input 6 Status for 1500R Physical Input 8 Status for 2000R
R	11036	IN8 (2000R)/IN6 (1500R) Momentary	Physical Input 6 Status for 1500R Physical Input 8 Status for 2000R Change Detect Between Host Scan
R	11037	IN7 Status	Physical Input 7 Status
R	11038	IN7 Momentary	Physical Input 7 Change Detect Between Host Scan
R	11039	IN6 Status	Physical Input 6 Status
R	11040	IN6 (DPU2000R) Momentary	Physical Input 6 Change Detect Between Host Scan
	11041	IN5 Status	Physical Input 5 Status
	11042	IN5 Momentary	Physical Input 5 Change Detect Between Host Scan
	11043	IN4 Status	Physical Input 4 Status
	11044	IN4 Momentary	Physical Input 4 Change Detect Between Host Scan
	11045	IN3 Status	Physical Input 3 Status
	11046	IN3 Momentary	Physical Input 3 Change Detect Between Host Scan
	11047	IN2 Status	Physical Input 2 Status
	11048	IN2 Momentary	Physical Input 2 Change Detect Between Host Scan
	11049	IN1 Status	Physical Input 1 Status
	11050	IN1 Momentary	Physical Input 1 Change Detect Between Host Scan
R	11051	43a Status	Reclosing Enabled
R	11052	43a Momentary	Status Reclosing Enabled Change Detect Between Host Scan
R	11053	52b Status	Breaker Status
R	11054	52b Momentary	Breaker Status Change Detect Between Host Scan
R	11055	52a Status	Breaker Status
R	11056	52a Momentary	Breaker Status Change Detect Between Host Scan
	R=DPU2000R Only (Reserved on DPU2000)		

Section 8 - 4X Register Read Capabilities

The DPU2000/1500R/2000R implementation of 4X Registers allow for both status reads and in limited cases for control register writes. Many host devices do not allow the access of data from discrete data types (such as 0X and 1X discrete output and input function codes). The Modbus implementation within the DPU2000/1500R/2000R relay allows for Modbus commands 03, 16 (10 hex) and 23 (17 hex) register commands. Real time relay status is available for the following relay data types and functionality:

- Relay Status
- Diagnostic Status
- Unit Information
- CT and PT Information
- Physical Input Status
- Logical Input Status
- Physical Output Status
- Logical Output Status
- Load Metering Data
- Demand Metering Data
- Master Trip Functionality
- Fault Record Buffering (1- 32)
- Event Record Buffering (1- 128)
- Breaker Counter Operation Retrieval
- Force of Physical Outputs
- Breaker Control Functions over the network
- Reset of Counter, Event Buffer, Operational Buffer, Seal In and Target information

Each function code and data type shall be explained in detail, within the following sections.

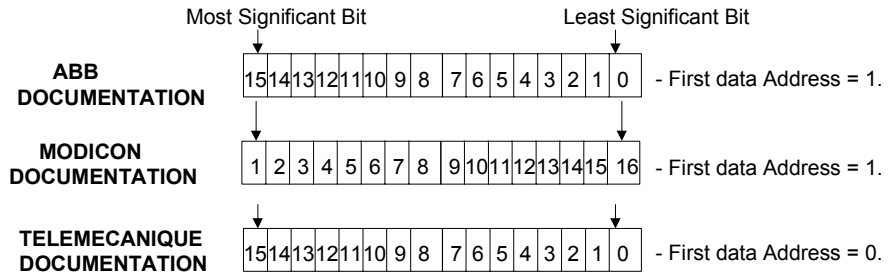
Modbus protocol allows a variety of information to be placed within the 4X Register types. The interpretation of the returned data is key to data received in the request. Modbus protocol is predicated upon register information being returned. A register is 2 bytes, or 16 bits which translates into one word. Multiple words may be combined to form a longer word which allows a larger read to obtained from the DPU2000/1500R/2000R. The DPU2000/1500R/2000R supports the following data return types for 4X formats:

- Unsigned - 16 bits - 2 bytes - Range 0 to + 65,535
- Signed - 16 bits - 2 bytes - Range –32,768 to 32,767
- Unsigned Long - 32 bits - 4 bytes - Range 0 to +4,294,967,295
- Signed Long - 32 bits - 4 bytes - Range -2,147,483,648 to +2,147,483,647
- ASCII - 16 bits - 2 bytes - 2 characters per register (Reference Appendix B)

The tables contained within this document reference the above definitions and give the cadence of bytes or words as:

- MSB Most Significant Byte
- LSB Least Significant Byte
- MSW Most Significant Word
- LSW Least Significant Word
- Msb Most signficant bit
- Lsb Least significant bit

One must take particular note when interpreting the data bits returned from the IED. Different manufacturers input data from Modbus devices however, each manufacturer starts its address start addresses taking into account the zero offset whereas, other manufacturers do not. Some manufacturers number their data bit presentations in the registers differently. Figure 8-1 illustrates the register decoding differences.



For Example: If a Telemechanique PLC was serving as a Modbus host, the ABB documentation for bit interpretation most significant bit = bit 15 leftmost bit, least significant bit = bit 0 rightmost bit. However, to access a register the host would need to subtract the value of 1 from the data address to obtain the correct data.

If a Modicon PLC was serving as a Modbus host, the ABB documentation would need to be transposed to acknowledge that any data analyzed by the host in the bit 16 position would reflect the status described as Bit 0 lsb nomenclature. No data address offset would need to be performed to obtain the correct information from the protective relay.

Figure 8-1. Vendor Documentation Translation Example

Function Code 03 – Read Holding Registers (Read Only)

The 4x frame sequence is illustrated in Figure 8-2 for Function 03 (Read Holding Registers). The Host sends the protocol request and the DPU2000/1500R/2000R responds. The host decodes the data requested dependent upon the definition of the register data. The reader should note that Modbus ASCII denotes a Colon (:) and Carriage Return/Line Feed combination for Start of Message and End Of Message designators. Modbus RTU designates 3 character delays for a Start of Message and End Of Message designator. Tables 8-1 through 8-11 list the register mapping for Modbus reads. Access of Momentary data access is not available through 4X reads.

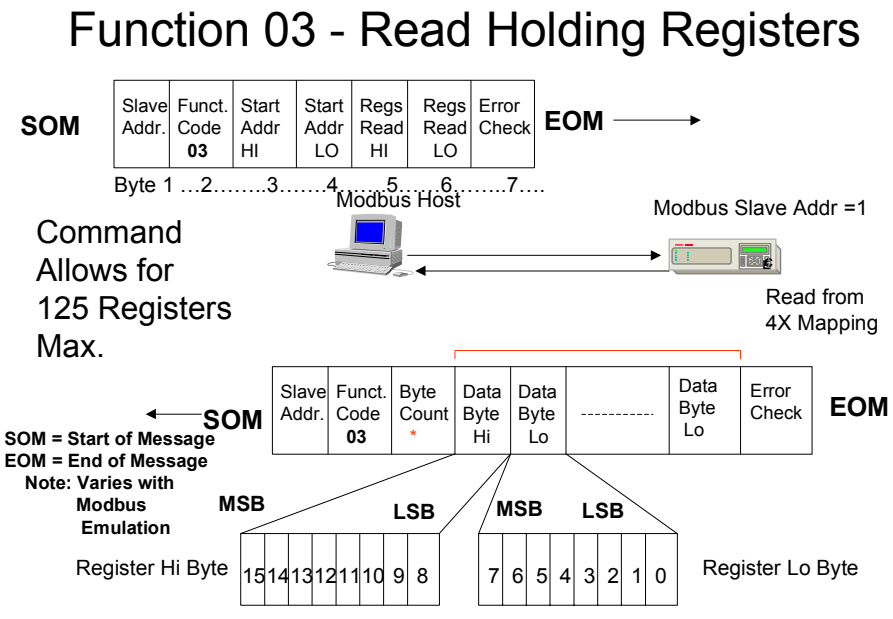


Figure 8-2. 4X Data Read Frame Format

Relay Status (1 Register Defined)

Bit 0 shall update if the unit has failed Self Test. Bit 1 (Lsb) through Bit 4, Bit 9 and 10, shall update to a 1 if any of the corresponding data to the bit group changes. The Bits shall reset when the register is polled by the host.

Bits 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 and 11, update the status real time indicates the state of the bit defined DPU2000/1500R/2000R relay feature.

If Bit 2 is enabled, then 6X Register parameterization data has been changed through the front panel of the DPU2000/1500R/2000R. In an automation application, a read of this register allows for quick determination of which data to access for immediate display. The Bits are reset when read by the host. Table 8-1 lists the bit mapping for the relay status register.

The Relay Status register is especially valuable in that if an DPU2000/1500R/2000R value has changed, it may be determined via a read of Register 40129. Once the Relay Status register has been accessed by the host, all bits in Register 40129 will be reset by the relay. The status shall then be refreshed by the DPU2000/1500R/2000R until the next host read of Register 40129. Once the status change has been detected by the host, specific registers further detailing the status change may be accessed by the host.

Table 8-1. Relay Status Modbus Address Map Definition

Register Address	Item	Description
40129	Relay Status	Unsigned 16 bit
	Bit 0 Self Test (Lsb)	Self Test In Progress
	Bit 1 Contact Input Changed	Input Transitioned
	Bit 2 Local Settings Changed	Settings Changed
	Bit 3 Remote Edit Disabled	Edit Via Network Enabled
	Bit 4 Alternate Settings 1 Active	Alternate Setting Group 1 Enabled
	Bit 5 Alternate Settings 2 Active	Alternate Setting Group 2 Enabled
	Bit 6 New Fault Record	New Fault Record In Buffer
	Bit 7 Control Power Cycled	Unit Power Cycled
	Bit 8 New Operation Recorded	New Operation Record in Buffer
	Bit 9 New Peak Demand Recorded	New Peak Demand In Buffer
	Bit 10 New Minimum Demand Value	New Minimum Demand In Bufferl
	Bit 11 Momentary Change	Momentary Change Detect Sensed
	Bit 12 Reserved	
	Bit 13 Reserved	
	Bit 14 Reserved	
	Bit 15 Reserved (Msb)	

Application Example: A Modbus Host is able to parse data in a bit format which it access through the network. The host is required to monitor a DPU2000/1500R/2000R for new fault and event records. What command should be sent to an DPU2000/1500R/2000R to gather the information.

Figures 8-3 and 8-4 illustrate data strings sent to the DPU2000/1500R/2000R to determine if a new event or operation record has been stored.

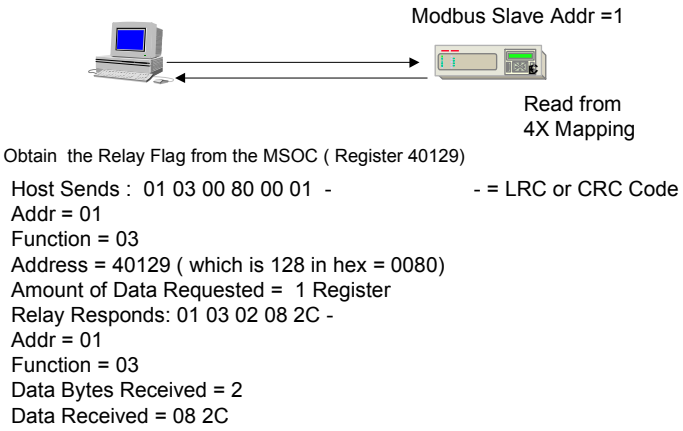


Figure 8-3. Application Example: Fetch Relay Status from the DPU2000/1500R/2000R

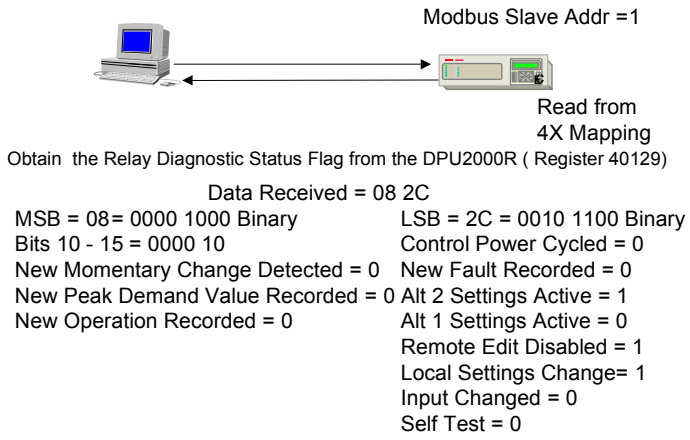


Figure 8-4. Application Example: Returned Relay Response

Since the last read of the status register, a new fault record and event record has been input within the DPU2000/1500R/2000R buffers. The recloser function (43A) is disabled. Communication is enabled through the RS232 front panel port. The host may then access additional status such as Fault or Event Records contained within the relay.

Diagnostic Status (2 Registers Defined)

Bits 0, 1, or 2 are updated continuously. The DPU2000/1500R/2000R performs diagnostics:

- Upon power-up of the unit.
- Continuously thereafter on a periodic basis. A variety of DPU2000/1500R/2000R diagnostics are performed and completed in 20 minute intervals.

If a “SELF TEST” failure is reported in Register 40129 Bit 0 or discrete output 0007, access of Register 40129 shall enable the user to access the cause. Diagnostic Status is reported via MMI front panel or Network port access.

Bit 3 Reflects the OR’ing of all EEPROM Settings stored. (ie if one fails[bit 0, 1, or 2 is set to a 1] this is set. Within the DPU2000/1500R/2000R are three relay parameter copies. Upon power-up, the copies are compared to each other. If there is a miscompute, an DPU2000/1500R/2000R PROM Failure is logged. Bit 3 is set when the unit failures to successfully read from all three copies of the Stored Parameters.

Bits 0 through 3 are cleared only at a unit Power On Reset, or a unit DPU2000/1500R/2000R reset through the front panel.

IMPLEMENTATION TIP: Front Panel reset is accomplished by pressing the “C”, “E”, and “UP”arrow keys simultaneously on the Front MMI Panel of the DPU2000/2000R.

The bit shall indicate 1 for diagnostic failure indication. These bits show the status.

Table 8-2. Diagnostic Status Modbus Address Map Definition

Register Address	Item	Description
40130	Main CPU Diag. Status Bit 15: DSP COP FAILURE (msb) Bit 14: DSP +5V FAILURE Bit 13: DSP +/-15V FAILURE Bit 12: DSP +/-5V FAILURE Bit 11: DSP ADC FAILURE Bit 10: DSP EXT RAM FAILURE Bit 9: DSP INT RAM FAILURE Bit 8: DSP ROM FAILURE Bit 7: Spare Bit 6: Spare Bit 5: Spare Bit 4: Spare Bit 3: CPU EEPROM FAILURE Bit 2: CPU NVRAM FAILURE Bit 1: CPU EPROM FAILURE Bit 0: CPU RAM FAILURE (lsb)	Unsigned 16 Bit Digital Signal Processor Failure Digital Signal Process Pwr Supply Fail Digital Signal Process Pwr Supply Fail Digital Signal Process Pwr Supply Fail Analog/Digital Converter Fail Digital Signal Process Pipeline Fail Digital Signal Process RAM Fail Digital Signal Process ROM Fail Reserved Reserved Reserved Reserved EEPROM Checksum fail on Refresh Non-Volatile RAM Failure Checksum Failure on EPROM Main CPU RAM FAILURE
40131	Bit 0 Reserved (Lsb) Bit 1 Reserved Bit 2 Reserved Bit 3 Reserved Bit 4 Reserved Bit 5 Reserved Bit 6 Reserved Bit 7 Reserved Bit 8 Heartbeat Low Bit Bit 9 Heartbeat Bit 10 Heartbeat Bit 11 Heartbeat Bit 12 Heartbeat Bit 13 Heartbeat Bit 14 Heartbeat Bit 15 Heartbeat Hi Bit (Msb)	The upper byte of this word updates every second indicating that the unit is alive. A host may monitor this register to determine if the unit is online.

Unit Information (15 Registers Defined)

Unit information status allows retrieval of DPU2000/1500R/2000R Executive firmware revision numbers, DPU2000/1500R/2000R Catalog numbers as well as DPU2000/1500R/2000R Unit Serial numbers. The DPU2000/1500R/2000R has the use of only one communication port, access of Register 40143 allows a remote host to determine which port is designated for use. Two of the registers within the unit information block are scaled, 40140 and 40141. The returned unsigned 16 bit data values when divided by 100 will mirror the revision numbers as seen on the front LCD panel within the Unit Information Menu of the DPU2000/1500R/2000R. These are the only scaled registers within this block of 4X Registers available for read. Table 8-3 further defines the Unit Information status block.

Table 8-3. Unit Information Status Modbus Address Map Definition

Register Address	Item	Description
40132	Relay Configuration Bit 0 PT Configuration Bit 1 Power Unit Reporting Bit 2 Reserved Bit 3 Reserved Bit 4 Reserved Bit 5 Reserved Bit 6 Reserved Bit 7 Reserved Bit 8 Reserved Bit 9 Reserved Bit 10 Reserved Bit 11 Reserved Bit 12 Reserved Bit 13 Reserved Bit 14 Reserved Bit 15 Reserved (Msb)	Unsigned Integer 0 = Delta 1 = Wye PT Config. 0 = Kwatt/KVar 1 = Mwatt/ Mvar Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
40133	Catalog Number (MSW)	ASCII – 2 Characters Leftmost Digits
40134	Catalog Number	ASCII – 2 Characters
40135	Catalog Number	ASCII – 2 Characters
40136	Catalog Number	ASCII – 2 Characters
40137	Catalog Number	ASCII – 2 Characters
40138	Catalog Number	ASCII – 2 Characters
40139	Catalog Number	ASCII – 2 Characters
40138	Catalog Number	ASCII – 2 Characters
40139	Catalog Number	ASCII – 2 Characters
40142	Catalog Number (LSW)	ASCII – 2 Characters Rightmost Digits
40143	Main CPU Sw Version Number	Unsigned 16 Bit – (Scale Factor 100)
40144	Analog DSP Sw Version Number	Unsigned 16 Bit – (Scale Factor 10)
40145	Front Panel Controller Sw Version Number	Unsigned 16 Bit – (Scale Factor 10)
40146	Communication Sw Version Number	Unsigned 16 Bit – (Scale Factor 10)
40147	Unit Serial Number (MSW)	Unsigned Long 32 Bit (Most Significant Word - 16 Bits)
40148	Unit Serial Number (LSW)	Unsigned Long 32 Bit (Least Significant Word - 16 Bits)
40149	Unit Name (Most Significant Digits)	ASCII – 2 Characters (Leftmost Digits)
40150	Unit Name	ASCII – 2 Characters
40151	Unit Name	ASCII – 2 Characters
40152	Unit Name	ASCII – 2 Characters
40153	Unit Name	ASCII – 2 Characters
40154	Unit Name	ASCII – 2 Characters
40155	Unit Name	ASCII – 2 Characters
40156	Unit Name	ASCII – 2 Characters
40157	Unit Name (Least Significant Digits)	ASCII – 2 Characters (Rightmost Digits)

Read Quick Status (3 Registers Defined)

CT and PT ratio configuration data is available. As standard, The CT ratio is to 1as is the Neutral and PT ratios are to 1. Quick status registers are illustrated in Table 8-4.

Table 8-4. Quick Status Modbus Address Map Definition

Register Address	Item	Description
40158	Phase CT Ratio	Unsigned 16 Bit
40159	Neutral Ratio	Unsigned 16 Bit
40160	PT Ratio	Unsigned 16 Bit

Power Fail Status Information (9 Registers Defined)

If the DPU2000, DPU1500R or DPU2000R loses power, the unit has the capability to sense power is being lost. During this shutdown time, the unit stores the timestamp of power fail occurrence. The storage format is shown in Table 8-5.

Table 8-5. Power Fail Table Register Definition

Address	Item	Description
40161	Power Fail Timestamp Year	Unsigned Integer 16 Bits 1900<=Range<= 2100
40162	Power Fail Timestamp Month	Unsigned Integer 16 Bits 1<=Range<=12
40163	Power Fail Timestamp Day	Unsigned Integer 16 Bits 1<=Range<=31
40164	Power Fail Timestamp Hours	Unsigned Integer 16 Bits 0<=Range<=23
40165	Power Fail Timestamp Minutes	Unsigned Integer 16 Bits 0<=Range<=59
40166	Power Fail Timestamp Seconds	Unsigned Integer 16 Bits 0<=Range<=59
40167	Power Fail Timestamp Hundreths of Seconds	Unsigned Integer 16 Bits 0<=Range<99
40168	Power Fail Timestamp Fail Type	Unsigned Integer 16 Bits 1 = DC
40169	Power Fail Timestamp Machine State	Unsigned Integer 16 Bits 0 = Circuit Breaker Closed 1 = Picked Up 2 = Circuit Breaker Tripping 3 = Circuit Breaker Failed to Open 4 = Circuit Breaker Open 6 = Circuit Breaker Open 7 = Circuit Breaker Failed to Open 8 = Control Switch Trip Fail 9 = Circuit Breaker State Unknown

Fast Status (2 Registers Defined)

Fast Status is available for an operator interface to determine the device queried. The Division Code for the DPU 2000/1500R/2000R is 1A HEX, the product ID for the DPU2000/1500R/2000R is 0E HEX.

One should also notice that the reporting of a new operation record is reported here in word 40170 in bit position 9. The bit is reset whenever the word is accessed via a network read.

Table 8-6. Fast Status Modbus Address Map Definition

Register Address	Item		Description
40170	Fast Status		Unsigned 16 Bit
	Bit 0 – 5	Division Code (Lsb)	00 0101 = 07 HEX
	Bit 6	Reserved	Reserved
	Bit 7	Reserved	Reserved
	Bit 8	Reserved	Reserved
	Bit 9	Unreported Operation Record	1 = Unreported Record
	Bit 10 – 15	Reserved	Reserved
40171	Fast Status		Unsigned Integer 16 Bit
	Bit 0 – 5	Reserved (Lsb)	Reserved
	Bit 6	Reserved	Reserved
	Bit 7	Reserved	Reserved
	Bit 8	Reserved	Reserved
	Bit 9	Reserved	Reserved
	Bit 10 – 15	Product ID (Msb)	00 1110 = 0E HEX left justified

Communication Event Log (8 Registers Defined)

Whenever a communication error occurs, the DPU2000/1500R/DPU 2000R generates an exception response to the rejected command. Registers 40172 through 40179 contains information on the last communication error experienced via the front communication port, rear INCOM port or the RS232/485 ports resident on the relay's communication card. Table 8-7 lists the register definition for the event log.

Table 8-7. Communication Error Event Log

Address	Item	Definitiion
40172	Last Comm Port Error	Unsigned Integer 0 = Modbus Plus (Type 6 or 7 Card Only DPU2000R) 1 = INCOM 2 = RS232 3 = RS485
40173	Last Comm Error Command	Unsigned Integer/Word Byte Decode If Modbus or Modbus Plus, register contains Modbus Command. If INCOM or Standard Ten Byte, register contains Command + Subcommand in upper lower byte decode.
40174	Last Comm Error Register Request	Unsigned Integer Last Requested Address on Comm error read/write request.
40175	Last Comm Error Type	Unsigned Integer 1 = Invalid Password 2 = Checksum Error 3 = Block/Register Range Invalid 4 = Block/Register attempted to be accessed invalid 5 = Range of data attempted to be accessed invalid 6 = Invalid Data 7 = Settings being edited elsewhere in unit or remote edit disabled 8 = A write to one setting group attempted while actively editing another 9 = Breaker State Invalid 10 = Data entered is below minimum value 11 = Data entered is above maximum allowed 12 = Data entered is out of step 32 = Reference Type or File Number Invalid 33 = Too many registers for Modbus Protocol 34 = Invalid Function Code 35 = Invalid Record Control
40176	Control Mask If Write Error	Unsigned Integer Control Mask 1 Write Mask (MSW)
40177	Control Mask If Write	Unsigned Integer

	Error	Control Mask 1 Write Mask (LSW)
40178	Control Mask If Write Error	Unsigned Integer Control Mask 2 Write Mask (MSW)
40179	Control Mask If Write Error	Unsigned Integer Control Mask 2 Write Mask (LSW)

Metering Values

Metering Values are defined Table 8-8. Various data types are associated with each element. Some values, such as Kwatts (32 Bit, 4 byte, 2 word) are signed to denote power flow. All metering values are reported in primary units and should reflect the status as shown on the DPU2000/1500R/2000R Front Panel Interface, ECP or WinECP metering screens. Other numbers are scaled, such as frequency to denote a decimal point when read. Frequency 40539 should be divided by 100 to obtain the decimal point which is visible when viewing the value from the front panel.

Table 8-8. DPU2000/DPU1500R/DPU2000R Metering Values

Register Address	Item	Description
40257	Ia Magnitude	Unsigned 16 Bit
40258	Ia Angle	Unsigned 16 Bit
40259	Ib Magnitude	Unsigned 16 Bit
40260	Ib Angle	Unsigned 16 Bit
40261	Ic Magnitude	Unsigned 16 Bit
40262	Ic Angle	Unsigned 16 Bit
40263	In Magnitude	Unsigned 16 Bit
40264	In Angle	Unsigned 16 Bit
40265	Van Magnitude	Unsigned 32 Bit High Order Word MSW
40266	Van Magnitude	Unsigned 32 Bit Low Order Word LSW
40267	Van Angle	Unsigned 16 Bit
40268	Vbn Magnitude	Unsigned 32 Bit High Order Word MSW
40269	Vbn Magnitude	Unsigned 32 Bit Low Order Word LSW
40270	Vbn Angle	Unsigned 16 Bit
40271	Vcn Magnitude	Unsigned 32 Bit High Order Word MSW
40272	Vcn Magnitude	Unsigned 32 Bit Low Order Word LSW
40273	Vcn Angle	Unsigned 16 Bit
40274	Vab Magnitude	Unsigned 32 Bit High Order Word MSW
40275	Vab Magnitude	Unsigned 32 Bit Low Order Word LSW
40276	Vab Angle	Unsigned 16 Bit
40277	Vbc Magnitude	Unsigned 32 Bit High Order Word MSW
40278	Vbc Magnitude	Unsigned 32 Bit Low Order Word LSW
40279	Vbc Angle	Unsigned 16 Bit
40280	Vca Magnitude	Unsigned 32 Bit High Order Word MSW
40281	Vca Magnitude	Unsigned 32 Bit Low Order Word LSW
40282	Vca Angle	Unsigned 16 Bit
40283	Kwatts (Phase A)	Signed 32 Bit High Order Word MSW
40284	Kwatts (Phase A)	Signed 32 Bit Low Order Word LSW
40285	Kwatts (Phase B)	Signed 32 Bit High Order Word MSW
40286	Kwatts (Phase B)	Signed 32 Bit Low Order Word LSW
40287	Kwatts (Phase C)	Signed 32 Bit High Order Word MSW
40288	Kwatts (Phase C)	Signed 32 Bit Low Order Word LSW
40289	Kwatts (Three Phase)	Signed 32 Bit High Order Word MSW
40290	Kwatts (Three Phase)	Signed 32 Bit Low Order Word LSW
40291	Kvars (Phase A)	Signed 32 Bit High Order Word MSW
40292	Kvars (Phase A)	Signed 32 Bit Low Order Word LSW
40293	Kvars (Phase B)	Signed 32 Bit High Order Word MSW
40294	Kvars (Phase B)	Signed 32 Bit Low Order Word LSW
40295	Kvars (Phase C)	Signed 32 Bit High Order Word MSW

Register Address	Item	Description
40296	Kvars (Phase C)	Signed 32 Bit Low Order Word LSW
40297	Kvars (Three Phase)	Signed 32 Bit High Order Word MSW
40298	Kvars (Three Phase)	Signed 32 Bit Low Order Word LSW
40299	Kwatt Hours (Phase A)	Signed 32 Bit High Order Word MSW
40300	Kwatt Hours (Phase A)	Signed 32 Bit Low Order Word LSW
40301	Kwatt Hours (Phase B)	Signed 32 Bit High Order Word MSW
40302	Kwatt Hours (Phase B)	Signed 32 Bit Low Order Word LSW
40303	Kwatt Hours (Phase C)	Signed 32 Bit High Order Word MSW
40304	Kwatt Hours (Phase C)	Signed 32 Bit Low Order Word LSW
40305	Kwatt Hours 3 Phase	Signed 32 Bit High Order Word MSW
40306	Kwatt Hours 3 Phase	Signed 32 Bit Low Order Word LSW
40307	Kwatt Hours (Phase A)	Signed 32 Bit High Order Word MSW
40308	Kwatt Hours (Phase A)	Signed 32 Bit Low Order Word LSW
40309	Kwatt Hours (Phase B)	Signed 32 Bit High Order Word MSW
40310	Kwatt Hours (Phase B)	Signed 32 Bit Low Order Word LSW
40311	Kwatt Hours (Phase C)	Signed 32 Bit High Order Word MSW
40312	Kwatt Hours (Phase C)	Signed 32 Bit Low Order Word LSW
40313	KVArHrs 3 Phase	Signed 32 Bit High Order Word MSW
40314	KVArHrs 3 Phase	Signed 32 Bit Low Order Word LSW
40315	Zero Sequence Current Magnitude (Computed)	Unsigned 16 Bit
40316	Zero Sequence Current Angle (Computed)	Unsigned 16 Bit
40317	Positive Sequence Current Magnitude	Unsigned 16 Bit
40318	Positive Sequence Current Angle	Unsigned 16 Bit
40319	Negative Sequence Current Magnitude	Unsigned 16 Bit
40320	Negative Sequence Current Angle	Unsigned 16 Bit
40321	Positive Sequence Voltage Magnitude	Unsigned 32 Bit High Order Word MSW
40322	Positive Sequence Voltage Magnitude	Unsigned 32 Bit Low Order Word LSW
40323	Positive Sequence Voltage Angle	Unsigned 16 Bit
40324	Negative Sequence Voltage Magnitude	Unsigned 32 Bit High Order Word MSW
40325	Negative Sequence Voltage Magnitude	Unsigned 32 Bit Low Order Word LSW
40326	Negative Sequence Angle	Unsigned 16 Bit
40327	Frequency	Unsigned 16 Bit (Multiplier = 100)
40328	Power Factor Bit 0 = PF Bit 1 = PF Bit 2 = PF Bit 3 = PF Bit 4 = PF Bit 5 = PF Bit 6 = PF Bit 7 = Sign Bit 8 = Lead/Lag Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved	Unsigned Byte Decode Power Factor (LSByte lsb) (X 100) Power Factor Power Factor Power Factor Power Factor Power Factor Power Factor (MSByte msb) 0 = Positive 1 = Negative 0 = Leading 1 = Lagging Reserved Reserved Reserved

Register Address	Item	Description
	Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Reserved Reserved Reserved Reserved
40329	Zero Sequence Current Magnitude (Measured)	Unsigned 32 Bit High Order Word MSW
40330	Zero Sequence Current Magnitude (Measured)	Unsigned 32 Bit Low Order Word LSW
40331	Zero Sequence Current Angle (Measured)	Unsigned 16 Bit
40332	Zero Sequence Voltage Magnitude (Measured)	Unsigned 32 Bit High Order Word MSW
40333	Zero Sequence Voltage Magnitude (Measured)	Unsigned 32 Bit Low Order Word LSW
40334	Zero Sequence Voltage Angle (Measured)	Unsigned 16 Bit
40335	Power Factor Value	Signed 16 Bit (Multiplier = 100)
40336	Power Factor Direction	Unsigned 16 Bit 1=Lagging 0 = Leading
40337	Kvars 3 Phase	Unsigned 32 Bit High Order Word MSW
40338	Kvars 3 Phase	Unsigned 32 Bit Low Order Word LSW
40339	Fault Distance	Unsigned 16 Bit Integer
40340	Vbus to Vline Voltage Difference	Unsigned 32 Bit High Order Word MSW
40431	Vbus to Vline Voltage Difference	Unsigned 32 Bit Low Order Word LSW
40342	Vbus to Vline Angle Difference	Unsigned 16 Bit
40343	Synch Check Slip Frequency (Note 1)	Signed 16 Bit Integer
40344	Zero Sequence Voltage Mag (Derived) (Note 1)	Unsigned 32 Bit High Order Word MSW
40345	Zero Sequence Voltage Mag (Derived) (Note 1)	Unsigned 32 Bit Low Order Word LSW
40346	Zero Sequence Voltage Angle (Derived) (Note 1)	Unsigned 16 Bit
Note 1 – Version 3.19 Firmware or Later		

Demand Metering and Reactive Power Values (20 Registers Defined)

Demand Metering is reported within Table 8-9. The accumulated magnitudes are reported in 16 bit unsigned and 32 bit unsigned numerical values as indicated in the following table. The demands are reset by writing a reset command to the 4X Register, 41668 Bit 5. Please reference Table 8-11 of this document for the control register group and bit designation to reset this group of registers. Refer to Table 8-1 Register 40129, bit 10 which will indicate that a new Peak Demand Value has been accumulated within this table.

Demand metering is calculated on a fixed demand window accumulation. The demands are based upon a time window of 15, 30, or 60-minute calculation intervals. Refer to Table 8-13 within this document to reference the procedure for setting the sliding demand window time base.

Demand Metering initiates at time = 0 which may be a unit power up, system reset via the front panel or through a demand metering reset via the network as described in Table 8-11 of this document. It is not dependent upon the time- of-day clock (TOD) within the unit. The DPU2000/2000R has an internal timer that is monitored to determine the end of the selected interval (15, 30, or 60 minutes) and the start of the new interval.

Current (Ia, Ib, Ic, and In) and power (KW and KVAR) are calculated and integrated within the demand calculation for that interval on a 32 cycle time period interval within the demand time window selected. The following figures

illustrate the method of calculating and reporting the Demand Values depending upon reporting of current or energy.

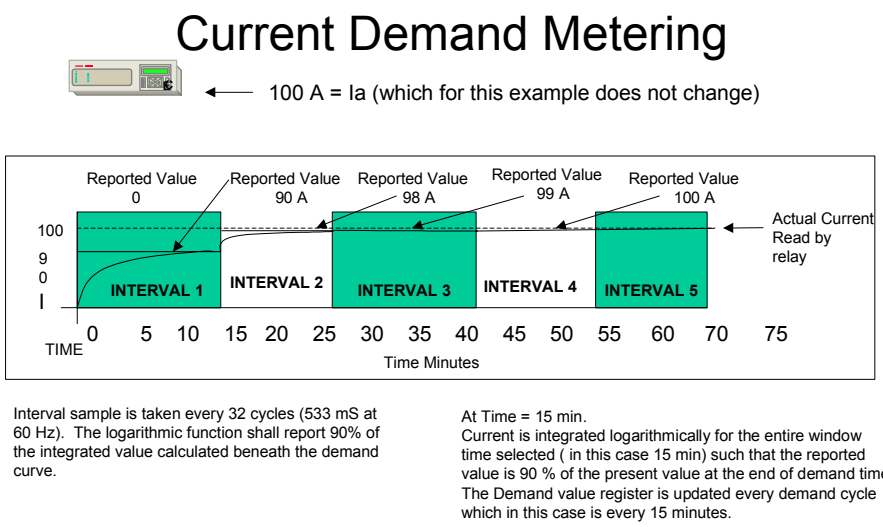


Figure 8-5. Demand Current Calculation

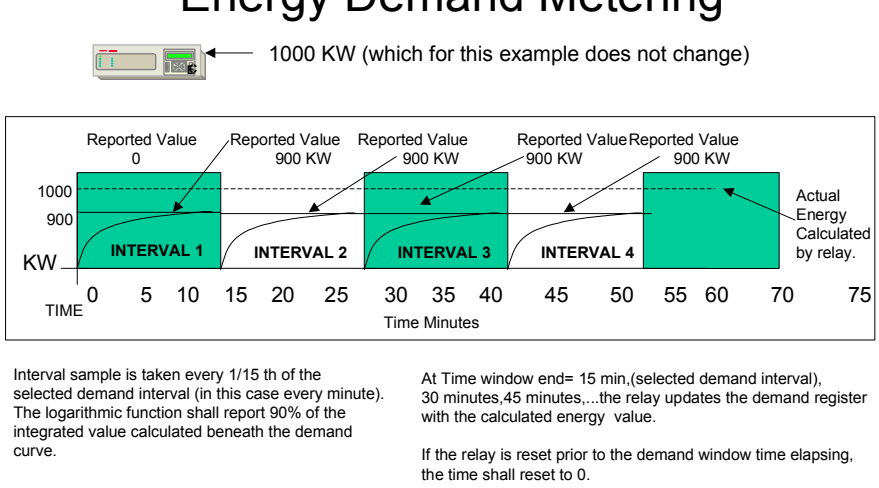


Figure 8-6. Energy Demand Calculation

Figures 8-5 and 8-6 illustrate the energy and current calculation methods and data reported when accessed via the network. To simplify the explanation, the current and energy has been kept constant. This example illustrates a calculation based upon a window size of 15 minute demand intervals.

Table 8-9. Demand Metering Modbus Address Map Definition

Register Address	Item	Description
40385	Ia Magnitude	Unsigned 16 Bit
40386	Ib Magnitude	Unsigned 16 Bit
40387	Ic Magnitude	Unsigned 16 Bit
40388	In Magnitude	Unsigned 16 Bit
40389	Kwatts Phase A	Unsigned 32 Bit High Order Word MSW
40390	Kwatts Phase A	Unsigned 32 Bit Low Order Word LSW
40391	Kwatts Phase B	Unsigned 32 Bit High Order Word MSW

40392	Kwatts Phase B	Unsigned 32 Bit Low Order Word LSW
40393	Kwatts Phase C	Unsigned 32 Bit High Order Word MSW
40394	Kwatts Phase C	Unsigned 32 Bit Low Order Word LSW
40395	Kwatts 3 Phase	Unsigned 32 Bit High Order Word MSW
40396	Kwatts 3 Phase	Unsigned 32 Bit Low Order Word LSW
40397	Kvars Phase A	Unsigned 32 Bit High Order Word MSW
40398	Kvars Phase A	Unsigned 32 Bit Low Order Word LSW
40399	Kvars Phase B	Unsigned 32 Bit High Order Word MSW
40400	Kvars Phase B	Unsigned 32 Bit Low Order Word LSW
40401	Kvars Phase C	Unsigned 32 Bit High Order Word MSW
40402	Kvars Phase C	Unsigned 32 Bit Low Order Word LSW
40403	Kvars 3 Phase	Unsigned 32 Bit High Order Word MSW
40404	Kvars 3 Phase	Unsigned 32 Bit Low Order Word LSW

Minimum and Maximum Peak Demand (48 Registers Defined)

Peak Demands are monitored and logged within the DPU2000, DPU1500R, and DPU2000R. The demands are constantly logged by the IED until reset by the operator. The reset bit is located in Register 41158 and 41159. Please reference Section 11 for the procedure to initiate Minimum and Maximum Peak Value reset. Each value is timestamped and the peak value is stored. The values are compared every 2 seconds. If the new value is greater than the previous stored value (as is the case for the peak demand) or less than the previous stored value (as is the case for the minimum demand), the old value is discarded and the new value is reported. Peak Demand and Minimum Demand definitions are defined in Tables 8-10 and 8-11. The status of the update is reflected in Bits 9 and 10 of Register 40129. Please reference the 6X Register configuration tables to configure energy demand parameterization.

Table 8-10. Peak Demand Register Map for the DPU2000R and DPU2000

Register Address	Item	Description
40513	Peak Demand Current Phase A	Unsigned Integer 16 Bits
40514	Peak Demand Current Phase A Year	Most Significant Byte 8 Bits 00<= Range <= 99
40514	Peak Demand Current Phase A Month	Least Significant Byte 8 Bits 00<= Range <= 12
40515	Peak Demand Current Phase A Day	Most Significant Byte 8 Bits 00<= Range <= 31
40515	Peak Demand Current Phase A Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40516	Peak Demand Current Phase A Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40516	Reserved Byte	Reserved
40517	Peak Demand Current Phase B	Unsigned Integer 16 Bits
40517	Peak Demand Current Phase B Year	Most Significant Byte 8 Bits 00<= Range <= 99
40518	Peak Demand Current Phase B Month	Least Significant Byte 8 Bits 00<= Range <= 12
40518	Peak Demand Current Phase B Day	Most Significant Byte 8 Bits 00<= Range <= 31
40519	Peak Demand Current Phase B Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40519	Peak Demand Current Phase B Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40520	Reserved Byte	Reserved
40521	Peak Demand Current Phase C	Unsigned Integer 16 Bits
40522	Peak Demand Current Phase C Year	Most Significant Byte 8 Bits 00<= Range <= 99

Register Address	Item	Description
40522	Peak Demand Current Phase C Month	Least Significant Byte 8 Bits 00<= Range <= 12
40523	Peak Demand Current Phase C Day	Most Significant Byte 8 Bits 00<= Range <= 31
40523	Peak Demand Current Phase C Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40524	Peak Demand Current Phase C Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40524	Reserved Byte	Reserved
40525	Peak Demand Current Neutral	Unsigned Integer 16 Bits
40526	Peak Demand Current Neutral Year	Most Significant Byte 8 Bits 00<= Range <= 99
40526	Peak Demand Current Neutral Month	Least Significant Byte 8 Bits 00<= Range <= 12
40527	Peak Demand Current Neutral Day	Most Significant Byte 8 Bits 00<= Range <= 31
40527	Peak Demand Current Neutral Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40528	Peak Demand Current Neutral Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40528	Reserved Byte	Reserved
40529	Kwatt Hours (Phase A) Peak Demand	Signed 32 Bit High Order Word MSW
40530	Kwatt Hours (Phase A) Peak Demand	Signed 32 Bit Low Order Word LSW
40531	Peak Demand Kwatt Hours (Phase A) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40531	Peak Demand Kwatt Hours (Phase A) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40532	Peak Demand Kwatt Hours (Phase A) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40532	Peak Demand Kwatt Hours (Phase A) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40533	Peak Demand Kwatt Hours (Phase A) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40533	Reserved Byte	Reserved
40534	Kwatt Hours (Phase B) Peak Demand	Signed 32 Bit High Order Word MSW
40535	Kwatt Hours (Phase B) Peak Demand	Signed 32 Bit Low Order Word LSW
40536	Peak Demand Kwatt Hours (Phase B) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40536	Peak Demand Kwatt Hours (Phase B) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40537	Peak Demand Kwatt Hours (Phase B) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40537	Peak Demand Kwatt Hours (Phase B) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40538	Peak Demand Kwatt Hours (Phase B) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40538	Reserved Byte	Reserved
40539	Kwatt Hours (Phase C) Peak Demand	Signed 32 Bit High Order Word MSW
40540	Kwatt Hours (Phase C) Peak Demand	Signed 32 Bit Low Order Word LSW
40541	Peak Demand Kwatt Hours (Phase C) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40541	Peak Demand Kwatt Hours (Phase C) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40542	Peak Demand Kwatt Hours (Phase C) Day	Most Significant Byte 8 Bits 00<= Range <= 31

Register Address	Item	Description
40542	Peak Demand Kwatt Hours (Phase C) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40543	Peak Demand Kwatt Hours (Phase C) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40543	Reserved Byte	Reserved
40544	Kwatt Hours (3 Phase) Peak Demand	Signed 32 Bit High Order Word MSW
40545	Kwatt Hours (3 Phase) Peak Demand	Signed 32 Bit Low Order Word LSW
40546	Peak Demand Kwatt Hours (3 Phase) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40546	Peak Demand Kwatt Hours (3 Phase) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40547	Peak Demand Kwatt Hours (3 Phase) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40547	Peak Demand Kwatt Hours (3 Phase) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40548	Peak Demand Kwatt Hours (3 Phase) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40548	Reserved Byte	Reserved
40549	KVAR Hours (Phase A) Peak Demand	Signed 32 Bit High Order Word MSW
40550	KVAR Hours (Phase A) Peak Demand	Signed 32 Bit Low Order Word LSW
40551	Peak Demand KVAR Hours (Phase A) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40551	Peak Demand KVAR Hours (Phase A) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40552	Peak Demand KVAR Hours (Phase A) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40552	Peak Demand KVAR Hours (Phase A) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40553	Peak Demand KVAR Hours (Phase A) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40553	Reserved Byte	Reserved
40554	KVAR Hours (Phase B) Peak Demand	Signed 32 Bit High Order Word MSW
40555	KVAR Hours (Phase B) Peak Demand	Signed 32 Bit Low Order Word LSW
40556	Peak Demand KVAR Hours (Phase B) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40556	Peak Demand KVAR Hours (Phase B) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40557	Peak Demand KVAR Hours (Phase B) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40557	Peak Demand KVAR Hours (Phase B) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40558	Peak Demand KVAR Hours (Phase B) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40558	Reserved Byte	Reserved
40559	KVAR Hours (Phase C) Peak Demand	Signed 32 Bit High Order Word MSW
40560	KVAR Hours (Phase C) Peak Demand	Signed 32 Bit Low Order Word LSW
40561	Peak Demand KVAR Hours (Phase C) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40561	Peak Demand KVAR Hours (Phase C) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40562	Peak Demand KVAR Hours (Phase C) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40562	Peak Demand KVAR Hours (Phase C) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40563	Peak Demand KVAR Hours (Phase C) Minute	Most Significant Byte 8 Bits

Register Address	Item	Description
		00<= Range <= 59
40563	Reserved Byte	Reserved
40564	KVAR Hours (3 Phase) Peak Demand	Signed 32 Bit High Order Word MSW
40565	KVAR Hours (3 Phase) Peak Demand	Signed 32 Bit Low Order Word LSW
40566	Peak Demand KVAR Hours (3 Phase) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40566	Peak Demand KVAR Hours (3 Phase) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40567	Peak Demand KVAR Hours (3 Phase) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40567	Peak Demand KVAR Hours (3 Phase) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40568	Peak Demand KVAR Hours (3 Phase) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40568	Reserved Byte	Reserved

Table 8-11. Minimum Demand Register Map for the DPU2000R and DPU2000

Register Address	Item	Description
40641	Minimum Demand Current Phase A	Unsigned Integer 16 Bits
40642	Minimum Demand Current Phase A Year	Most Significant Byte 8 Bits 00<= Range <= 99
40642	Minimum Demand Current Phase A Month	Least Significant Byte 8 Bits 00<= Range <= 12
40643	Minimum Demand Current Phase A Day	Most Significant Byte 8 Bits 00<= Range <= 31
40643	Minimum Demand Current Phase A Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40644	Minimum Demand Current Phase A Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40644	Reserved Byte	Reserved
40645	Minimum Demand Current Phase B	Unsigned Integer 16 Bits
40646	Minimum Demand Current Phase B Year	Most Significant Byte 8 Bits 00<= Range <= 99
40646	Minimum Demand Current Phase B Month	Least Significant Byte 8 Bits 00<= Range <= 12
40647	Minimum Demand Current Phase B Day	Most Significant Byte 8 Bits 00<= Range <= 31
40647	Minimum Demand Current Phase B Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40648	Minimum Demand Current Phase B Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40648	Reserved Byte	Reserved
40649	Minimum Demand Current Phase C	Unsigned Integer 16 Bits
40650	Minimum Demand Current Phase C Year	Most Significant Byte 8 Bits 00<= Range <= 99
40650	Minimum Demand Current Phase C Month	Least Significant Byte 8 Bits 00<= Range <= 12
40651	Minimum Demand Current Phase C Day	Most Significant Byte 8 Bits 00<= Range <= 31
40651	Minimum Demand Current Phase C Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40652	Minimum Demand Current Phase C Minute	Most Significant Byte 8 Bits 00<= Range <= 59

Register Address	Item	Description
40652	Reserved Byte	Reserved
40653	Minimum Demand Current Neutral	Unsigned Integer 16 Bits
40654	Minimum Demand Current Neutral Year	Most Significant Byte 8 Bits 00<= Range <= 99
40654	Minimum Demand Current Neutral Month	Least Significant Byte 8 Bits 00<= Range <= 12
40655	Minimum Demand Current Neutral Day	Most Significant Byte 8 Bits 00<= Range <= 31
40655	Minimum Demand Current Neutral Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40656	Minimum Demand Current Neutral Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40656	Reserved Byte	Reserved
40657	Kwatt Hours (Phase A) Minimum Demand	Signed 32 Bit High Order Word MSW
40658	Kwatt Hours (Phase A) Minimum Demand	Signed 32 Bit Low Order Word LSW
40659	Minimum Demand Kwatt Hours (Phase A) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40659	Minimum Demand Kwatt Hours (Phase A) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40660	Minimum Demand Kwatt Hours (Phase A) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40660	Minimum Demand Kwatt Hours (Phase A) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40661	Minimum Demand Kwatt Hours (Phase A) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40661	Reserved Byte	Reserved
40662	Kwatt Hours (Phase B) Minimum Demand	Signed 32 Bit High Order Word MSW
40663	Kwatt Hours (Phase B) Minimum Demand	Signed 32 Bit Low Order Word LSW
40664	Minimum Demand Kwatt Hours (Phase B) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40664	Minimum Demand Kwatt Hours (Phase B) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40665	Minimum Demand Kwatt Hours (Phase B) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40665	Minimum Demand Kwatt Hours (Phase B) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40666	Minimum Demand Kwatt Hours (Phase B) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40666	Reserved Byte	Reserved
40667	Kwatt Hours (Phase C) Minimum Demand	Signed 32 Bit High Order Word MSW
40668	Kwatt Hours (Phase C) Minimum Demand	Signed 32 Bit Low Order Word LSW
40669	Minimum Demand Kwatt Hours (Phase C) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40669	Minimum Demand Kwatt Hours (Phase C) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40670	Minimum Demand Kwatt Hours (Phase C) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40670	Minimum Demand Kwatt Hours (Phase C) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40671	Minimum Demand Kwatt Hours (Phase C) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40671	Reserved Byte	Reserved
40672	Kwatt Hours (3 Phase) Minimum Demand	Signed 32 Bit High Order Word MSW
40673	Kwatt Hours (3 Phase) Minimum Demand	Signed 32 Bit Low Order Word LSW

Register Address	Item	Description
40674	Minimum Demand Kwatt Hours (3 Phase) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40674	Minimum Demand Kwatt Hours (3 Phase) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40675	Minimum Demand Kwatt Hours (3 Phase) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40675	Minimum Demand Kwatt Hours (3 Phase) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40676	Minimum Demand Kwatt Hours (3 Phase) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40676	Reserved Byte	Reserved
40677	KVAR Hours (Phase A) Minimum Demand	Signed 32 Bit High Order Word MSW
40678	KVAR Hours (Phase A) Minimum Demand	Signed 32 Bit Low Order Word LSW
40679	Minimum Demand KVAR Hours (Phase A) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40679	Minimum Demand KVAR Hours (Phase A) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40680	Minimum Demand KVAR Hours (Phase A) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40680	Minimum Demand KVAR Hours (Phase A) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40681	Minimum Demand KVAR Hours (Phase A) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40681	Reserved Byte	Reserved
40682	KVAR Hours (Phase B) Minimum Demand	Signed 32 Bit High Order Word MSW
40683	KVAR Hours (Phase B) Minimum Demand	Signed 32 Bit Low Order Word LSW
40684	Minimum Demand KVAR Hours (Phase B) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40684	Minimum Demand KVAR Hours (Phase B) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40685	Minimum Demand KVAR Hours (Phase B) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40685	Minimum Demand KVAR Hours (Phase B) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40686	Minimum Demand KVAR Hours (Phase B) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40686	Reserved Byte	Reserved
40687	KVAR Hours (Phase C) Minimum Demand	Signed 32 Bit High Order Word MSW
40688	KVAR Hours (Phase C) Minimum Demand	Signed 32 Bit Low Order Word LSW
40689	Minimum Demand KVAR Hours (Phase C) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40689	Minimum Demand KVAR Hours (Phase C) Month	Least Significant Byte 8 Bits 00<= Range <= 12
40690	Minimum Demand KVAR Hours (Phase C) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40690	Minimum Demand KVAR Hours (Phase C) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40691	Minimum Demand KVAR Hours (Phase C) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40691	Reserved Byte	Reserved
40692	KVAR Hours (3 Phase) Minimum Demand	Signed 32 Bit High Order Word MSW
40693	KVAR Hours (3 Phase) Minimum Demand	Signed 32 Bit Low Order Word LSW
40694	Minimum Demand KVAR Hours (3 Phase) Year	Most Significant Byte 8 Bits 00<= Range <= 99
40694	Minimum Demand KVAR Hours	Least Significant Byte 8 Bits

Register Address	Item	Description
	(3 Phase) Month	00<= Range <= 12
40695	Minimum Demand KVAR Hours (3 Phase) Day	Most Significant Byte 8 Bits 00<= Range <= 31
40695	Minimum Demand KVAR Hours (3 Phase) Hour	Most Significant Byte 8 Bits 00<= Range <= 23
40696	Minimum Demand KVAR Hours (3 Phase) Minute	Most Significant Byte 8 Bits 00<= Range <= 59
40696	Reserved Byte	Reserved

Breaker Counters (11 Registers Defined) Modbus Function 03 Read Only

Breaker Counters allow diagnostic evaluation of operations for maintenance purposes. With Reclosing enabled (79), the counters 40776 through 40781 are updated. The DPU2000/1500R/2000R allows selection of reclosure for up to 4 shots with the fifth event initiating lockout. The Unreported Fault and Operation registers are decremented only when the faults are READ from the appropriate registers (41410 to 41452 for fault records, and 41538 through 41547). Reference the Fault Record and Operation Record data sections of this manual for an explanation of this feature. Table 8-12 defines the register map for the Breaker Counter capabilities within the unit.

Table 8-12. Breaker Counter Definition

Register Address	Item	Description
40769	Unreported Operation Counter	Unsigned Integer 16 Bits 0<=Range<=9999
40770	Unreported Fault Counter	Unsigned Integer 16 Bits 0<=Range<= 9999
40771	KSIA	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ia – Current existing when breaker opened on Phase A.
40772	KSIB 0 – 9999	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ib – Current existing when breaker opened on Phase B.
40773	KSIC 0 – 9999	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ic – Current existing when breaker opened on Phase C.
40774	Overcurrent Trip Counter	Unsigned 16 Bits 0 – 9999
40775	Total Breaker Operations	Unsigned 16 Bits 0 – 9999
40776	Recloser Counter 1	Unsigned 16 Bits 0<=Range<=9999
40777	RecLoser Counter 2	Unsigned 16 Bits 0<=Range<= 9999
40778	First Reclose Counter 0 – 9999	Unsigned 16 Bits 0 – 9999
40779	Second Reclose Counter 0 – 9999	Unsigned 16 Bits 0 – 9999
40780	Third Reclose Counter 0 – 9999	Unsigned 16 Bits 0 – 9999
40781	Fourth Reclose Counter 0 – 9999	Unsigned 16 Bits 0 – 9999

Discrete 4X Register Bit Data Reporting (26 Registers Defined)

The DPU2000 and DPU2000R offers bit status reporting via 0X and 1X Modbus/Modbus Plus command retrieval. Some hosts however do not offer the capability to read data via these data types. The data types have been structured to be reported in 4X data types. Reported data is of the following types:

- Logical Outputs
- Logical Inputs
- Physical Inputs
- Forced Physical Input State Reporting
- Forced Physical Output State Reporting
- Forced Logical Input State Reporting

The following registers only report the status of the elements. Some of the elements are latched and behave as do their 0X and 1X counterparts. The bits are reset depending upon the reset control via the 4X control registers (Reference Section 10).

Table 8-23. Logical Inputs (12 Registers - 128 Elements)

DPU2000	Address	Item	Description
	40897	Logical Output	Unsigned Integer 16 Bits
Y		Bit 15 = CLOSE	DPU is Closing Breaker (msb leftmost bit)
Y		Bit 14 = TRIP	DPU is Tripping Breaker
Y		Bit 13 = ALARM	DPU in Alarm
Y		Bit 12 = 27-1P	Single Phase Undervoltage Input Enabled
Y		Bit 11 = 46	Negative Sequence Time Overcurrent Function Enabled
Y		Bit 10 = 50P-1	Level 1 Neutral Inst. Overcurrent Function Enabled
Y		Bit 9 = 50N-1	Level 1 Phase Inst. Overcurrent Function Enabled
Y		Bit 8 = 50P-2	Level 2 Neutral Inst. Overcurrent Function Enabled
Y		Bit 7 = 50N-2	Level 2 Phase Inst. Overcurrent Function Enabled
Y		Bit 6 = 50P-3	Level 3 Neutral Inst. Overcurrent Function Enabled
Y		Bit 5 = 50N-3	Level 3 Phase Inst. Overcurrent Function Enabled
Y		Bit 4 = 51P	Time Phase Overcurrent Function Enabled
Y		Bit 3 = 51N	Time Ground Overcurrent Function Enabled
N		Bit 2 = 59	Overvoltage Element Enabled
N		Bit 1 = 67P	Pos. Seq. Dir. Phase Time Overcurrent Enabled
N		Bit 0 = 67N (lsb)	Neg. Seq. Dir. Ground Time Overcurrent Enabled (lsb rightmost bit)
	40898	Logical Output	Unsigned Integer 16 Bits
N		Bit 15 = 81S	Over Frequency Shed (msb leftmost bit)
N		Bit 14 = 81R	Over Frequency Restore
Y		Bit 13 = PATA	Phase A Target Alarm
Y		Bit 12 = PBTA	Phase B Target Alarm
Y		Bit 11 = PCTA	Phase C Target Alarm
Y		Bit 10 =TCFA	Trip Circuit Failure Alarm
Y		Bit 9 = TCC	Tap Changer Cutoff Contact (Recloser Active)
Y		Bit 8 = 79DA	Recloser Disabled Alarm
Y		Bit 7 = PUA	Pickup Alarm
Y		Bit 6 = 79LOA	Recloser Lockout Alarm
Y		Bit 5 = BFA	Breaker Fail Alarm
Y		Bit 4 = PPDA	Phase Current Demand Alarm
Y		Bit 3 = NPDA	Neutral Current Demand Alarm
Y		Bit 2 = BFUA	Blown Fuse Alarm
Y		Bit 1 = KSI	Kiloamp Summation Alarm
Y		Bit 0 = 79CA	Recloser Counter Alarm (1 or 2) (lsb rightmost bit)
	40899	Logical Output	Unsigned Integer 16 Bits
Y		Bit 15 = HPFA	High Power Factor Alarm (msb leftmost bit)
Y		Bit 14 = LPFA	Low Power Factor Alarm
Y		Bit 13 = OCTC	Overcurrent Trip Counter Energized Alarm
Y		Bit 12 = 50-1D	Phase Inst. Overcurrent Disabled Energized Alarm

DPU2000	Address	Item	Description
Y		Bit 11 = 50-2D	Phase Inst. Overcurrent Disabled Energized Alarm
Y		Bit 10 = STC	Settings Table Changed Alarm
Y		Bit 9 = ZSC	Zone Sequence Coordination Enabled Indicator
Y		Bit 8 = PH3-D	Phase Control Disabled Alarm
Y		Bit 7 = GRD-D	Ground Control Disabled Alarm
Y		Bit 6 = 32PA	Pos. Sequence Zone Phase Pickup Alarm
Y		Bit 5 = 32NA	Neg. Sequence Zone Neutral Pickup Alarm
Y		Bit 4 = 27-3P	Three Phase Undervoltage Alarm
Y		Bit 3 = VarDA	Phase Kilovar Demand Alarm
Y		Bit 2 = 79CA-2	Recloser Counter 2 Alarm
Y		Bit 1 = TRIP A	Phase A Trip Alarm
Y		Bit 0 = TRIP B	Phase B Trip Alarm (lsb rightmost bit)
	40900	Logical Output	Unsigned Integer 16 Bits
Y		Bit 15 =TRIPC	Phase C Trip Alarm (msb leftmost bit)
Y		Bit 14 = 27-1 (L)	Single Phase Undervoltage Alarm
Y		Bit 13 = 46 (L)	Neg. Seq. Time Overcurrent Trip Seal In Alarm
Y		Bit 12 = 50P-1 (L)	Phase Instantaneous Trip Seal In Level 1 Alarm
Y		Bit 11 = 50N-1 (L)	Neutral Instantaneous Trip Seal In Level 1 Alarm
Y		Bit 10 = 50P-2 (L)	Phase Instantaneous Trip Seal In Level 2 Alarm
Y		Bit 9 = 50N-2 (L)	Neutral Instantaneous Trip Seal In Level 2 Alarm
Y		Bit 8 = 50P-3 (L)	Phase Instantaneous Trip Seal In Level 3 Alarm
Y		Bit 7 = 50N-3 (L)	Neutral Instantaneous Trip Seal In Level 3 Alarm
Y		Bit 6 = 51P (L)	Phase Time Overcurrent Trip Alarm
Y		Bit 5 = 51N (L)	Neutral Time Overcurrent Trip Alarm
N		Bit 4 = 59 (L)	Single Phase Overcurrent Alarm
N		Bit 3 = 67P (L)	Pos. Sequence Supervised Dir. Time Overcurrent Trip Alarm
N		Bit 2 = 67N (L)	Neg. Sequence Supervised Dir. Time Overcurrent Trip Alarm
N		Bit 1 = 81S1 (L)	Freq. Load Shed Module 1 Activated
N		Bit 0 = 81R1 (L)	Freq. Load Restoration Module 1 Activated (lsb rightmost bit)
	40901	Logical Output	Unsigned Integer 16 Bit (msb leftmost bit)
Y		Bit 15 = 81O-1	Overfrequency Alarm Module 1 Setting Exceeded Alarm
Y		Bit 14 = 27-3P (L)	Phase Undervoltage Alarm
Y		Bit 13 = TRIP A (L)	Phase A Trip Alarm
Y		Bit 12 = TRIP B (L)	Phase B Trip Alarm
Y		Bit 11 = TRIP C (L)	Phase C Trip Alarm
N		Bit 10 = ULO 1	User Logical Output 1 Energized
N		Bit 9 = ULO 2	User Logical Output 2 Energized
N		Bit 8 = ULO 3	User Logical Output 3 Energized
N		Bit 7 = ULO 4	User Logical Output 4 Energized
N		Bit 6 = ULO 5	User Logical Output 5 Energized
N		Bit 5 = ULO 6	User Logical Output 6 Energized
N		Bit 4 = ULO 7	User Logical Output 7 Energized
N		Bit 3 = ULO 8	User Logical Output 8 Energized
N		Bit 2 = ULO 9	User Logical Output 9 Energized
Y		Bit 1 = PVArA	Positive 3 Phase Kilovar Alarm
Y		Bit 0 = NVArA	Negative 3 Phase Kilovar Alarm (lsb rightmost bit)
	40902	Logical Output	Unsigned Integer 16 Bit
Y		Bit 15 = BZA w/o SEF	Bus Zone Alarm without Sensitive Earth Fault (msb leftmost)
N		Bit 14 = SEF	Sensitive Earth Fault Alarm
N		Bit 13 = SEF **(L)**	Sensitive Earth Fault Alarm
N		Bit 12 = 79CA-2 **(L)**	Recloser Counter 2 Exceeded Alarm
N		Bit 11 = 79CA **(L)**	Recloser Counter Exceeded Alarm
N		Bit 10 = WATT 2	Positive Watt Alarm 2
N		Bit 9 = WATT 1	Positive Watt Alarm 1
N		Bit 8 = CLTA	Cold Load Timer Alarm
Y		Bit 7 = 81R2	Frequency Restore Module 2 Setting Exceeded Alarm

DPU2000	Address	Item	Description
Y		Bit 6 = 81S2	Frequency Shed Module 2 Setting Exceeded Alarm
Y		Bit 5 = 81O2	Overfrequency Alarm Module 2 Setting Exceeded Alarm
Y		Bit 4 = 81R2	Frequency Restore Module 2 Setting Exceeded Alarm
Y		Bit 3 = 81S2	Frequency Shed Module 2 Setting Exceeded Alarm
Y		Bit 2 = 81O2	Overfrequency Alarm Module 2 Setting Exceeded Alarm
Y		Bit 1 = 81O1	Overfrequency Alarm Module 1 Setting Exceeded Alarm
Y		Bit 0 = LOADA	Load Current Alarm (lsb rightmost bit)
	40903	Logical Output	Unsigned Integer 16 Bit
N		Bit 15 = 59G	Ground Overvoltage (msb leftmost bit)
N		Bit 14 = 59G (L)	Ground Overvoltage Latched
N		Bit 13 = Rclin	Recloser In
N		Bit 12 = 79V	Overfrequency Velocity Enabled
N		Bit 11 = SBA	Slow Breaker Alarm
N		Bit 10 = 25	Synch Check Condition Sensed
N		Bit 9 = 25 (L)	Synch Check Condition Sensed
N		Bit 8 = BFA (L)	Breaker Failure Alarm
Y		Bit 7 = 32N-2 (L)	Neutral Power Directional Alarm
N		Bit 6 = 32P-2 (L)	Phase Power Directional Alarm
N		Bit 5 = 32N-2	Neutral Power Directional Alarm
Y		Bit 4 = 32P-2	Phase Power Directional Alarm
Y		Bit 3 = ReTrip (L)	Breaker Failure Retrip Alarm
Y		Bit 2 = BFT (L)	Breaker Failure Trip Alarm
Y		Bit 1 = ReTrip	Breaker Failure Retrip Alarm
Y		Bit 0 = BFT	Breaker Failure Trip Alarm (lsb rightmost bit)
	40904	Logical Output	Unsigned Integer 16 Bits
		Bit 15 = LO1	Latched Output 1 (msb leftmost bit)
		Bit 14 = LO2	Latched Output 2
		Bit 13 = LO3	Latched Output 3
		Bit 12 = LO4	Latched Output 4
		Bit 11 = LO5	Latched Output 5
		Bit 10 = LO6	Latched Output 6
		Bit 9 = LO7	Latched Output 7
		Bit 8 = LO8	Latched Output 8
		Bit 7 = 79 ON	Hot Hold Tagging Off
		Bit 6 = 79 OFF	Hot Hold Tagging On
		Bit 5 = 79 TAG	Hot Hold Tagging Tagged
		Bit 4 = 3Ph 59	3 Phase Overvoltage
		Bit 3 = 3PH 59 (L)	3 Phase Overvoltage Latched
		Bit 2 = 47	Negative Sequence Overvoltage
		Bit 1 = 47 (L)	Negative Sequence Overvoltage Latched
		Bit 0 = Reserved	Reserved (lsb rightmost bit)

Table 8-14. Logical Input Definition (8 Registers – 127 Elements)

DPU2000	Register Address	Item	Description
	40905	Logical Input	Unsigned Integer 16 Bits
Y		Bit 15 = 52a	Breaker Status 1 = Closed 0 = Open (msb leftmost)
Y		Bit 14 = 52b	Breaker Status Inverted
Y		Bit 13 = 43a	Reclosing Function Status
Y		Bit 12 = PH3	Phase Control Enabled
Y		Bit 11 = GRD	51N/50N-1/50N-2 Enabled
Y		Bit 10 = SCC	Spring Charging Contact Input Enabled
Y		Bit 9 = 79S	Single Shot Reclosing Enabled
Y		Bit 8 = 79M	Multiple Shot Reclosing Enabled
Y		Bit 7 = TCM	Trip Coil Monitoring Enabled
Y		Bit 6 = 50-1	50P-1 and 50N-1 Inst. Overcurrent Protection Enabled

Y		Bit 5 = 50-2	50P-2 and 50P-2 Inst. Overcurrent Protection Enabled
Y		Bit 4 = 50-3	50P-3 and 50P-3 Inst. Overcurrent Protection Enabled
Y		Bit 3 = ALT1	Alternate Settings 1 Enabled
Y		Bit 2 = ALT2	Alternate Settings 2 Enabled
Y		Bit 1 = ECI2	Event Capture 2 Enabled
Y		Bit 0 = ECI1	Event Capture 1 Enabled (lsb rightmost)
	40906	Logical Input	Unsigned Integer 16 Bits
Y		Bit 15 = WCI	Waveform Capture Initiate Enabled (msb leftmost)
Y		Bit 14 = ZSC	Zone Sequence Coordination Enabled
Y		Bit 13 = OPEN	Control Switch to Open Breaker Enabled
Y		Bit 12 = CLOSE	Control Switch to Close Breaker Enabled
Y		Bit 11 = 46	Negative Seq. Time Overcurrent Enabled
N		Bit 10 = 67P	Positive Seq. Dir. Controlled Phase Overcurrent Enabled
N		Bit 9 = 67N	Negative Seq. Dir. Controlled Phase Overcurrent Enabled
N		Bit 8 = ULI 1	User Logical 1 Bit Enabled
N		Bit 7 = ULI 2	User Logical 2 Bit Enabled
N		Bit 6 = ULI 3	User Logical 3 Bit Enabled
N		Bit 5 = ULI 4	User Logical 4 Bit Enabled
N		Bit 4 = ULI 5	User Logical 5 Bit Enabled
N		Bit 3 = ULI 6	User Logical 6 Bit Enabled
N		Bit 2 = ULI 7	User Logical 7 Bit Enabled
N		Bit 1 = ULI 8	User Logical 8 Bit Enabled
N		Bit 0 = ULI 9	User Logical 9 Bit Enabled (lsb rightmost)
	40907	Logical Input	Unsigned Integer 16 Bits
Y		Bit 15 = CRI	Reclose and Overcurrent Counters Cleared (msb leftmost)
Y		Bit 14 = ARCI	Automatic Reclose Inhibited
Y		Bit 13 = TARC	Trip and Automatic Reclose and Intiated
Y		Bit 12 = SEFTC	Sensitive Earth Fault Torque Control
N		Bit 11 = EXTBFI	External Starter Input Energized
N		Bit 10 = BFI	Breaker Fail Trip Logic Initiated
Y		Bit 9 = UDI	User Display Interface Message Sent to Device
N		Bit 8 = 25	Sync Check Enabled
N		Bit 7 = 25By	Sync Check Bypassed
Y		Bit 6 = LOCAL	Local Control Only when = 1
Y		Bit 5 = TGT	Target LED's Reset
Y		Bit 4 = SIA	Seal In Alarms Reset
Y		Bit 3 = LIS 1	Latched Input 1 Set
Y		Bit 2 = LIS 2	Latched Input 2 Set
Y		Bit 1 = LIS 3	Latched Input 3 Set
Y		Bit 0 = LIS 4	Latched Input 4 Set (lsb rightmost)
	40908	Logical Input	Unsigned Integer 16 Bits
Y		Bit 15 = LIS5	Latched Input 5 Set (msb leftmost)
		Bit 14 = LIS 6	Latched Iinput 6 Set
		Bit 13 = LIS 7	Latched Input 7 Set
		Bit 12 = LIS 8	Latched Input 8 Set
		Bit 11 = LIR 1	Latched Input 1 Reset
		Bit 10 = LIR 2	Latched Input 2 Reset
		Bit 9 = LIR 3	Latched Input 3 Reset
		Bit 8 = LIR4	Latched Input 4 Reset
		Bit 7 = LIR 5	Latched Input 5 Reset
		Bit 6 = LIR 6	Latched Input 6 Reset
		Bit 5 = LIR 7	Latched Input 7 Reset
		Bit 4 = LIR 8	Latched Input 8 Reset
		Bit 3 = TR_SET	Tagging Relay Set
		Bit 2 = TR RST	Tagging Relay Reset
		Bit 1 =Reserved	Reserved
		Bit 0 = Reserved	Reserved (lsb rightmost
	40909	Logical Input	Unsigned Integer 16 Bits

Y		Reserved	Reserved
Y	40910	Logical Input Reserved	Unsigned Integer 16 Bits Reserved
Y	40911	Logical Input Reserved	Unsigned Integer 16 Bits Reserved
Y	40912	Logical Input Reserved	Unsigned Integer 16 Bits Reserved

Table 8-15. Physical Output Table (1 Register Defined)

Relay	Register	Item	Description
DPU2000R/1500R	40913	Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = Reserved Bit 9 = Reserved Bit 8 = Reserved Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3 Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = CLOSE Bit 0 = TRIP	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
DPU2000	40913	Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = Reserved Bit 9 = OUT 8 Bit 8 = OUT 7 Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3 Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = Reserved Bit 0 = TRIP	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)

Table 8-16. Physical Inputs (1 Register Defined)

Relay	Register	Item	Description
DPU2000/2000R	40914	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved	16 Bit Unsigned Integer (msb leftmost bit)

		Bit 11 = Reserved Bit 10 = IN 8 Bit 9 = IN 7 Bit 8 = IN 6 Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	 (lsb rightmost bit)
DPU1500R	40914	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = IN 6 Bit 9 = Reserved Bit 8 = Reserved Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)

Table 8-17. Force Table Mapping

Notes	Register Address	Item	Descripton
FORCE PHYSICAL INPUT SELECT STATUS			
DPU2000/2000R	40915	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = IN 8 Bit 9 = IN 7 Bit 8 = IN 6 Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
DPU1500R	40915	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved	16 Bit Unsigned Integer (msb leftmost bit)

		Bit 10 = IN 6 Bit 9 = Reserved Bit 8 = Reserved Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	(lsb rightmost bit)
NOTE: 0 = Normal 1 = Forced Element			
FORCE PHYSICAL INPUT SELECT STATE STATUS			
DPU2000/ 2000R	40916	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = IN 8 Bit 9 = IN 7 Bit 8 = IN 6 Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
DPU1500R	40916	FORCE PHYS IN Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = IN 6 Bit 9 = Reserved Bit 8 = Reserved Bit 7 = IN 5 Bit 6 = IN 4 Bit 5 = IN 3 Bit 4 = IN 2 Bit 3 = IN 1 Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
NOTE : 0 = Open or Forced Reset 1 = Closed or Forced Set			
FORCE PHYSICAL OUTPUT SELECT STATUS			
DPU1500R /2000R	40917	PHYS OUT Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = Reserved Bit 9 = Reserved	16 Bit Unsigned Integer (msb leftmost bit)

		Bit 8 = OUT 6 Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3 Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = Reserved Bit 0 = TRIP	(lsb rightmost bit)
DPU2000	40917	PHYS OUT Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = OUT 8 Bit 9 = OUT 7 Bit 8 = OUT 6 Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3 Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = CLOSE Bit 0 = TRIP	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
NOTE: 0 = Normal 1 = Forced			
FORCE PHYSICAL OUTPUT SELECT STATE STATUS			
DPU1500R /2000R	40918	PHYS OUT Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = Reserved Bit 9 = Reserved Bit 8 = OUT 6 Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3 Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = Reserved Bit 0 = TRIP	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
DPU2000	40918	PHYS OUT Bit 15 = Reserved Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = OUT 8 Bit 9 = OUT 7 Bit 8 = OUT 6 Bit 7 = OUT 6 Bit 6 = OUT 5 Bit 5 = OUT 4 Bit 4 = OUT 3	16 Bit Unsigned Integer (msb leftmost bit)

		Bit 3 = OUT 2 Bit 2 = OUT 1 Bit 1 = CLOSE Bit 0 = TRIP	(lsb rightmost bit)
NOTE: 0= Open (De-asserted) 1 = Closed (Asserted)			
FORCE LOGICAL INPUT FORCED SELECT STATUS			
	40919	FORCED LOGICAL IN Bit 15 = FLI 17 Bit 14 = FLI 18 Bit 13 = FLI 19 Bit 12 = FLI 20 Bit 11 = FLI 21 Bit 10 = FLI 22 Bit 9 = FLI 23 Bit 8 = FLI 24 Bit 7 = FLI 25 Bit 6 = FLI 26 Bit 5 = FLI 27 Bit 4 = FLI 28 Bit 3 = FLI 29 Bit 2 = FLI 30 Bit 1 = FLI 31 Bit 0 = FLI 32	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
	40920	FORCED LOGICAL IN Bit 15 = FLI 1 Bit 14 = FLI 2 Bit 13 = FLI 3 Bit 12 = FLI 4 Bit 11 = FLI 5 Bit 10 = FLI 6 Bit 9 = FLI 7 Bit 8 = FLI 8 Bit 7 = FLI 9 Bit 6 = FLI 10 Bit 5 = FLI 11 Bit 4 = FLI 12 Bit 3 = FLI 13 Bit 2 = FLI 14 Bit 1 = FLI 15 Bit 0 = FLI 16	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
NOTE: 0= Normal 1= Forced Element			
FORCE LOGICAL INPUT SELECT STATE STATUS (2 Registers 32 Elements defined)			
	40921	FORCED LOGICAL IN Bit 15 = FLI 17 Bit 14 = FLI 18 Bit 13 = FLI 19 Bit 12 = FLI 20 Bit 11 = FLI 21 Bit 10 = FLI 22 Bit 9 = FLI 23 Bit 8 = FLI 24 Bit 7 = FLI 25 Bit 6 = FLI 26 Bit 5 = FLI 27 Bit 4 = FLI 28 Bit 3 = FLI 29 Bit 2 = FLI 30 Bit 1 = FLI 31	16 Bit Unsigned Integer (msb leftmost bit)

		Bit 0 = FLI 32	(lsb rightmost bit)
	40922	FORCED LOGICAL IN Bit 15 = FLI 1 Bit 14 = FLI 2 Bit 13 = FLI 3 Bit 12 = FLI 4 Bit 11 = FLI 5 Bit 10 = FLI 6 Bit 9 = FLI 7 Bit 8 = FLI 8 Bit 7 = FLI 9 Bit 6 = FLI 10 Bit 5 = FLI 11 Bit 4 = FLI 12 Bit 3 = FLI 13 Bit 2 = FLI 14 Bit 1 = FLI 15 Bit 0 = FLI 16	16 Bit Unsigned Integer (msb leftmost bit) (lsb rightmost bit)
	40923	LOGICAL OUTPUT STATUS Bit 15 = 21P-1 Bit 14 = 21P-1 (L) Bit 13 = 21P-2 Bit 12 = 21P-2 (L) Bit 11 = 21P-3 Bit 10 = 21P-3(L) Bit 9 = 21P-4 Bit 8 = 21P-4 (L) Bit 7 = C1 Bit 6 = C2 Bit 5 = C3 Bit 4 = C4 Bit 3 = C5 Bit 2 = C6 Bit 1 = TRIPT Bit 0 = NTA	16 Bit Unsigned Integer (msb leftmost bit) Phase Distance Element Zone 1 Phase Distance Element Zone 1 Latched Phase Distance Element Zone 2 Phase Distance Element Zone 2 Latched Phase Distance Element Zone 3 Phase Distance Element Zone 3 Latched Phase Distance Element Zone 4 Phase Distance Element Zone 4 Latched Control Key 1 Energized Control Key 2 Energized Control Key 3 Energized Control Key 4 Energized Control Key 5 Energized Control Key 6 Energized Trip Target Energized Neutral Target Alarm (lsb rightmost bit)
	40924	LOGICAL OUTPUT STATUS Bit 15 = Time T Bit 14 = InstT Bit 13 = NetSeqT Bit 12 = FreqT Bit 11 = DirT Bit 10 = VoltT Bit 9 = DistT Bit 8 = SEFT Bit 7 = ULO 10 Bit 6 = ULO 11 Bit 5 = ULO 12 Bit 4 = ULO 13 Bit 3 = ULO 14 Bit 2 = ULO 15 Bit 1 = ULO 16 Bit 0 = LBLL	16 Bit Unsigned Integer (msb leftmost bit) Time Element Target Alarm Energized Instantaneous ElementTarget Alarm Energized Negative Sequence Target Alarm Energized Frequency Element Target Alarm Energized Directional Element Target Alarm Energized Voltage Element Target Alarm Energized Distance Element Target Alarm Energized Sensitive Earth Fault Target Alarm Energized User Logical Output 10 Energized User Logical Output 11 Energized User Logical Output 12 Energized User Logical Output 13 Energized User Logical Output 14 Energized User Logical Output 15 Energized User Logical Output 16 Energized Live Bus Live Line (lsb rightmost bit)
	40925	LOGICAL OUTPUT STATUS Bit 15 = LBDL Bit 14 = LBLL	16 Bit Unsigned Integer (msb leftmost bit) Live Bus Dead Line Status Live Bus Live Line Status

		Bit 13 = DBDL Bit 12 = 46A Bit 11 = 46A **(L)** Bit 10 = REMOTE D Bit 9 = Prim Set Active Bit 8 = ALT1 Set Active Bit 7 = ALT2 Set Active Bit 6 = ShiftA - 1 Bit 5 = ShiftA - 2 Bit 4 = ShiftA - 3 Bit 3 = ShiftA - 4 Bit 2 = ShiftB - 1 Bit 1 = ShiftB - 2 Bit 0 = ShiftB - 3	Dead Bus Dead Line Status Negative Sequence Element Energized Negative Sequence Element Energized Latched Voltage Element Target Alarm Energized Primary Settings Group Active Alternate 1 Settings Group Active Alternate 2 Settings Group Active Shift Register A Position 1 State Energized Shift Register A Position 2 State Energized Shift Register A Position 3 State Energized Shift Register A Position 4 State Energized Shift Register B Position 1 State Energized Shift Register B Position 2 State Energized Shift Register B Position 3 State Energized (lsb rightmost bit)
	40926	LOGICAL OUTPUT STATUS Bit 15 = ShiftB - 4 Bit 14 = Reserved Bit 13 = Reserved Bit 12 = Reserved Bit 11 = Reserved Bit 10 = Reserved Bit 9 = Reserved Bit 8 = Reserved Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Reserved Bit 3 = Reserved Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	16 Bit Unsigned Integer (msb leftmost bit) Shift Register B Position 4 State Energized Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved (lsb rightmost bit)
NOTE: 0 = ON 1 = OFF			

Section 9 – Register Scaling and Re-Mapping

In the evolution of SCADA hosts, different capabilities have been implemented in conjunction with a protocol's implementation. Some SCADA manufacturers have limited the range of numbers accepted at the host level. Other SCADA manufacturers have reserved alternate definitions of most significant bit placement. Still, other SCADA manufacturers have restricted the amount of commands, which a host may send over a network.

ABB's implementation of Register Scaling and Re-mapping is one method of dealing with certain restrictions or limitations of a SCADA host's protocol implementation. For example, if a host device only accepts numbers from a value of 0 to 4095 (12 bit unipolar) or –2047 to + 2048, how can that host device interpret the Van (Voltage a to neutral) in the DPU2000 which reports the value as a number from 0 to +4,294,967,295 (32 bit number)? The answer is that one of the devices must take the 32 bit data and scale it into a format usable by the other device. Many hosts share this limitation and are unable to undertake the mathematical machinations to scale the data value. The ABB DPU2000 and 2000R permits scaling of its own internal data. The procedure is straightforward in that a simple configuration screen is presented to the operator and menu of choices is selected to complete the configuration procedure.

Re-mapping is especially instrumental in increasing network throughput by allowing all information to be accessed via one network transaction. Within the DPU2000 and 2000R, multitudes of values are available for retrieval via a network connection. However, different protocols require that each group of information can only be accessed via a single network query. Thus if three different groups of information are required via the network, three network accesses must occur. However, if the information is re-mapped to a single memory area in the relay, only one network access need be undertaken to gather the data. Network throughput is increased. Register scaling and re-mapping is common to all ABB DPU2000 and 2000R relays. The Register Scaling and Re-mapping procedure is the same for DNP/Modbus/Modbus Plus/Standard Ten Byte Protocols.

DPU2000 and DPU1500R/DPU2000R protective relays provide for scaling and re-mapping functionality. The DPU does not support this capability. Figure 9-1 illustrates the example of re-mapping Van to one of 32 possible Modbus register locations. The example table configuration entries are shown in the figure. A definition of each configuration entry and mathematically derived configuration examples follow. It must be remembered that the User Definable Registers are network read only using Modbus Code 03 (Read Holding Registers).

DPU2000, DPU1500R and 2000R Internal Operation

The DPU2000 and DPU1500R/DPU2000R reads the raw analog values received from the CT and PT physical connections. The microprocessor-based relay then converts the analog values to a raw digital numeric value from the relay's internal Analog to Digital Converter (A/D) hardware platform. The conversion of the voltage and current readings is not complete. The DPU2000 and DPU1500R/DPU2000R microprocessor then takes the raw converted value and performs a mathematical calculation providing a numeric value which is displayed on the relay's front panel MMI or through network accesses.

A protection engineer would recognize the terms as such:

PRIMARY VALUES – the metering values displayed on the protective relay's front panel interface.

SECONDARY VALUES – the current or voltage received by the CT or PT attached to the unit.

SCALED VALUES – the value received by the host device (or calculated by the IED and transmitted to the host) through the communication interface.

The mathematical calculations involved require the CT Phase, CT Neutral, and PT ratios in order to convert the raw A/D to an understandable value, displayed on the front panel MMI or available for access via a network connection. Thus, the information Van (Voltage A to Neutral), is displayed on the front panel MMI is in converted format (not raw A/D readings), and the data received via the Modbus/Modbus Plus Registers (40265 and 40266) is reported in Volts in a 32 bit representation. The maximum value able to be physically metered by the relay is dependent upon the DPU2000/2000R and the ratio of the PT and CT's used. The CT and PT values are entered into the DPU through ECP/WinECP in the Configuration Settings Menu illustrated in Figure 9-2.

However, life as we know it, is not perfect. Many SCADA hosts are unable to interpret the 32-bit value received over a network. What can be done? ABB's answer is to provide for a fill-in-the-blanks method of scaling. This method takes the interpreted value and provides for DIVISOR SCALING (taking the MMI/network register values and dividing by a constant) or a RATIO SCALING (taking the MMI values/network register values, PT Ratios, CT Ratios and Full SCALE Metered Readings) and transform it into a raw scaled value depending on the minimum/maximum value the SCADA system can interpret. The SCADA system must then receive the mathematical value and perform its own internal calculations so that the data may be displayed to the operator which mirrors that displayed on the relay's front panel.

TYPICAL SCALING EXAMPLE

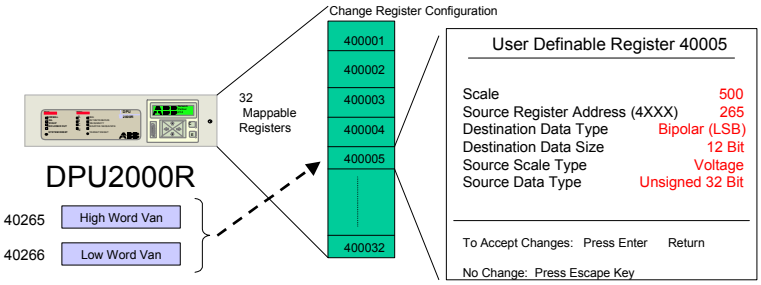


Figure 9-2. Register Scaling Methodology

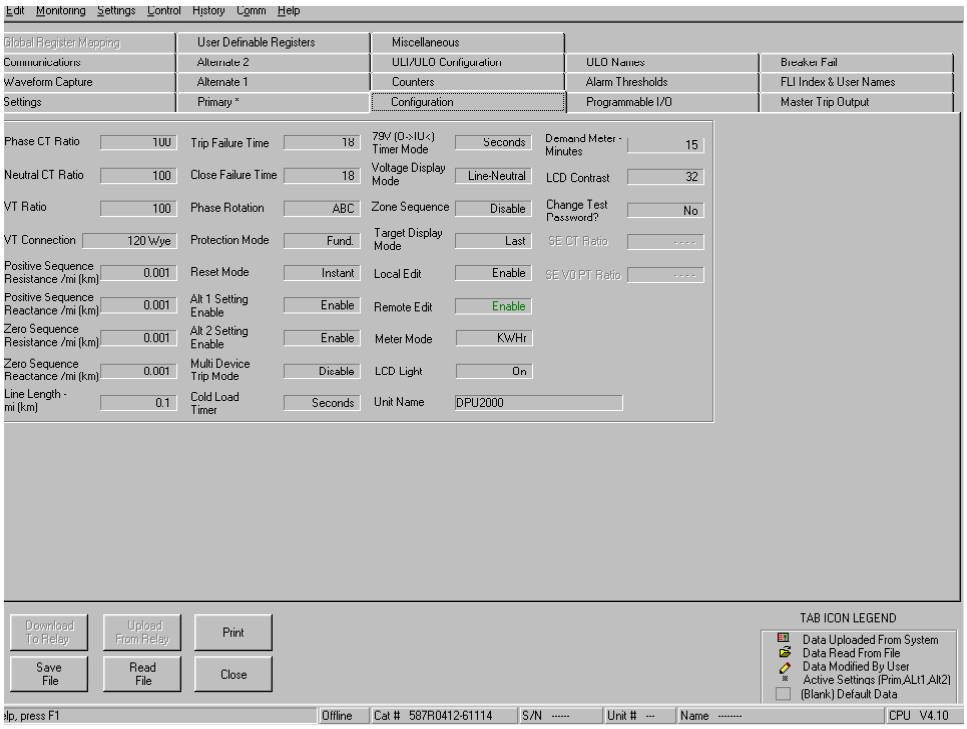
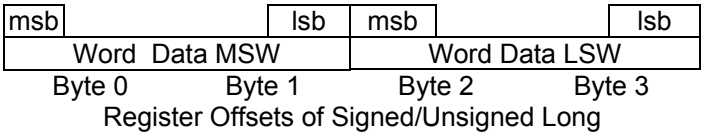


Figure 9-2. Change Configuration Settings Menu Illustrating CT and VT Configuration

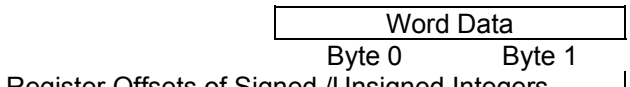
ABB Data Type Definitions

All definitions within this guide shall be based upon bits or registers. Since the ABB concept of Register Scaling and Remapping is based upon the Modbus Protocol, it is essential to understand Modbus Protocol even when providing Register Scaling and Remapping for DNP, Modbus Plus or Standard Ten Byte Protocols.

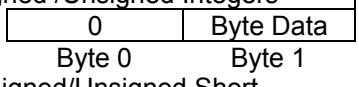
For example, Modbus requires all register values to be reported in 16 bit portions (1 word). Two registers may be combined to form numeric representations for IEEE notations, long signed (a number from –2,147,483,648 to +2,147,483,647) or unsigned numbers (a number from 0 to +4,294,967,295). If a value is requested in the short form (a number from –128 to +127, or 0 to 255), 16 bits will be returned as a response to the host's request, but the number will be within the range of an 8 bit integer.



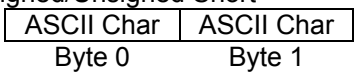
Register Offsets of Signed/Unsigned Long



Register Offsets of Signed /Unsigned Integers



Register Offsets of Signed/Unsigned Short



Register Offsets of ASCII Characters

The DPU2000 and DPU1500R/DPU2000R support the following data return types for 4X formats:

- Unsigned Short - 8 bits – 1 byte in 1 word – Range 0 to 255
- Signed Short - 8 bits – 1 byte in 1 word – Range –128 to +127
- Unsigned - 16 bits – 2 bytes in 1 word – Range 0 to + 65,535
- Signed - 16 bits – 2 bytes in 1 word – Range –32,768 to 32,767
- Unsigned Long - 32 bits – 4 bytes in 2 words – Range 0 to +4,294,967,295
- Signed Long - 32 bits – 4 bytes – in 2 words Range -2,147,483,648 to +2,147,483,647
- ASCII - 16 bits – 2 bytes – in 1 word 2 characters per register (Reference Appendix B)

The tables contained within this document reference the above definitions and give the cadence of bytes or words as:

- MSB Most Significant Byte
- LSB Least Significant Byte
- MSW Most Significant Word
- LSW Least Significant Word
- msb Most significant bit
- lsb Least significant bit

Register Scaling Investigated

Within WinECP, the Change Settings Mode must be entered. A selection titled "Register Configuration" will appear to the operator. Within WINECP, a screen as depicted in Figure 9-3 appears allowing configuration of any of the 32 available registers.

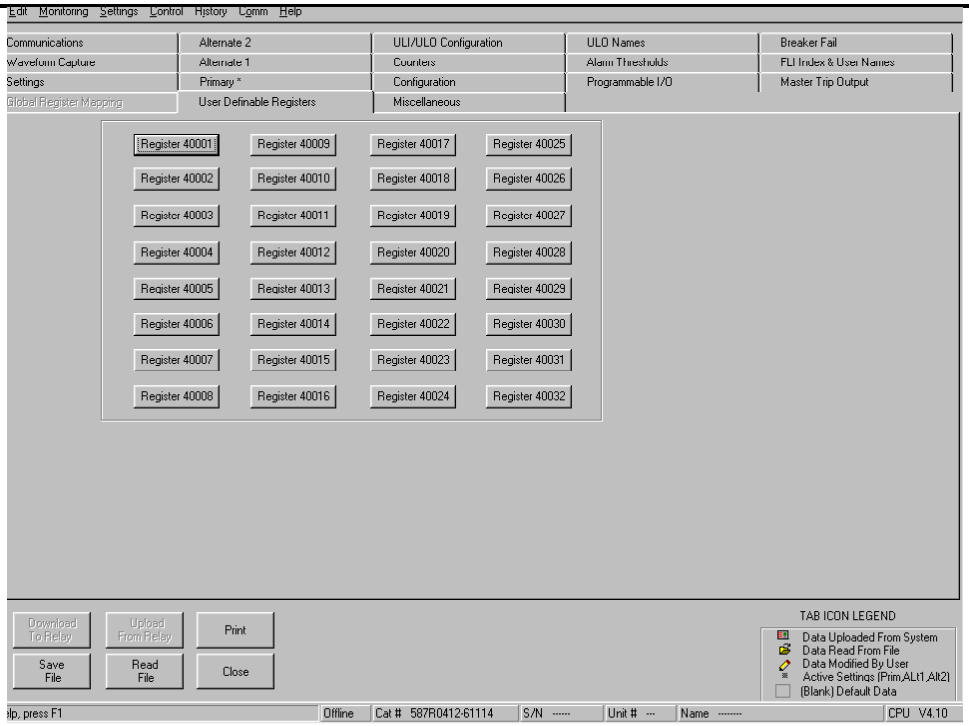


Figure 9-3. User Definable Register Configuration Screen

When using the ABB ECP Relay configuration program or the ABB WinECP Relay configuration program, the following menu items must be selected for each of the 32 mapp-able and scalable entries. The scaled register addresses are resident in Modbus addressing format from Register 40001 through 40032. The following fields must be configured to perform scaling correctly:

Table 9-1. Register Scaling Queries

ECP Query	Query Selections
Scaling Method	Unipolar
	Negative Unipolar
	Bipolar
	Offset Bipolar
Destination Register Justification (Selectable with Scaling Method)	LSB (Least Significant Bit)
	MSB (Most Significant Bit)
Destination Register Size	16 Bits
	12 Bits
	8 Bits
	4 Bits
	2 Bit
Source Register Address	257 – XXXX which is a valid 4X Register listed within this document
Source Register Type	16 Bits Signed
	16 Bits Unsigned
	32 Bits Signed
	32 Bits Unsigned
Source Scale Type	Current
	Voltage
	Power
	Normal
	Remainder

Figure 9-4 illustrates the ECP configuration which appears before the operator upon configuration of each of the User Definable Registers (UDR). Using the computer's arrow keys to select the field, and depressing the space bar shall allow configuration of the fields within this popup menu screen.

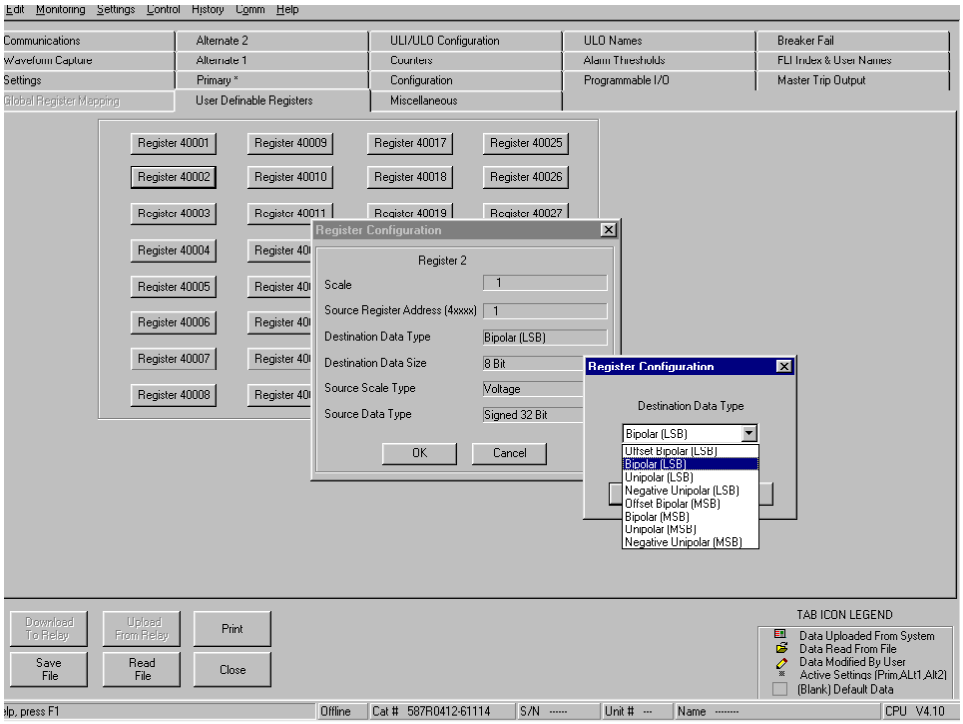


Figure 9-4. Popup Menu Configuration Screen for Data Type Register Selections

Scaling Option and Destination Register Length Options Explained

The source data may be scaled from a 32 bit or 16 bit value from the relay to a 16, 12, 8, 4, or 2, bit scale of the value which is sent to a destination register. The scaling, minimum and maximum values sent to the destination register are listed in the table below.

Table 9-2. Min/Maximum Ranges for Scaled Numbers Depending Upon Scale Option and Bit Length Selected

Scale Option	16 Bit Scale		12 Bit Scale		8 Bit Scale		4 Bit Scale		2 bit Scale	
	min	max	min	max	min	max	min	max	min	max
Offset Bipolar	0	65535	0	4095	0	255	0	15	0	4
Bipolar	-32768	32767	-2048	2047	-128	127	-8	7	-1	2
Unipolar	0	65535	0	4095	0	255	0	15	0	4
Negative Unipolar	0	65535	0	4095	0	255	0	15	0	4

The above table lists the maximum and minimum values reported to a host in the scaled format. Figure 9-5 illustrates the value correlation between the scale bit minimum and maximum numbers reported to the host versus the unscaled values generated by the DPU2000 and 2000R.

Within following discussions of scaling parameters, it should be remembered that the bit scale shall be referred to as the quantity "N" which is used extensively for the final scaled value calculation. N shall be a value of 16,12, 8, 4, or 2, which corresponds to the Bit Scale type referred to in Table 9-2 above.

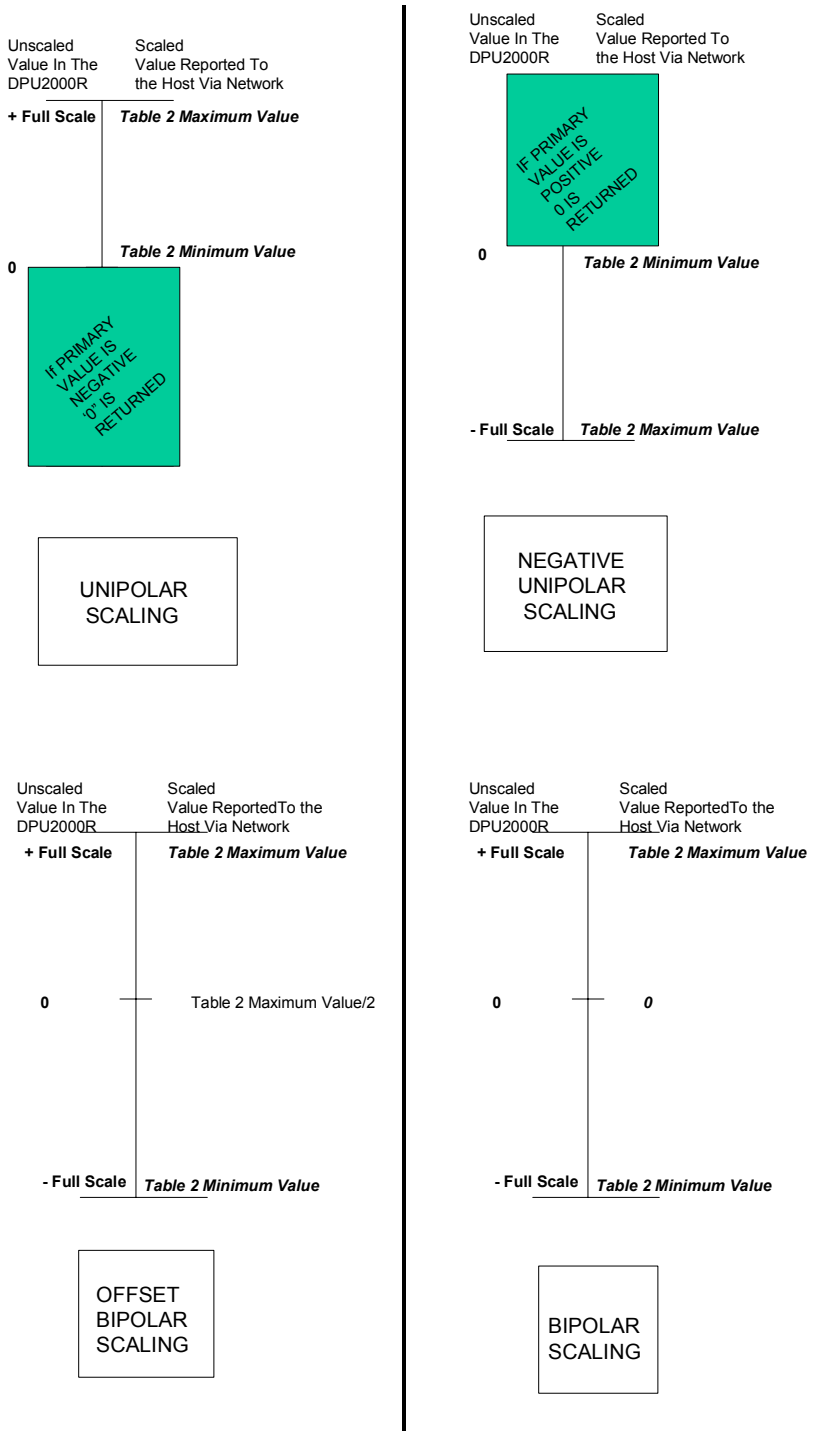


Figure 9-5. Relationship Between Scaled and Unscaled Formats for Offset Bipolar, Bipolar, Unipolar, and Negative Unipolar Scaling Selection in the DPU2000 and 2000R

If one were to mathematically compute the minimum and maximum values as described above in Table 9-2 and relate the values to the unscaled full scale + and full scale – values, the following equations would result from the analysis.

Data Type Definitions	Value Ranges
EQUATION 1:	
Offset Bipolar	(0 to $+2^N$-1) where 0 = -FS, 2^{N-1}-1 = 0 and 2^N-1 = +FS
EQUATION 2:	
Bipolar	(-2^{N-1} to + 2^{N-1}-1) where -2^{N-1} = -FS, 0 = 0 and 2^{N-1}-1 = +FS
EQUATION 3:	
Unipolar	(0 to 2^N-1) where 0 = 0 and 2^N-1 = +FS
EQUATION 4:	
Negative Unipolar	(0 to 2^N-1) where 0 = 0 and 2^N-1 = -FS

NOTE: for the above equations “N” = the amount of bits selected for scaling (i.e. 16, 12, 8, 4 , 1)

Destination Register Length Justification Options Explained

When differing hosts receive data, it receives it bit by bit. A host may interpret the bits byte by byte placing the first 8 bits of data interpreted as a MSB (Most Significant Byte) and the next 8 bits as the LSB (Least Significant Byte). Other hosts may receive the data interpreted as the first 8 bits being as LSB (Least Significant Byte) and the next 8 bits as being MSB (Most Significant Byte). Data interpretation differs by various protocol implementers (hence host or RTU manufacturers). This presents a special challenge to the automation engineer. For example, some host device implementations count the first address as address zero whereas other implementers count the first address as address 1 and internally shift the address to offset it by 1 to account for the baseline format.

Thus, ABB has included a method to account for these differences between hosts expecting to receive analog data in a specific format. ABB allows the data to be presented to the host in a Most Significant Bit Justification (MSB) and a Least Significant Bit Justification (LSB).

Another interpretation has been that of most significant bit and least significant bit justification. Two selections are possible for the query Destination Bit Justification. Selections as per Table 9-1 and Figure 9-3 are MSB and LSB. Figure 9-6 illustrates the bit definition and bit padding for the Destination Bit Justification field selection and Destination Register Size query.

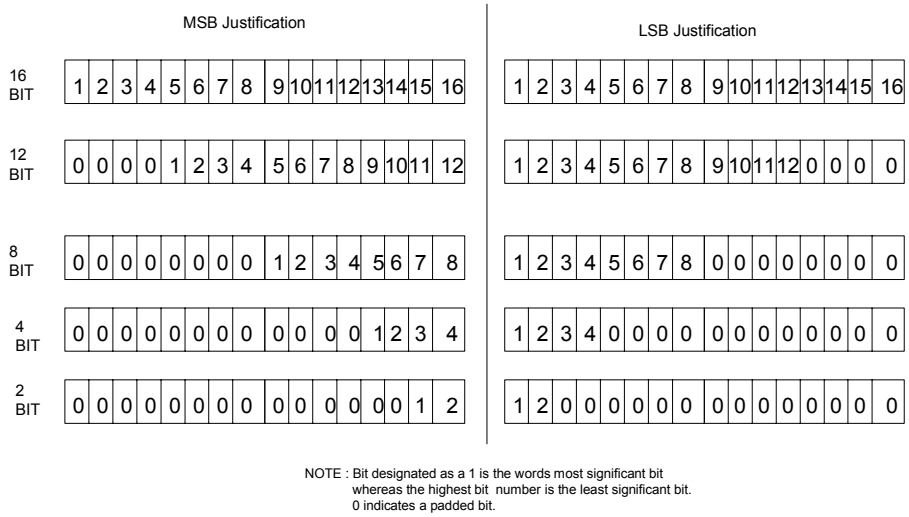


Figure 9-6. Bit Justification Notation

An investigation of Figure 9-6 illustrates that register justification shifts the data to the left of the right of the register. If the reported data for example is to be reported as 1 after scaling, the internal Modbus presentation to the host shall be 0001 hex in 12 bit MSB justification format and 0010 in the 12 bit LSB justification format. In both cases Bit 12 is set to represent the number 1, however the reported data to the host is shifted accordingly depending upon the hosts interpretation of the Modbus data.

Source Register Address and Source Register Type Explained

The Source register address is the root address number of any accepted and valid DPU2000 or DPU1500R/DPU2000R address listed within the Modbus Protocol Section of this Automation Technical Guide. For example, if one wished to map the Voltage a to neutral value from its Modbus address at Register 40265, the entry within the Source Register query would be 265. The leading 40 designation (or 4X as some refer to it as) is not required.

Unsigned Short	Register 40257	Current Phase A	16 Bit Register Unsigned
Signed Short	Register 40335	Power Factor	16 Bit Register Signed
Unsigned Long	Register 40265	Voltage Phase A	32 Bit Double Register Unsigned
Signed Long	Register 40283	kWatts Phase A	32 Bit Double Register Signed

The query field may contain any of the above four register types for data transfer.

Source Scale Range and Source Scale Type Selections Explained

Scaling is determined by a simple formula depending upon the Scale Type, Full Scale/Scale Factor, Scaling Option, and Destination Length, values.

Each of the 4X Registers defined within the Modbus Protocol Document are classified by being a Current Value, Voltage Value, or Power Value. If one of these aforementioned scale types are selected, the value in the Full Scale/Scale Factor field is designated as the maximum value of the unscaled source value. If the source value is above the configured Full Scale/Scale Factor field value, the maximum value (as shown in Table 9-2) will be reported as the destination register scaled value.

The values within the relay may be scaled by an integer factor if a normal or remainder scaling type is selected. If one of aforementioned selections are within the Full Scale/Scale Factor selection field then the selection is automatically the scale factor.

The allowable values for the Full Scale/Scale Factor field are from 1 to 65535. This is equivalent to the secondary quantities and the relationship to the primary quantities being scaled as per said formulas below. (which should be familiar to those of you who are “old” transducer engineers.)

If one of the voltage, current, or power Scale Types are selected, then one or more of the following CT /PT ratio values must be known to compute the destination scaled value. The quantities which must be known to compute the equations for scaling are:

Index 40158:	Unsigned Short	Phase CT (CT)
Index 40159:	Unsigned Short	Neutral CT Ratio (CT)
Index 40160:	Unsigned Short	PT Ratio (PT)

The values may be viewed from the ECP/WinECP program as illustrated in Figure 9-4

IF OFFSET BIPOLAR CURRENT IS SELECTED

EQUATION 5: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units

$$\text{UDR Register Value} = (2^{N-1} * \text{Source Value} / [\text{FS} * \text{CT Ratio}]) + 2^{N-1} - 1$$

IF OFFSET BIPOLAR VOLTAGE IS SELECTED

EQUATION 6: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units

$$\text{UDR Register Value} = (2^{N-1} * \text{Source Value} / [\text{FS} * \text{PT Ratio}]) + 2^{N-1} - 1$$

IF OFFSET BIPOLAR POWER IS SELECTED

EQUATION 7: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units

$$\text{UDR Register Value} = (2^{N-1} * \text{Source Value} / [\text{FS} * \text{CT Ratio} * \text{PT Ratio}]) + 2^{N-1} - 1$$

IF NORMAL SCALING IS SELECTED

EQUATION 8: NOTE Source Value is Primary Units
UDR Register Value = Source Value / Scale

IF REMAINDER SCALING IS SELECTED

EQUATION 9: NOTE: Source Value is Primary Units
UDR Register Value = Remainder of [Source Value / Scale] (commonly referred to as the modulus function).

IF BIPOLAR CURRENT IS SELECTED

EQUATION 10: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N-1}*Source Value / [FS*CT Ratio])

IF BIPOLAR VOLTAGE IS SELECTED

EQUATION 11: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N-1}*Source Value / [FS*PT Ratio])

IF BIPOLAR POWER IS SELECTED

EQUATION 12: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N-1}*Source Value / [FS*CT Ratio*PT Ratio])

IF UNIPOLAR CURRENT IS SELECTED

EQUATION 13: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N}*Source Value / [FS*CT Ratio])+2^{N-1}-1

IF UNIPOLAR VOLTAGE IS SELECTED

EQUATION 14: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N-1}*Source Value / [FS*PT Ratio])+2^{N-1}-1

IF UNIPOLAR POWER IS SELECTED

EQUATION 15: NOTE Source value is Primary Units, FS [Scale Field] is Secondary Units
UDR Register Value = (2^{N}*Source Value / [FS*CT Ratio*PT Ratio])+2^{N-1}-1

If equations 8 or 9 are used, the SCALE entry shown in Figure 9-4 refers to the Scale divisor denominator as referenced. One should notice that if equations 5 through 7 or 10 through 16 are used, the Scale entry shown in Figure 5-1, refers to the full scale value referenced in the equations.

IF UNIPOLAR OR NEGATIVE UNIPOLAR EQUATIONS ARE USED, Then the BIPOLAR equations above are applicable with the note that:

FOR UNIPOLAR, if the result of the equation (10,11,or 12) is positive, then the register is filled with the value calculated, else the reported value is 0.

FOR NEGATIVE UNIPOLAR, if the result of the equation (10,11, or 12) is negative, then the register is filled with the absolute value of the equation. If the calculated value is positive in sign, then the reported value is 0.

DPU2000 and 2000R User Definable Register Defaults

The DPU2000 and 2000R contains User Definable Register default mappings as shown in Table 9-3 below. It should be noted that the register shall saturate at the maximum values computed and shown in Table 9-2 above. The maximum saturation value can be computed to be 2N -1 where N is the register size in bits.

Table 9-3. Default Scaling and Re-Mapping Register Assignments

Programmable Register	Register Type (Bits)	Start Register (Bits/Type)	FS or Scale(Type)	Description
40001	Unipolar (16,LSB)	129 (16/Unsigned)	1 (Normal)	Relay Status
40002	Offset Bipolar (12,LSB)	257 (16/Unsigned)	10 (Current)	Load Current A
40003	Offset Bipolar (12,LSB)	259 (16/Unsigned)	10 (Current)	Load Current B
40004	Offset Bipolar (12,LSB)	261(16/Unsigned)	10 (Current)	Load Current C
40005	Offset Bipolar (12,LSB)	265 (32/Unsigned)	150 (Voltage)	Voltage VAN
40006	Offset Bipolar (12,LSB)	268 (32/Unsigned)	150 (Voltage)	Voltage VBN
40007	Offset Bipolar (12,LSB)	271 (32/Unsigned)	150 (Voltage)	Voltage VCN
40008	Offset Bipolar (12,LSB)	289 (32/Signed)	3000 (Power)	3 Phase Watts
40009	Offset Bipolar (12,LSB)	297 (32/Signed)	3000 (Power)	3 Phase VARs
40010	Offset Bipolar (12,LSB)	283 (32/Signed)	1000 (Power)	Phase A Watts
40011	Offset Bipolar (12,LSB)	285 (32/Signed)	1000 (Power)	Phase B Watts
40012	Offset Bipolar (12,LSB)	287(32/Signed)	1000 (Power)	Phase C Watts
40013	Offset Bipolar (12,LSB)	291 (32/Signed)	1000 (Power)	Phase A VARs
40014	Offset Bipolar (12,LSB)	293 (32/Signed)	1000 (Power)	Phase B VARs
40015	Offset Bipolar (12,LSB)	295 (32/Signed)	1000 (Power)	Phase C VARs
40016	Unipolar (16,LSB)	158 (16/Unsigned)	1 (Normal)	Phase CT Ratio
40017	Unipolar (16,LSB)	160 (16/Unsigned)	1 (Normal)	PT Ratio
40018	Offset Bipolar (12,LSB)	263 (16/Unsigned)	10 (Current)	Load Current
40019	Unipolar (16,LSB)	305 (32/Signed)	10000 (Normal)	+3 Phase kWatthours (High)
40020	Unipolar (16,LSB)	305 (32/Signed)	10000 (Remainder)	+3 Phase kWatthours (Low)
40021	Neg Unipolar (16,LSB)	305 (32/Signed)	10000 (Normal)	-3 Phase kWatthours (High)
40022	Neg Unipolar (16,LSB)	305 (32/Signed)	10000 (Remainder)	-3 Phase kWatthours (Low)
40023	Unipolar (16,LSB)	313 (32/Signed)	10000 (Normal)	+3 Phase kVARhours (High)
40024	Unipolar (16,LSB)	313 (32/Signed)	10000 (Remainder)	+3 Phase kVARhours (Low)
40025	Neg Unipolar (16,LSB)	313 (32/Signed)	10000 (Normal)	-3 Phase kVARhours (High)
40026	Neg Unipolar (16,LSB)	313 (32/Signed)	10000 (Remainder)	-3 Phase kVARhours (Low)
40027	Unipolar (16,LSB)	327(16/Unsigned)	1 (Normal)	System Frequency
40028	Undefined	Undefined	Undefined	Undefined
40029	Undefined	Undefined	Undefined	Undefined
40030	Undefined	Undefined	Undefined	Undefined
40031	Undefined	Undefined	Undefined	Undefined
40032	Undefined	Undefined	Undefined	Undefined

An explanation of some of the above default mappings are offered as a guide to understanding the scaling methodology implementation. Figure 9-7 illustrates the scaling procedure for Registers 40002 through 40005 [UDR 2 through 5, DNP 3.0 indexes 98 through 101). Source Registers 40257, 40259, and 40261 contain the MMI reported [Primary Units] current values to be remapped and re-scaled to 12 bit Offset Bipolar Values. [Scaled Value from 0 to 4095].

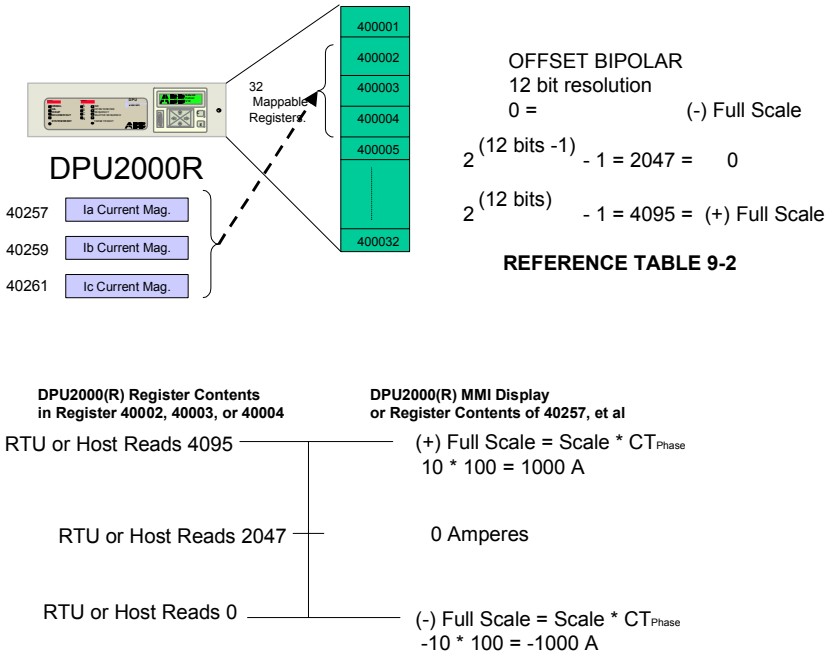


Figure 9-7. Register Scaling Default Example

The mathematics to determine the reported value to the host is illustrated in Figure 9-8 and using Equation 5 above.

Full Scale = **10 A**
CT Ratio (Current Calculation) = **100:1** (as per the default screen shown in Figure 9-2)
Source Value Location = **259 16 Bit Value Signed**
Calculate the 12 bit scaled reading when the DPU1500R/DPU2000R indicates 5A for Ia.

$$((2^{(12\ bits\ -1)} * 5A)/(10\ A * 100)) + (2^{(12\ bits\ -1)} - 1) = 3071\ counts.$$

Thus Equation 7 illustrates that a current of 5A displayed on the MMI shall indicate a count of 3071 reported to the SCADA Host when Register 40002 is read. The SCADA host shall then interpret it and display it on its host screen as 5 A.

Perhaps another example shall suffice. The DPU2000/2000R also meters voltages. The next example illustrates the scaling which occurs for the default Registers 40005, 40006, and 40007. Figure 9-8 shows the scale algorithm application for scaling to an Offset Bipolar 12 bit number.

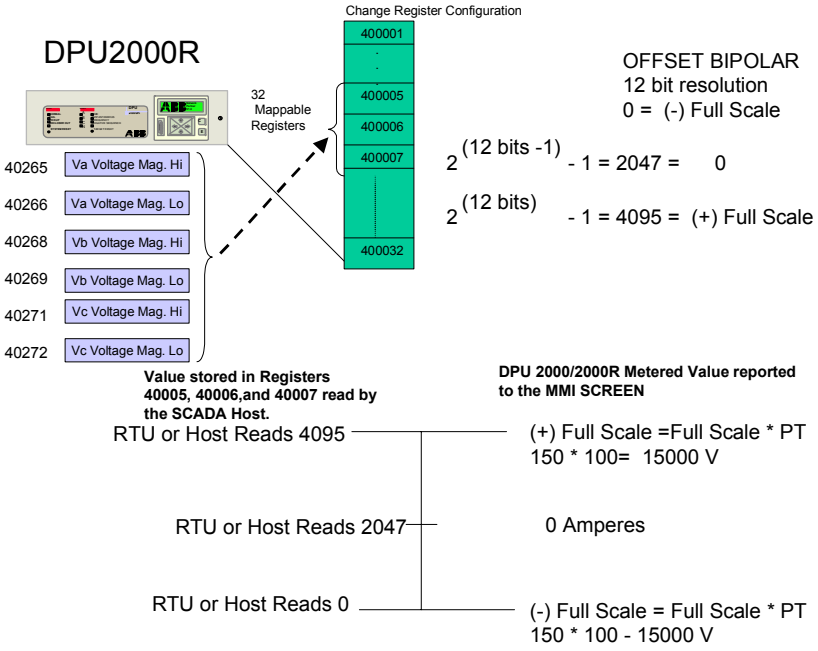


Figure 9-8. Scaling Example for Voltage Mapped Registers

The values used for this example are:

Note the Full Scale used to perform the calculations are primary units being Full Scale Secondary * PT Ratio.

Full Scale = **150 V [Secondary Units]**
PT Ratio (Current Calculation) = **100:1**
Source Value Location = **265** **32 Bit Value Unsigned**

Using Equation 6 the following results when calculating the numeric value reported to the SCADA host when Register 40005, 40006 or 40007 is accessed.

$$((2^{(12\ bits\ -1)} * 11884)/(150 * 100)) + (2^{(12\ bits\ -1)} - 1) = 3699.562\ counts$$

1621.7699.5+ 2047 = 3698.76

When the front panel MMI reads 11884 V, a value of 3698 is reported to the SCADA host.

One final example is illustrated for transferring values from different areas in the protective relay to the default table. Such values as Relay status (located in Register 129 [and transferred to UDR 1 40001), Phase CT ratio (used by the SCADA host to provide for scale conversion located in Register 158 [and transferred to UDR 16, Register 40016), PT ratio (used by the SCADA host to provide for scale conversion in register 160 [As per Table 9-8] and transferred to UDR 17, Register 40017), and system frequency (Transferred to UDR 27, Register 40017).

The transfer of registers to a block is accomplished by using equation 8 and providing a scale factor of 1. Thus the contents of the source register are divided by 1 and transferred to the User Definable Register Table. It is important that the scale type of 16 be used to ensure the transfer is not scaled.

Section 10 - 4X Register Write Capabilities

All of the Modbus status retrieval have involved 03 register read commands only. Modbus allows for two types of commands involving control writes to obtain read data. One Modbus command allows register writes. Another Modbus command allows for register writes and reads with one command. The type of functionality performed with relay writes is as such:

- Access of Fault Records
- Access of Event Records
- Trip/Close Initiation
- Enable/Disable of Protective Functions
- Clearing of Event Counters
- Enable/Disable of Supervisory Functions
- Reset of Targets
- Clear of Seal In's

Function Code 16 Preset 4X Registers (Write Only)

Figure 10-1 illustrates the Modbus command structure writing multiple registers.

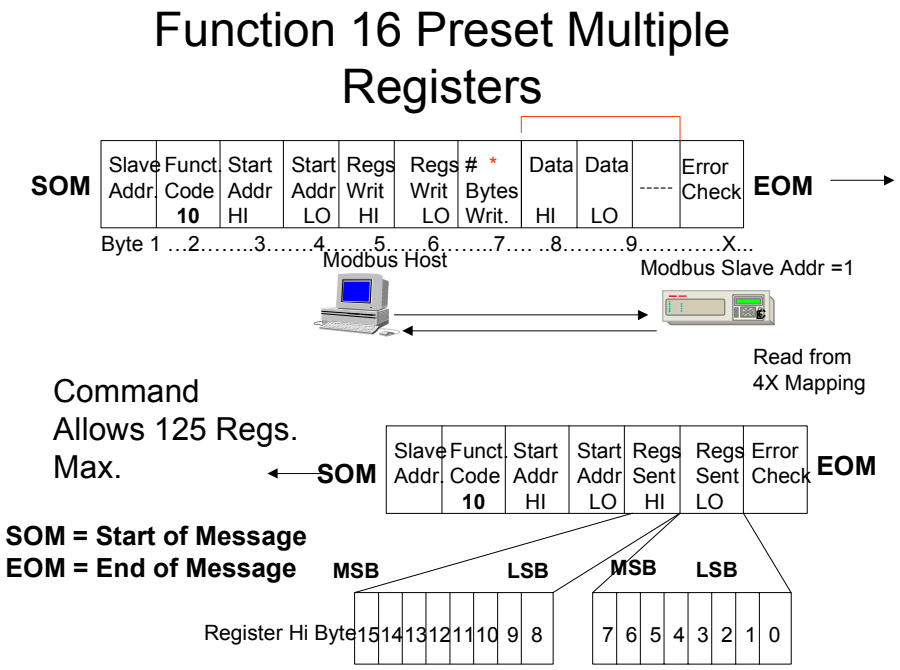


Figure 10-1. Modbus Write Command 16 (10 HEX) Allowing Writes to the DPU2000/2000R

The write multiple register command is convenient for writing the following control blocks:

- Control Block 1 – 41664 through 41670
- Control Block 2 – 41671 through 41676
- Control Block 3 – 41677 through 41682
- Control Block 4 – 41683 through 41688

Control Block 1 allows for:

- Initiation of Relay Trip
- Initiation of Relay Close
- Resetting of Targets
- Enabling or Disabling of Selective Protective Functions
- Disabling or Enabling of Communication Port Functions.
- Enabling or Disabling of Supervisory Control Functions via the Communication Ports

Control Block 2 allows for:

- Forcing of Outputs 1 through 4 for a limited pulse duration time

Control Block 3 allows for:

- Reset of Latch Bit Functions

Control Block 4 allows for:

- Reserved Functions

Whenever a write occurs to the DPU2000/2000R:

- The DPU2000/2000R receives the command:
- Command Interpreted in 1 quarter cycle.
- Relay Protection Occurs.
- Command acts on the device.
- The command response is generated to the Host from the DPU2000/2000R after the action is completed.

The defined control blocks 1 and 2 are write capable and are well suited for access control via the Modbus command 16 (10 HEX).

Function 23 Read/Write Register (Read/Write Concurrently)

Another format command which allows for a simultaneous read/write is command 23 (17 HEX). Figure 10-2 illustrates the read/write 4X Register command format. The 23 command is used when the user wishes to write a register for control buffer access and read a group of registers which was accessed via the read.

Control Blocks 1 and 2 allows for access of protective device function state. If a user wished to read the status of each function within the relay, a Function Read/Write Register Command would be the most desirable command to be issued. Read/Write register data commands are also useful in accessing the Operation and Fault record blocks.

Review of the Modbus 23 command allows for write and read of data if the total amount of read and write registers do not exceed over 125 words. An advantage of using a combined read/write command is that of speed. If conventional commands were to be used, a 16 Write 4X Register Command would be issued and thereafter, within 10 seconds, a 03 Modbus (Read 4X Register Command) would then be issued to extract the data from the relay. Using Modbus command 23 allows for decreasing of the overhead associated with multiple register reads and writes.

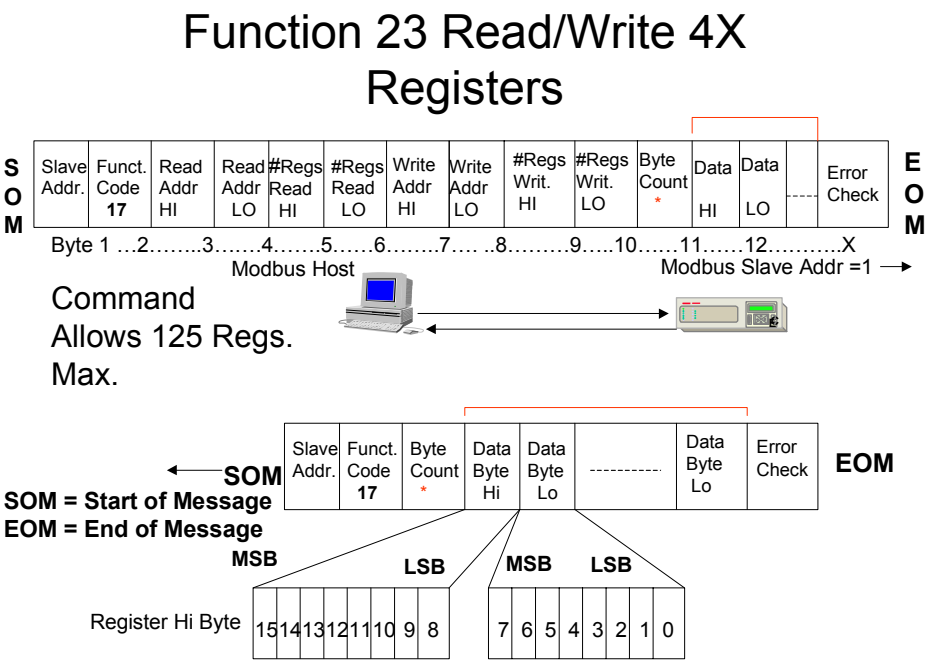


Figure 10-2. Function 23 READ/WRITE Command Format

Fault Records (27 Registers Defined)

Fault records are stored in the DPU2000/2000R according to the following format. Figure 10-3 illustrates the method of accessing the Fault Record Data via the DPU2000/2000R. The DPU2000/2000R has an internal circular buffer, which stores a maximum of 32 faults. These faults are stored internally to the DPU2000/2000R's fault stack as indicated in the figure. Each fault is defined as a block of 26 registers as shown in Tables 10-1 and 22. The first defined register in the table is the fault record control register. Fault records are viewed by writing a data word to 41409 as defined in the table below and reading the block of consecutive registers from 41410 through 41452.

If the number of faults exceed 32, then the buffer overwrites the oldest record contained within its internal stack. Access and control can be accomplished over Modbus in one of two methods.

If 41409 has a value of 1 written to it, Registers 41410 through 41452 will fill with the FIRST fault within the 32 records stored in the unit. 41409 will then reset to a value of 0 when Registers 41410 through 41452 are refreshed by the DPU2000/DPU1500R/DPU2000R.

If 41409 has a value of 2 written to Register 41409, Registers 41410 through 41452 will contain the NEXT record of fault data which was pointed after the write command executed. 41409 will reset to a value of 0 after the record has entered the buffer and is read by the host.

If 41409 has a value of 3 written to it, Registers 41410 through 41452 will fill with the LAST UNREPORTED record of fault data in the 32 records of fault data stored in the unit. For example, if two records of data accumulated between reads, a read oldest unreported record command would point to the oldest record of data accumulated in the buffer. If the command of 3 was then sent to Registers 41409, the last record of unreported data would be placed in the buffer. If a command of 3 was then sent to Register 41409, all the registers would display a value of 0 (Registers 41410 through 41452) indicating that no more records are available to be reported to the host. The number of unreported fault records may be read from the IED by accessing Modbus Register 40770.

If no data accumulated within the fault record, values of 0 shall be returned in the buffer. A new fault record entry is indicated via Bit 6 of Register 40129 being set to a 1. Reference Table 10-3 of this document for a more detailed explanation of the registers bit map.

The Fault Record number can be a number from 1 to 999. ONLY THE PREVIOUS 32 RECORDS ARE KEPT IN THE FAULT RECORD BUFFER. Fault Records are sequentially numbered from 1 to 999. If the fault number is presently at 999, and an additional fault is recorded, the fault number shall rollover to 1. The Record number and fault buffer cannot be cleared and reset through a keypad or unit reset procedure or a reset via the network as explained in Section 3 as a note.

Method 1:

The host writes a Modbus 23 Command (Modbus 4X Register Read/Write) in which a control code (1, 2, or 3) is written to 41409 and the buffer is filled with fault data in Registers 41410 through 41452 to be returned as a response to the command. A command of 1 = Points to the First Record in the Fault Table. A command of 2 Points to the next fault in the fault table. A command of 3 points to the last unreported fault in the fault table. Figure 10-4 graphically illustrates the write/read process for access of fault or operation records.

Method 2:

The host writes a Modbus Command 16 (Modbus 4X Register Write Command) in which a control code (1, 2, or 3) is written to 41409 and the buffer is filled with fault data in Registers 41410 through 41452. Within 10 seconds after the 16 command is issued, the host issues a Modbus 03 command (Modbus 4X Register Read command) in which the fault data is retrieved from the buffer in Register 41410 through 41452.

Table 10-1. Fault Status Modbus Address Map Definition

Register Address	Item		Description
41409	Fault Record Control Register 1 = First Record 2 = Next Record 3 = Oldest Unreported Record		Unsigned 16 Bit 1 = Fill 41026 – 41051 with First Record Data. 2 = Fill 41026 – 41051 with next Record Data pointed to in buffer. 3 = Fill 41026 – 41051 with the last (oldest unreported) record of data.
41410	Fault Trip Type (see below)		Unsigned 16 Bit See Reference at end of table
41411	Active Set and Reclose Sequence		Unsigned 16 Bit 17 = Primary Settings – Reclose 1 18 = Primary Settings – Reclose 2 19 = Primary Settings – Reclose 3 20 = Primary Settings – Reclose 4 21 = Primary Settings – LOCKOUT 33 = Alt 1 Settings – Reclose 1 34 = Alt 1 Settings – Reclose 2 35 = Alt 1 Settings – Reclose 3 36 = Alt 1 Settings – Reclose 4 37 = Alt 1 Settings – LOCKOUT 65 = Alt 2 Settings – Reclose 1 66 = Alt 2 Settings – Reclose 2 67 = Alt 2 Settings – Reclose 3 68 = Alt 2 Settings – Reclose 4 69 = Alt 2 Settings – LOCKOUT
41412	Fault Record Number		Unsigned 16 Bit (1 – 999, only last 32 kept)
41413	Year	2 digit 00 -99	Unsigned 16 Bit Year of Fault
41414	Month	1 - 12	Unsigned 16 Bit Month of Fault
41415	Day	1 - 31	Unsigned 16 Bit Day of Fault
41416	Hour	00 - 23	Unsigned 16 Bit Hour of Fault
41417	Minute	00 - 59	Unsigned 16 Bit Minute of Fault
41418	Second	00 - 59	Unsigned 16 Bit Second of Fault

41419	Hundred Seconds 0 - 99	Unsigned 16 Bit Hundredth Second of Fault Time
41420	Fault Ia Magnitude	Unsigned 16 Bit (X Reg 41424)
41421	Fault Ib Magnitude	Unsigned 16 Bit (X Reg 41424)
41422	Fault Ic Magnitude	Unsigned 16 Bit (X Reg 41424)
41423	Fault Current Scale Type	Unsigned 16 Bit
41424	Fault In Magnitude	Unsigned 16 Bit
41425	Fault Ia Angle	Unsigned 16 Bit
41426	Fault Ib Angle	Unsigned 16 Bit
41427	Fault Ic Angle	Unsigned 16 Bit
41428	Fault In Angle	Unsigned 16 Bit
41429	Zero Seq. Current Mag	Unsigned 16 Bit
41430	Pos. Seq. Current Mag	Unsigned 16 Bit
41431	Neg. Seq. Current Mag	Unsigned 16 Bit
41432	Zero Seq. Angle	Unsigned 16 Bit
41433	Pos. Seq. Angle	Unsigned 16 Bit
41434	Neg. Seq. Angle	Unsigned 16 Bit
41435	Fault Kvan/KVab Magnitude	Unsigned 16 Bit (X 100)
41436	Fault Kvbn/KVbc Magnitude	Unsigned 16 Bit (X 100)
41437	Fault Kvcn/Kvca Magnitude	Unsigned 16 Bit (X 100)
41438	Fault Kvan/KVab Angle	Unsigned 16 Bit
41439	Fault Kvbn/KVbc Angle	Unsigned 16 Bit
41440	Fault Kvcn/Kvca Angle	Unsigned 16 Bit
41441	Pos Sequence KV Magnitude	Unsigned 16 Bit
41442	Neg Sequence KV Magnitude	Unsigned 16 Bit
41443	Positive Sequence V Angle	Unsigned 16 Bit
41444	Negative Sequence V Angle	Unsigned 16 Bit
41445	Fault Location	Unsigned 16 Bit (X 10)
41446	Breaker Impedance Hi Word	Unsigned Long 32 Bit (MSW)
41447	Breaker Impedance Lo Word	Unsigned Long 32 Bit (LSW)
41448	Breaker Operate Time mS Hi Word	Unsigned Long 32 Bit (MSW)
41449	Breaker Operate Time mS Low Word	Unsigned Long 32 Bit (LSW)
41450	Relay Operate Time mS Hi Word	Unsigned Long 32 Bit (MSW)
41451	Relay Operate Time Lo Word	Unsigned Long 32 Bit (LSW)
41452	Record Status	Record Status Bit 1 = 0 = Fault 1= Event Capture Bit 0 = Wye = 0 Delta = 1

Table 10-2. Fault Codes

Fault Element Type	Message Number
51P	0
51N	1
50P-1	2
50N-1	3
50P-2	4
50N-2	5
50P-3	6
50N-3	7
67P (DPU2000 & DPU2000R)	8
67N (DPU2000 & DPU2000R)	9
46	10
81 (DPU2000 & DPU2000R	11
Zone Step	12
ECI-1	13
ECI-2	14
SEF (for SE model)	15
46A	16

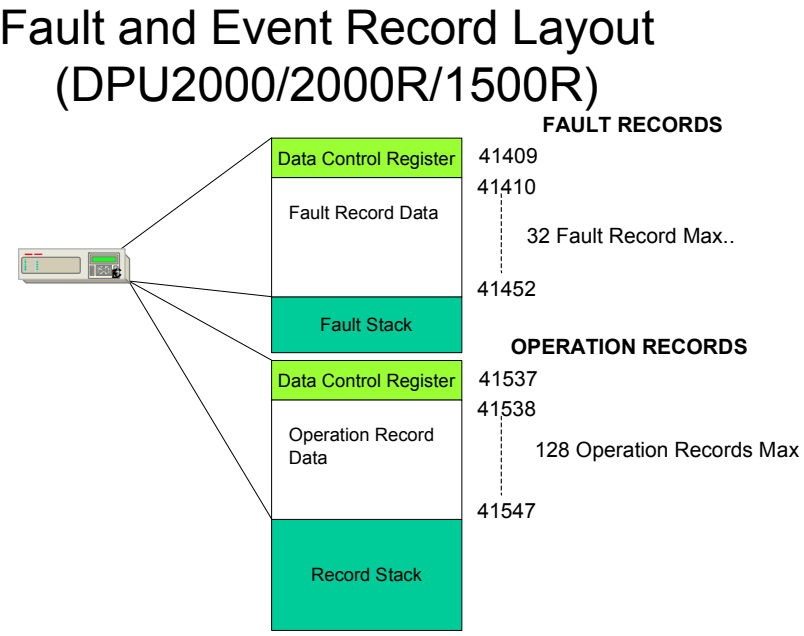


Figure 10-3. Event and Operation Memory Map for the DPU2000/2000R

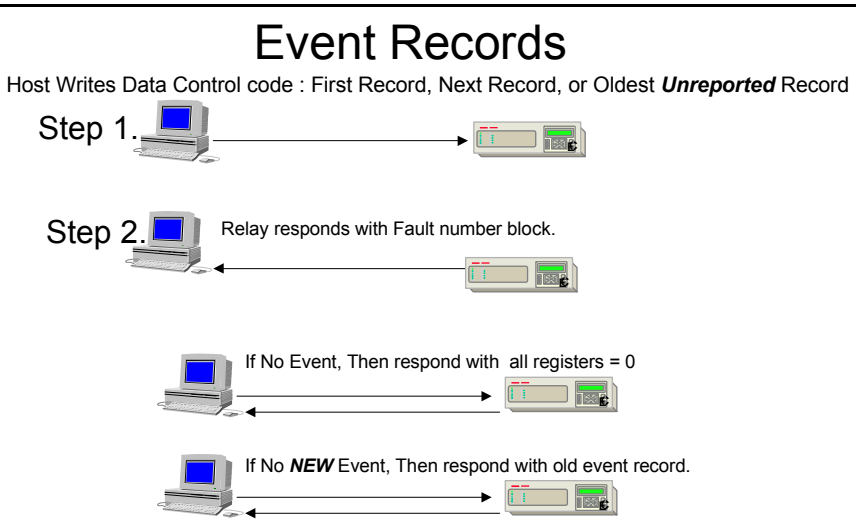


Figure 10-4. Event Record Access Illustration if Function 23 is Issued to DPU2000/2000R Device

Event Records (11 Registers Defined)

Event Record data is stored in the same manner as the Fault Record Data. Figure 10-3 illustrates the method of storage of the Event Record Data. As illustrated, 128 Groups of fault data is stored internal to the DPU2000/2000R. Each group is comprised of 11 registers of data as defined in Tables 10-3 and 10-4. The register for pointing to a group is defined in Register 41281. Fault records are viewed by writing a data word to 41537 as defined in the table below and reading the block of consecutive registers from 41538 through 41547.

If the number of Operation Records exceed 128, then the buffer overwrites the oldest record contained within its internal stack. Access and control can be accomplished over Modbus in one of two methods.

If 41537 has a value of 1 written to it, Registers 41538 through 41547 will fill with the FIRST Operation record within the 128 records stored in the unit. 41537 will then reset to a value of 0 when Registers 41538 through 41547 are read.

If 41537 has a value of 2 written to it, Registers 41538 through 41547 will contain the NEXT record of Operation Record data which was pointed after the write command executed. 41537 will reset to a value of 0 after the record has entered the buffer and is read by the host.

If 41537 has a value of 3 written to it, Registers 41537 through 41547 will fill with the LAST UNREPORTED record of Operation Record data in the 128 records of fault data stored in the unit. For example, if two records of data accumulated between reads, a read LAST UNREPORTED record command would point to the oldest unreported record of data accumulated in the buffer. The host could then send another value of 3 to the control register to obtain the newest value of the unreported record. A write of 3 to the fault record also would fill the buffer with a value of zero to indicate there are no other values to be retrieved from the buffer. The number of unreported operation records may be read from Modbus Register 40769.

If no data accumulated within the fault record, (such as after a system reset), values of 0 shall be returned in the buffer. A new fault record entry is indicated via Bit 8 of Register 41537 being set to a 1. Reference Table 10-3 of this document for a more detailed explanation of the registers bit map.

As with fault records, there are two methods of obtaining the information via the Modbus 23 (Write/Read) command or a combination of the Modbus 16 (Write Register) and 03 (Read Register) commands.

Method 1:

> The host writes a Modbus 23 Command (Modbus 4X Register Read/Write) in which a control code (1, 2, or 3) is written to 41537 and the buffer is filled with fault data in Registers 41538 through 41548 to be returned in response to the command. A command of 1 = Points to the First Record in the Fault Table. A command of 2 Points to the next fault in the fault table. A command of 3 points to the last UNREPORTED fault in the fault table.

Method 2:

The host writes a Modbus Command 16 (Modbus 4X Register Write Command) in which a control code (1, 2, or 3) is written to 41537 and the buffer is filled with fault data in Registers 41538 through 41548. Within 10 seconds after the 16 command is issued, the host issues a Modbus 03 command (Modbus 4X Register Read command) in which the fault data is retrieved from the buffer in Register 41538 through 41548.

One should note the operation record event codes are arranged in groups to easily indicate the type of error dependent on the value of the operation record. Table 10-4 lists the Operation Record Event Codes. NOTE the fault or event record will only change if the Event Control Register is written and the consecutive registers in the bufer (41538 through 41547). When this step is performed the counter register for unreported faults or events will then decrement.

Table 10-3. Operation Record Address Definition

Register Address	Item	Description
41537	EvtRecCtlReg 1 = First Record 2 = Next Record 3 = Last Unreported Record	Fault Record Control Register Unsigned 16 Bit 1 = Fill 41281 – 41291 with First Record Data 2 = Fill 41281 – 41291 with next Record Data pointed to in buffer 3 = Fill 41281 – 41291 with the last unreported record of data between the last data access
41538	Year (0-99)	Unsigned 16 Bit Year of Event
41539	Month	Unsigned 16 Bit Month of Event
41540	Day	Unsigned 16 Bit Day of Event
41541	Hour	Unsigned 16 Bit Hour of Event
41542	Minute	Unsigned 16 Bit Minute of Event
41543	Second	Unsigned 16 Bit Second of Event
41544	Hundredths of a Second	Unsigned 16 Bit Hundredth Second of Event Date
41545	Message Number	Unsigned Integer 16 Bits 0<=Range <=999
41546	VALUE	Front panel interface changed value
41547	Operation Number	16 Bit Unsigned See Table 10-4

Table 10-4. Event Record Definition Type

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
0	51P Trip
1	51N Trip
2	50P-1 Trip
3	50N-1 Trip
4	50P-2 Trip
5	50N-2 Trip
6	50P-3 Trip
7	50N-3 Trip
8	67P Trip (DPU2000/R)
9	67N Trip (DPU2000/R)
10	46 Trip
11	27-1P Alarm
12	59 Alarm (DPU2000/R)
13	79V Block
14	81S-1 Trip (DPU2000/R)
15	81R-1 Restore (DPU2000/R)

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
16	81V Block (DPU2000/R)
17	TOC Pickup-No Trip
18	27-3P Alarm
19	SEF Trip
20	External Trip
21	External Close
22	Breaker Opened
23	Breaker Closed
24	Open Trip Contact
25	Recloser Lockout
26	Direct Trip
27	Direct Close
28	MDT Close
29	External Trip and ARC
30	Reclose Initiated
31	CB Failed to Trip
32	CB Failed to Close
33	CB Pops Open
34	CB Pops Closed
35	CB State Unknown
36	CB Stuck Closed
37	Ext. Trip CB Stuck
38	Springs Discharged
39	- Reserved for future use -
40	Manual Trip
41	Manual Close
42	Ground TC Enabled
43	Ground TC Disabled
44	Phase TC Enabled
45	Phase TC Disabled
46	Primary Set Active
47	Alt 1 Set Active
48	Alt 2 Set Active
49	Zone Step
50	Recloser Enabled
51	Recloser Disabled
52	Zone Sequence Enabled
53	Zone Sequence Disabled
54	50P/N-1 Disabled
55	50P/N-2 Disabled
56	50P/N-3 Disabled
57	50P/N-1 Enabled
58	50P/N-2 Enabled
59	50P/N-3 Enabled
60	81S-2 Trip (DPU2000/R)
61	81R-2 Restore (DPU2000/R)
62	81O-1 Overfrequency (DPU2000/R)
63	81O-2 Overfrequency (DPU2000/R)
64	Closed Failed No Sync
65	Live Bus Live Line (DPU2000R V5.20+)
66	Live Bus Dead Line (DPU2000R V5.20+)
67	Dead Bus Live Line (DPU2000R V5.20+)
68	Dead Bus Dead Line (DPU2000R V5.20+)
69	Software Error

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
70	Blown Fuse Alarm
71	OC Trip Counter
72	Accumulated KSI
73	79 Counter 1 Alarm
74	Phase Demand Alarm
75	Neutral Demand Alarm
76	Low PF Alarm
77	High PF Alarm
78	Trip Coil Failure
79	kVAR Demand Alarm
80	79 Counter 2 Alarm
81	Pos kVAR Alarm
82	Neg. kVAR Alarm
83	Load Alarm
84	Cold Load Alarm
85	Pos Watt Alarm 1
86	Pos Watt Alarm 2
87	32P Trip (DPU2000/R)
88	32N Trip (DPU2000/R)
89	- Reserved for future use -
90	Event Capture #1
91	Event Capture #2
92	Waveform Capture
93	BFT Operation (DPU2000/R)
94	RETRIP Operation (DPU2000/R)
95	Ext. BFI Enabled (DPU2000/R)
96	Ext. BFI Disabled (DPU2000/R)
97	BFI Enabled (DPU2000/R)
98	BFI Disabled (DPU2000/R)
99	- Reserved for future use -
100	ROM Failure
101	RAM Failure
102	Self Test Failed
103	EEPROM Failure
104	BATRAM Failure
105	DSP Failure
106	Control Power Fail
107	Editor Access
108	System Reboot Init
109	Interrupt Overlap
110	DSP COP Status
111	System Booting
112	- Reserved for future use -
113	- Reserved for future use -
114	- Reserved for future use -
115	Suprvsr Stack Pointer
116	User Stack Pointer
117	Task Control Block
118	Stack Base
119	Task Address
120	Shift-A
121	Shift-B
122	- Reserved for future use -
123	- Reserved for future use -

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
124	- Reserved for future use -
125	- Reserved for future use -
126	- Reserved for future use -
127	- Reserved for future use -
128	Springs Charged
129	Springs Discharged
130	79S Input Enabled
131	79S Input Disabled
132	79M Input Enabled
133	79M Input Disabled
134	TCM Input Closed
135	TCM Input Opened
136	ALT 1 Input Enabled
137	ALT 1 Input Disabled
138	ALT 2 Input Enabled
139	ALT 2 Input Disabled
140	Ext Trip Enabled
141	Ext Trip Disabled
142	Event Cap 1 Init
143	Event Cap 1 Reset
144	Event Cap 2 Init
145	Event Cap 2 Reset
146	Wave Cap Init
147	Wave Cap Reset
148	Ext Close Enabled
149	Ext Close Disabled
150	52a Closed
151	52a Opened
152	52b Closed
153	52b Opened
154	43a Closed
155	43a Opened
156	46 Unit Enabled
157	46 Unit Disabled
158	67P Unit Enabled (DPU2000/R)
159	67P Unit Disabled (DPU2000/R)
160	67N Unit Enabled (DPU2000/R)
161	67N Unit Disabled (DPU2000/R)
162	ULI1 Input Closed (DPU2000/R)
163	ULI1 Input Opened (DPU2000/R)
164	ULI2 Input Closed (DPU2000/R)
165	ULI2 Input Opened (DPU2000/R)
166	ULI3 Input Closed (DPU2000/R)
167	ULI3 Input Opened (DPU2000/R)
168	ULI4 Input Closed (DPU2000/R)
169	ULI4 Input Opened (DPU2000/R)
170	ULI5 Input Closed (DPU2000/R)
171	ULI5 Input Opened (DPU2000/R)
172	ULI6 Input Closed (DPU2000/R)
173	ULI6 Input Opened (DPU2000/R)
174	ULI7 Input Closed (DPU2000/R)
175	ULI7 Input Opened (DPU2000/R)
176	ULI8 Input Closed (DPU2000/R)
177	ULI8 Input Opened (DPU2000/R)

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
178	ULI9 Input Closed (DPU2000/R)
179	ULI9 Input Opened (DPU2000/R)
180	CRI Input Closed
181	CRI Input Opened
182	ARC Blocked
183	ARC Enabled
184	TARC Opened
185	SEF Enabled
186	SEF Disabled
187	User Display Input On
188	User Display Input Off
189	25 TC Enabled (DPU2000/R)
190	25 TC Disabled (DPU2000/R)
191	Lines Synced
192	Line Sync Lost
193	CB Slow
194	Local Disabled
195	Local Enabled
196	25 Bypass Enabled (DPU2000/R)
197	25 Bypass Disabled (DPU2000/R)
198	25 Sync Failed (DPU2000/R)
199	Catalog Number Update
200	- Reserved for future use -
201	- Reserved for future use -
202	- Reserved for future use -
203	- Reserved for future use -
204	- Reserved for future use -
205	- Reserved for future use -
206	- Reserved for future use -
207	- Reserved for future use -
208	- Reserved for future use -
209	- Reserved for future use -
210	- Reserved for future use -
211	- Reserved for future use -
212	- Reserved for future use -
213	- Reserved for future use -
214	- Reserved for future use -
215	59G Alarm (DPU2000R)
216	TGT Enabled (DPU2000R)
217	TGT Disabled (DPU2000R)
218	SIA Enabled (DPU2000R)
219	SIA Disabled (DPU2000R)
220	LIS Asserted (DPU2000R)
221	LIR Asserted (DPU2000R)
222	LIS Deasserted (DPU2000R)
223	LIR Deasserted (DPU2000R)
224	LO Asserted (DPU2000R)
225	LO Deasserted (DPU2000R)
226	TR_SET Asserted (DPU2000R)
227	TR_RST Asserted (DPU2000R)
228	TR_SET Deasserted (DPU2000R)
229	TR_RST Deasserted (DPU2000R)
230	TR_ON Asserted (DPU2000R)
231	TR_OFF Asserted (DPU2000R)

Operation/ Event Number	Operation/Event Record (Register 41547 code definition)
232	TR_TAG Asserted (DPU2000R)
233	59-3P Alarm (DPU2000R)
234	47 Alarm (DPU2000R)
235	21P-1 Zone 1 Trip (DPU2000R)
236	21P-2 Zone 2 Trip (DPU2000R)
237	21P-3 Zone 3 Trip (DPU2000R)
238	21P-4 Zone 4 Trip (DPU2000R)
239	ULI 10 Input Closed (DPU2000R V5.20+)
240	ULI 10 Input Opened (DPU2000R V5.20+)
241	ULI 11 Input Closed (DPU2000R V5.20+)
242	ULI 11 Input Opened (DPU2000R V5.20+)
243	ULI 12 Input Closed (DPU2000R V5.20+)
244	ULI 12 Input Opened (DPU2000R V5.20+)
245	ULI 13 Input Closed (DPU2000R V5.20+)
246	ULI 13 Input Opened (DPU2000R V5.20+)
247	ULI 14 Input Closed (DPU2000R V5.20+)
248	ULI 14 Input Opened (DPU2000R V5.20+)
249	ULI 15 Input Closed (DPU2000R V5.20+)
250	ULI 15 Input Opened (DPU2000R V5.20+)
251	ULI 16 Input Closed (DPU2000R V5.20+)
252	ULI 16 Input Opened (DPU2000R V5.20+)
253	46A Trip (DPU2000R V5.20+)
254	46A Unit Enabled (DPU2000R V5.20+)
255	46A Unit Disabled
256	- Note the operation number can not exceed 255 -

Section 11 - Providing Control Functionality in the DPU2000/1500R/2000R

As described in the beginning of this section, seven groups of control blocks are resident in the DPU2000/DPU 1500R/2000R. Each group is comprised of 6 consecutive registers. The seven control block groups are defined in Table 11-1. The first block within the set of registers determines whether or not the control block requires password control.

ABB relays are designed to operate with a variety of host products. Some host products cannot send a password with the control algorithm. With this in mind, the ABB DPU2000/DPU1500R/2000R allows control with or without password depending upon the setup performed in control register block 62560 through 62598. Register 62598 contains a register as to when the corresponding bit is set, the control block associated with the bit enables or disables password control. Please refer to the 6X Register control section in WinECP help screens for additional information regarding configuration of these registers.

One 4X Register at the beginning of the 4X control register groups is read only which feeds back the status of password control which was configured via Register 62598 (Security Mask Control Block). The register lists the seven control blocks found in the DPU/DPU2000/DPU2000R. Table 11-1 lists the Security Mask register, which reports, which of the control blocks require password control. A status of 1 in the defined bit location allows any value to be placed in the password field (as shown in Table 11-2). A status of 0 in the defined field requires the correct password to be sent as part of the control process.

Figure 11-1 illustrates the Group Blocks within the DPU2000/DPU1500R/2000R and its associated typical control register mapping.

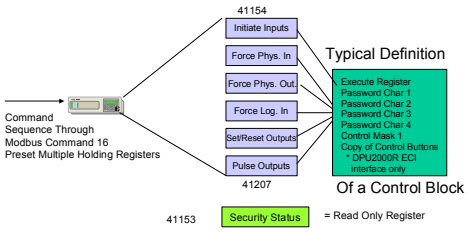


Figure 11-1. Typical Control Features Available for the DPU2000 and DPU1500R/DPU2000R

Table 11-1. Security Status Register Indicating Password Requirement

DPU2000	Notes	Register	Item	Description
Y		41153	16 Bit Unsigned	Security Mask (Read Only, See Register 62598 for setup)
Y			Bit 0 (lsb)	Initiate Input (Group I) Password Required
Y			Bit 1	Force Physical Input (Group II) Password Required
Y			Bit 2	Force Physical Output (Group III) Password Required
Y			Bit 3	Force Logical Input (Group IV) Password Required
Y			Bit 4	Set/ Reset Outputs (Group V) Password Required
Y			Bit 5	Pulse Outputs (Group VI) Password Required
			Bit 6	Initiate control button (Group VII) password required
			Bit 7	Reserved
			Bit 8	Reserved
			Bit 9	Reserved
			Bit 10	Reserved
			Bit 11	Reserved
			Bit 12	Reserved
			Bit 13	Reserved
			Bit 14	Reserved
			Bit 15 (msb)	Reserved
Note: Modbus Command 03 (Read Holding Register) is the only acceptable Modbus command which may access this data. A Modbus Command 16 or 23 is not allowed since this register cannot be manipulated via a read command.				

Note: Value of 0 in the bit location – Correct Password Required for Control Value of 1 in the bit location – any value in password location is allowable to enable control.

One method to perform control through the Control Block is as follows:

- Write all registers other than the register associated with the “Execute Register”.
- Write a “1” to execute the control command.

If an execute command is not written to the register block within 15 seconds after parameters have been configured in the block, the block will be reset and the entire configuration sequence must be re-initiated.

Another method to perform control through the Control Block is to write individual registers to the desired control Group block and then write “1” to the execute register within 15 seconds after all the writes have been completed.

Groups I through VII share commonality in that an operation type must be written to the Execute Register (register 41154 in Group I [INITIATE INPUT], 41160 in Group II [FORCE PHYSICAL INPUT], 41167 in Group III [FORCE PHYSICAL OUTPUT], 41174 in Group IV FORCE LOGICAL INPUT], 41184 in Group V [SET RESET OUTPUTS], and 41196 in Group VII [TOGGLE CONTROL BUTTONS]). Writing a value of 0 to the execute register voids a control execution of the function. Writing a Value of 1 to the execute register allows the function to operate if the consecutive registers are parameterized correctly.

A correct Password may have to be written to the block for the desired function to execute (Registers 41155 and 41156 in Group I [INITIATE INPUT], 41161 and 41162 in Group II [FORCE PHYSICAL INPUT], 41168 and 41169 in Group III [FORCE PHYSICAL OUTPUT], 41175 and 41176 in Group IV [FORCE LOGICAL INPUT], 41185 and 41186 in Group V [SET RESET OUTPUTS] ,41197 and 41198 in Group VII [TOGGLE CONTROL BUTTONS]) 412006-41207. The ABB DPU/DPU2000/DPU1500R/DPU2000R contains a default password of four spaces. If Appendix A is consulted, the ASCII code for a space is 20 (HEX). Thus the numerical value to be sent to the registers corresponding to the default password is 2020 (HEX) for password register 1 and 2020 (HEX) for password register 2.

> **IMPLEMENTATION TIP –** If control does not occur after initiation through the network, verify that the local/remote control bit is not configured in the programmable logical inputs logic or that the local.remote control bit is in the remote state. If the local/remote control bit is configured, and the control switch is in the local position (indicating that control via the network is inhibited), if one of the control commands are sent via the network, a Modbus exception response shall be sent to the host rejecting the command. If the local/remote control bit is not configured, control may take place via the operator interface panel (MMI) or via the network contemporaneously. Additionally, Modbus Registers 40172 through 40175, if read using Modbus Code “03” shall indicated the nature of the communication control errors of the last control function.

Group I Control Features Explained

Group I provides the following functionality:

- Trip
- Close
- Reset Energy Meters
- Reset Demands
- Reset Status
- Reset Targets
- Reset Alarm
- Toggle SCADA Ready

Group I control requires that the control bit be selected in Register 41158 and the same corresponding value should also be placed in 41159. If the values in the registers do not match, control shall not occur.

Table 11-2. Group I Control Registers

DPU2000	Notes	Register	Item	Description
			GROUP I	
Y		41154	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
Y		41155	Password	ASCII – 2 Characters Leftmost Digits
Y		41156	Password	ASCII – 2 Characters Rightmost Digits
Y		41157	Spare	
Y		41158	Change Initiate Input Mask	Unsigned (16 Bits)
Y			Bit 0 (lsb) Initiate CB Trip	1 = Control Bit State 0 = No Control
Y			Bit 1 Initiate CB Close (Based on State of 43a reclosing)	1 = Control Bit State 0 = No Control
Y			Bit 2 Reserved	
Y			Bit 3 Reserved	
Y			Bit 4 Reserved	
Y			Bit 5 Initiate CB Close (Independent of 43a reclosing)	1 = Control Bit State 0 = No Control
Y			Bit 6 Reserved	
Y			Bit 7 Reserved	
Y			Bit 8 Reset Targets	1 = Control Bit State 0 = No Control
Y			Bit 9 Reset Alarms	1 = Control Bit State 0 = No Control
Y			Bit 10 Reset Min/Max demands	1 = Control Bit State 0 = No Control
Y			Bit 11 Reset Relay Status	1 = Control Bit State 0 = No Control
Y			Bit 12 Reset Energy Meters	1 = Control Bit State 0 = No Control
Y	**		Bit 13 Toggle SCADA REDI	1 = Control Bit State 0 = No Control
Y			Bit 14 Reserved	
Y			Bit 15 Reserved (msb)	
Y		41159	Confirm Initiate Input Mask	Unsigned (16 Bits)
Y			Bit 0 (lsb) Initiate CB Trip	1 = Control Bit State 0 = No Control
Y			Bit 1 Initiate CB Close (Based on State of 43a reclosing)	1 = Control Bit State 0 = No Control
Y			Bit 2 Reserved	
Y			Bit 3 Reserved	
Y			Bit 4 Reserved	
Y			Bit 5 Initiate CB Close (Independent of 43a reclosing)	1 = Control Bit State 0 = No Control
Y			Bit 6 Reserved	
Y			Bit 7 Reserved	
Y			Bit 8 Reset Targets	1 = Control Bit State 0 = No Control
Y			Bit 9 Reset Alarms	1 = Control Bit State 0 = No Control
Y			Bit 10 Reset Min/Max demands	1 = Control Bit State 0 = No Control
Y			Bit 11 Reset Relay Status	1 = Control Bit State 0 = No Control
Y			Bit 12 Reset Energy Meters	1 = Control Bit State 0 = No Control
Y	**		Bit 13 Toggle SCADA REDI	1 = Control Bit State 0 = No Control
Y			Bit 14 Reserved	
Y			Bit 15 Reserved (msb)	
** = Version 1.70 Communication Firmware or Greater.				

Figure 11-2 illustrates the command sequence for performing a Circuit Breaker Trip Operation via the Modbus Network. Although the example illustrates that Registers 41155 through 41159 are written in one group, it is possible to send multiple registers in a group or single registers to completely configure this block. It is important

that the execute command (data value = 1 in Register 41154) be sent last to initiate the Trip action on the breaker.

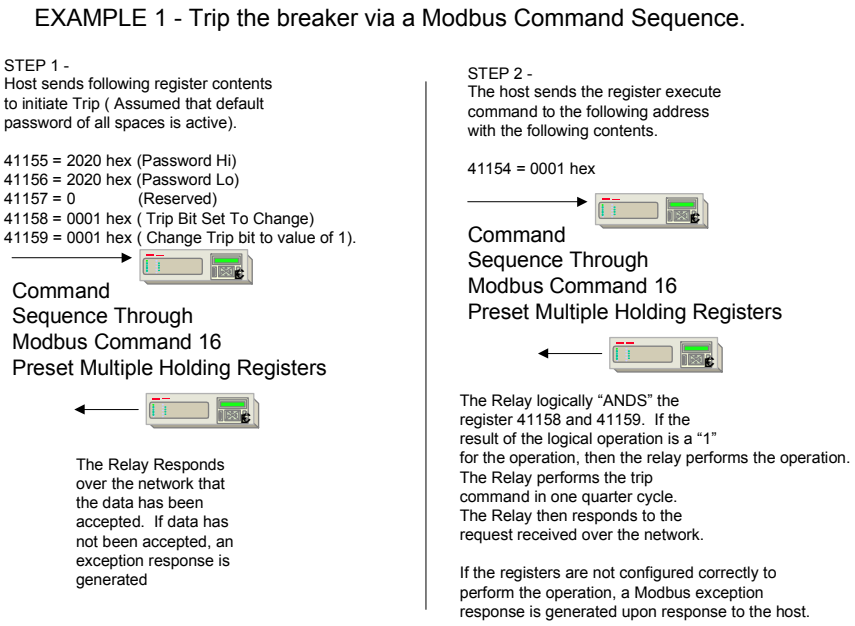


Figure 11-2. Circuit Breaker Trip Operation Via Modbus Network Control

Scada Redi®

In any substation installation, commissioning the installation can be an exceptionally time-consuming procedure. This capability can consume up to 2 days per IED tested. ABB DPU2000 and DPU2000R relays have the capability to allow a read only 4X Registers to be forced from a personal computer through the relay's communication port. Figure 11-1 illustrates the typical DPU2000 and DPU2000R memory map.

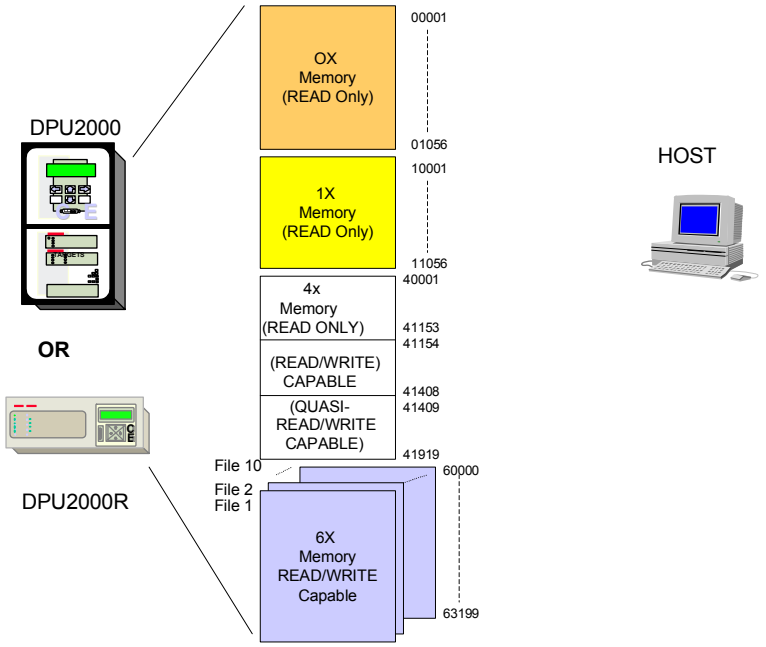


Figure 11-3. Typical Modbus/Modbus Plus Register Definition

During the commissioning process, it is required that the correct data is mapped from the relay to the host device. The conventional method is to have an individual with expensive test gear to apply individual voltages and currents to the relay terminals to simulate field conditions. The individual must be at the substation and a direct link must be made to the individual at the host device verifying the correct data is being received and interpreted correctly.

With 6X memory and some of the 4X memory, a host device can force the read/write capable 4X and 6X memory locations and verify data is sent and received to some memory location. The Scada REdi® provide much more flexibility allowing streamlining of the commissioning process.

Within the DPU2000 and DPU2000R control register memory map a single bit (Bit 13 in Register 41159) may be set to allow READ, WRITE, and READ/WRITE Modbus/Modbus Plus commands to be sent to the previously READ ONLY memory locations. A typical scenario is illustrated in Figures 11-2 and 11-3.

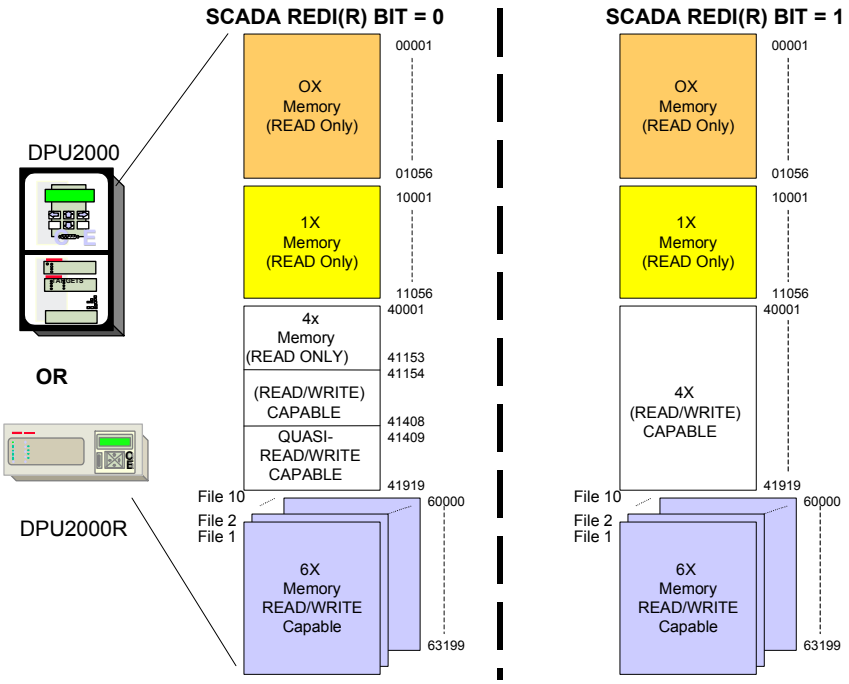


Figure 11-4. Scada Redi Memory Map Modification

As per Figure 11-2, all 4X memory is read/write capable. In other words, Modbus commands 03 –READ HOLDING REGISTERS, 16 – WRITE HOLDING REGISTERS, and 23 WRITE/READ HOLDING REGISTERS, may be used in communicating with the relay. **IT IS MOST IMPORTANT TO REALIZE THAT THE RELAY DISABLES LINK BETWEEN THE PROTECTIVE RELAY AND THE COMMUNCATION CARD (SIMILAR TO THE LOCAL REMOTE FEATURE). PROTECTIVE RELAY PROTECTION STILL OCCURS IF SCADA REDI ® IS SET. ONLY THE COMMUNICATION IS DISABLED BETWEEN THE RELAY AND COMMUNICATION CARD.**

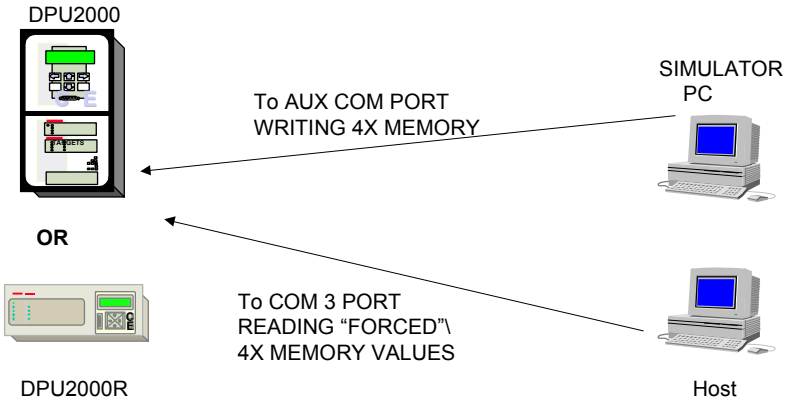


Figure 11-5 Typical Commissioning System

As shown in Figure 11-3, one system (a typical PC operating with a DDE utility and WINDOWS utility for example) could be forcing the registers and the second system, “the host” verifies that the data values are received correctly. Although the illustration shows a direct connect scenario, the Host and Simulator devices may be located offsite and connected to the substation via a modem or fiber optic connection.

Group II Control Features Explained

Group II places each of the Physical Input statuses reported to the processor in the DPU1500R/DPU2000R in to a logical state which is independent of the state of the contact input status present at the Physical Input of the DPU1500R/DPU2000R. There are three modes which a Physical Input status may be placed in:

- NORMAL – The DPU2000R Physical Input Status reflects that of the voltage present at the Physical Input Terminal.
- FORCED ON – The DPU1500R/DPU2000R Physical Input Status reported to the logic of the DPU1500R/DPU2000R processor shall show a state of 1.
- FORCED OFF – The DPU1500R/DPU2000R Physical Input Status reported to the logic of the DPU1500R/DPU2000R processor shall show a state of 0.

The Force Physical Input State is only valid for the DPU1500R/DPU2000R. The Force Physical Input State only affects the state reported to the central processor logic contained within the DPU1500R/DPU2000R. Table 11-3 lists the definition of the control registers and maps each of the internal control bits. Seven Registers are required to perform control for Group II functions.

Table 11-3. Group II Bit Definitions for DPU1500R/DPU2000R Control

DPU2000	Notes	Register	Item	Description
			GROUP II	
N		41160	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
N		41161	Password	ASCII – 2 Characters Leftmost Digits
N		41162	Password	ASCII – 2 Characters Rightmost Digits
N		41163	Spare	
N		41164	Force Physical Input Change Mask	Unsigned (16 Bits)
N			Bit 0 Reserved (lsb)	
N			Bit 1 Reserved	
N			Bit 2 Reserved	
N			Bit 3 Input 1 (Terminal 4)	1 = Control Bit State 0 = No Control
N			Bit 4 Input 2 (Terminal 5)	1 = Control Bit State 0 = No Control
N			Bit 5 Input 3 (Terminal 6)	1 = Control Bit State 0 = No Control
N			Bit 6 Input 4 (Terminal 7)	1 = Control Bit State 0 = No Control
N			Bit 7 Input 5 (Terminal 8)	1 = Control Bit State 0 = No Control
N			Bit 8 Input 6 (Terminal 9)	1 = Control Bit State 0 = No Control
N			Bit 9 Input 7 (Terminal 10)	1 = Control Bit State 0 = No Control
N			Bit 10 Input 8 (Terminal 12)	1 = Control Bit State 0 = No Control
N			Bit 11 Reserved	
N			Bit 12 Reserved	
N			Bit 13 Reserved	
N			Bit 14 Reserved	
N			Bit 15 Reserved (msb)	
N		41165	Force Physical Input Normal State Mask	Unsigned (16 Bits)
N			Bit 0 52a (lsb)	
N			Bit 1 52b	
N			Bit 2 43a	
N			Bit 3 Input 1 (Terminal 4)	1 = Normal State Override 0 = Normal State
N			Bit 4 Input 2 (Terminal 5)	1 = Normal State Override 0 = Normal State
N			Bit 5 Input 3 (Terminal 6)	1 = Normal State Override 0 = Normal State
N			Bit 6 Input 4 (Terminal 7)	1 = Normal State Override 0 = Normal State
N			Bit 7 Input 5 (Terminal 8)	1 = Normal State Override 0 = Normal State

N			Bit 8 Input 6 (Terminal 9)	1 = Normal State Override 0 = Normal State
N			Bit 9 Input 7 (Terminal 10)	1 = Normal State Override 0 = Normal State
N			Bit 10 Input 8 (Terminal 12)	1 = Normal State Override 0 = Normal State
N			Bit 11 Reserved	
N			Bit 12 Reserved	
N			Bit 13 Reserved	
N			Bit 14 Reserved	
N			Bit 15 Reserved (msb)	
N		41166	Force Physical Input Forcing State Mask	Unsigned (16 Bits)
N			Bit 0 52a (lsb)	
N			Bit 1 52b	
N			Bit 2 43a	
N			Bit 3 Input 1 (Terminal 4)	1 = Force Set State 0 = Force Reset State
N			Bit 4 Input 2 (Terminal 5)	1 = Force Set State 0 = Force Reset State
N			Bit 5 Input 3 (Terminal 6)	1 = Force Set State 0 = Force Reset State
N			Bit 6 Input 4 (Terminal 7)	1 = Force Set State 0 = Force Reset State
N			Bit 7 Input 5 (Terminal 8)	1 = Force Set State 0 = Force Reset State
N			Bit 8 Input 6 (Terminal 9)	1 = Force Set State 0 = Force Reset State
N			Bit 9 Input 7 (Terminal 10)	1 = Force Set State 0 = Force Reset State
N			Bit 10 Input 8 (Terminal 12)	1 = Force Set State 0 = Force Reset State
N			Bit 11 Reserved	
N			Bit 12 Reserved	
N			Bit 13 Reserved	
N			Bit 14 Reserved	
N			Bit 15 Reserved (msb)	
** = Version 1.70 Communication Firmware or Greater.				

Group II functions operate as follows:

Register 41164 = Force Physical Input Change Mask - Selects Control for the Function Specified.
Register 41165 = Force Physical Input Normal State Mask - Places Bit in Normal or Force Mode.
Register 41166 = Physical Input Forcing State Mask - If Bit is in Force Mode, Determines Force State.

A Truth Table for the aforementioned bits follows as illustrated in Table 11-4.

Table 11-4. State Truth Chart for Physical Input Forcing Function

Bit Value Change Mask Register 41164	Bit Value Normal/Forced Mask Register 41165	Bit Value Forced State Register 41166	Description
0	X	X	Normal - State follows Voltage at Term.
1	0	X	Normal – State follows Voltage at Term.
1	1	0	Input Forced – State = OFF
1	1	1	Input Forced – State = ON
Note: X = Don't Care State			

Once an input is forced on or off, it must be "unforced" or returned to normal state for the point to resume normal operation and reflect the state present at the physical input terminals present at the rear of the relay. **It is important to emphasize that the forced states are stored in the DPU1500R/DPU 2000R's non-volatile RAM and will remain forced until unforced by the operator. A point may be "unforced" via the front panel MMI, DOS ECP, WinECP, or through the Modbus commands covered within this section.**

A simple example illustrates the Force/Normal control sequence via the Modbus command operations. Figures 11-3, 11-4, and 11-5 illustrate the word patterns which must be transmitted to the DPU1500R/DPU2000R to complete a Force On, Force Off and Return to Normal State Operation within the DPU1500R/DPU2000R. As with the other control functions, the registers may be sent down individually, in blocks of data transferred, or as one block of data followed by an execute command as illustrated in Figures 11-3, 11-4, and 11-5.

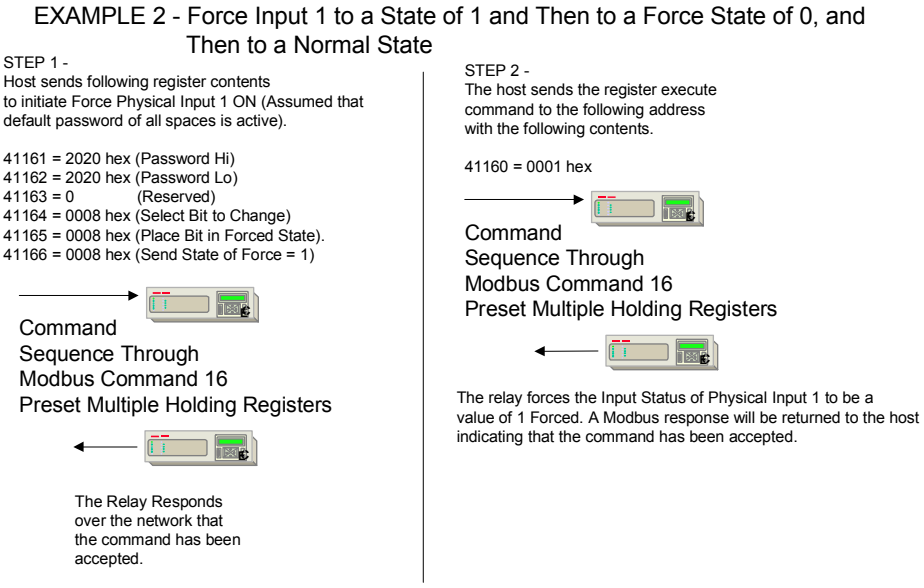


Figure 11-6a. Force Physical Input Example

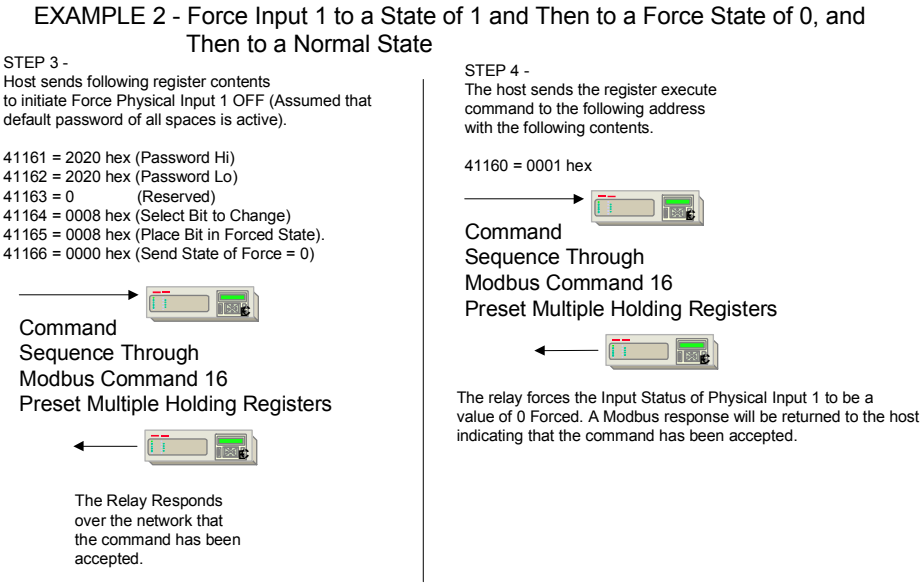


Figure 11-6b. Force Physical Input Example (Continued)

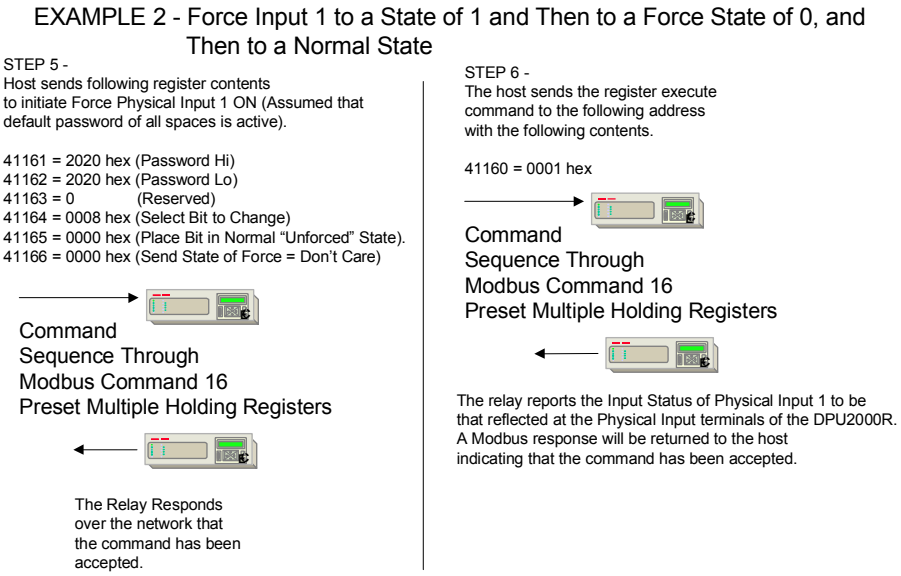


Figure 11-6c. Force Physical Input Example (Continued)

IMPLEMENTATION TIP – As is common practice with any control, after a control task has been completed via the network, the host should query the device to assure that control has been executed.

Group III Control Features Explained

The complimentary control functions are available for forcing the Physical Output contacts located at the back of the relay. The Physical Output force functions follows that of the Physical Input Force Functionality. There are three modes which a Physical Output may be placed:

- NORMAL – The DPU2000R Physical Output reflects that of the logic configured within the protective relay.
- FORCED ON – The DPU1500R/DPU2000R Physical Output is energized. The Physical Output status is reported as a 1. If the point status is viewed via ECP or WinECP, the point will show a forced status.
- FORCED OFF – The DPU1500R/DPU2000R Physical Output is de-energized. The Physical Output status is reported as a 0. If the point status is viewed via ECP or WinECP, the point will show a forced status.

Table 11-5 illustrates the mapping for Physical Output Forcing Capabilities.

Table 11-5. DPU1500R/DPU2000R Bit Control Function Definitions

DPU2000	Register	Item	Description
		GROUP III	
N	41167	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
N	41168	Password	ASCII – 2 Characters Leftmost Digits
N	41169	Password	ASCII – 2 Characters Rightmost Digits
N	41170	Spare	
N	41171	Force Physical Output Change Mask	Unsigned (16 Bits)
N		Bit 0 Trip (lsb)	
N		Bit 1 Close	
N		Bit 2 Output 1 (Terminals 28,27)	1 = Control Bit State 0 = No Control
N		Bit 3 Output 2 (Terminal 26,25)	1 = Control Bit State 0 = No Control

N		Bit 4 Output 3 (Terminal 24,23)	1 = Control Bit State 0 = No Control
N		Bit 5 Output 4 (Terminal 22 21)	1 = Control Bit State 0 = No Control
N		Bit 6 Output 5 (Terminal 19,20)	1 = Control Bit State 0 = No Control
N		Bit 7 Output 6 (Terminals 17,18)	1 = Control Bit State 0 = No Control
N		Bit 8 Reserved	
N		Bit 9 Reserved	
N		Bit 10 Reserved	
N		Bit 11 Reserved	
N		Bit 12 Reserved	
N		Bit 13 Reserved	
N		Bit 14 Reserved	
N		Bit 15 Reserved (msb)	
N	41172	Force Physical Output Normal State Mask	Unsigned (16 Bits)
N		Bit 0 Trip (lsb)	
N		Bit 1 Close	
N		Bit 2 Output 1 (Terminals 28,27)	1 = Normal State Override 0 = Normal State
N		Bit 3 Output 2 (Terminal 26,25)	1 = Normal State Override 0 = Normal State
N		Bit 4 Output 3 (Terminal 24,23)	1 = Normal State Override 0 = Normal State
N		Bit 5 Output 4 (Terminal 22 21)	1 = Normal State Override 0 = Normal State
N		Bit 6 Output 5 (Terminal 19,20)	1 = Normal State Override 0 = Normal State
N		Bit 7 Output 6 (Terminals 17,18)	1 = Normal State Override 0 = Normal State
N		Bit 8 Reserved	
N		Bit 9 Reserved	
N		Bit 10 Reserved	
N		Bit 11 Reserved	
N		Bit 12 Reserved	
N		Bit 13 Reserved	
N		Bit 14 Reserved	
N		Bit 15 Reserved (msb)	
N	41173	Force Physical Input Forcing State Mask	Unsigned (16 Bits)
N		Bit 0 Trip (lsb)	
N		Bit 1 Close	
N		Bit 2 Output 1 (Terminals 28,27)	1 = Force Set State 0 = Force Reset State
N		Bit 3 Output 2 (Terminal 26,25)	1 = Force Set State 0 = Force Reset State
N		Bit 4 Output 3 (Terminal 24,23)	1 = Force Set State 0 = Force Reset State
N		Bit 5 Output 4 (Terminal 22 21)	1 = Force Set State 0 = Force Reset State
N		Bit 6 Output 5 (Terminal 19,20)	1 = Force Set State 0 = Force Reset State
N		Bit 7 Output 6 (Terminals 17,18)	1 = Force Set State 0 = Force Reset State
N		Bit 8 Reserved	
N		Bit 9 Reserved	
N		Bit 10 Reserved	
N		Bit 11 Reserved	
N		Bit 12 Reserved	
N		Bit 13 Reserved	
N		Bit 14 Reserved	
N		Bit 15 Reserved (msb)	

Group III functions operate as follows:

Register 41171 = Force Physical Output Change Mask - Selects Control for the Function Specified.
Register 41172 = Force Physical Output Normal State Mask - Places Bit in Normal or Force Mode.

Register 41173 = Physical Output Forcing State Mask – If Bit is in Force Mode, Determines Force State. (State 1 = energized State 0 = de-energized).

A Truth Table for the aforementioned bits follows as illustrated in Table 11-6.

Table 11-6. State Truth Chart for Physical Input Forcing Function

Bit Value Change Mask Register 41171	Bit Value Normal/Forced Mask Register 41172	Bit Value Forced State Register 41173	Description
0	X	X	Normal – State follows Voltage at Term.
1	0	X	Normal – State follows Voltage at Term.
1	1	0	Output Forced – State = OFF
1	1	1	Output Forced – State = ON
Note: X = Don't Care State			

Once an Output is forced on or off, it must be " unforced" or returned to normal state for the point to resume normal operation and reflect the state present at the physical Output terminals present at the rear of the relay. **It is important to emphasize that the forced states are stored in the DPU1500R/DPU2000R's non-volatile RAM and will remain forced until unforced by the operator. A point may be "unforced" via the front panel MMI, DOS ECP, WinECP, or through the Modbus commands covered within this section.**

A simple example shall illustrate the Force/Normal control sequence via the Modbus command operations. Figures 11-6, 11-7, and 11-8 illustrate the word patterns which must be transmitted to the DPU1500R/DPU2000R to complete a Force On, Force Off and Return to Normal State Operation within the DPU1500R/DPU2000R. As with the other control functions, the registers may be sent down individually, in blocks of data transferred, or as one block of data followed by an execute command as illustrated in Figures 11-6, 11-7, and 11-8.

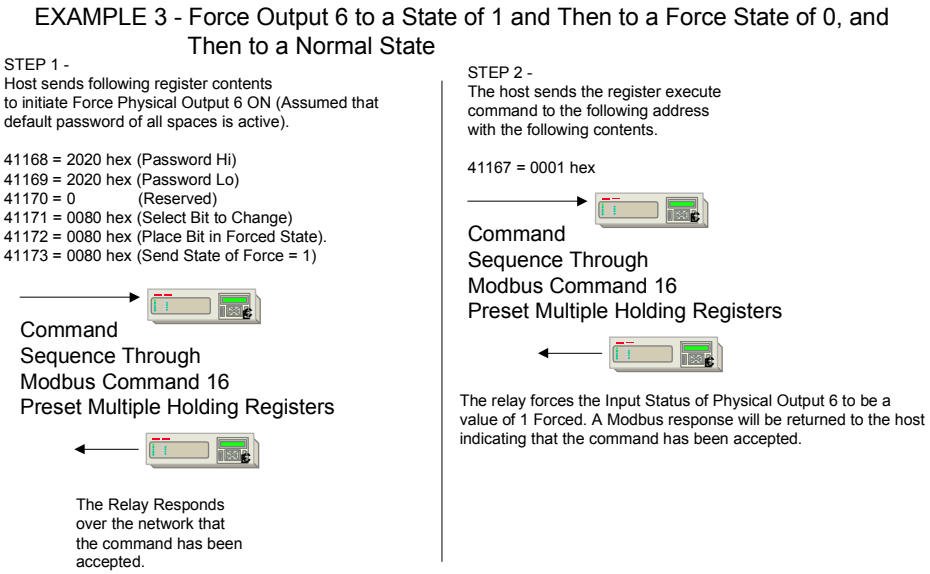


Figure 11-7a. Force Physical Output Example

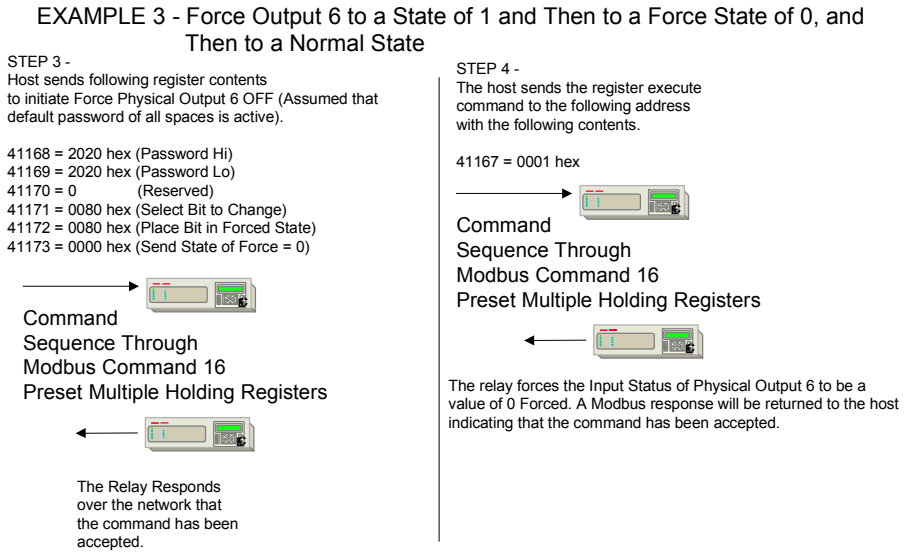


Figure 11-7b. Force Physical Output Example (Continued)

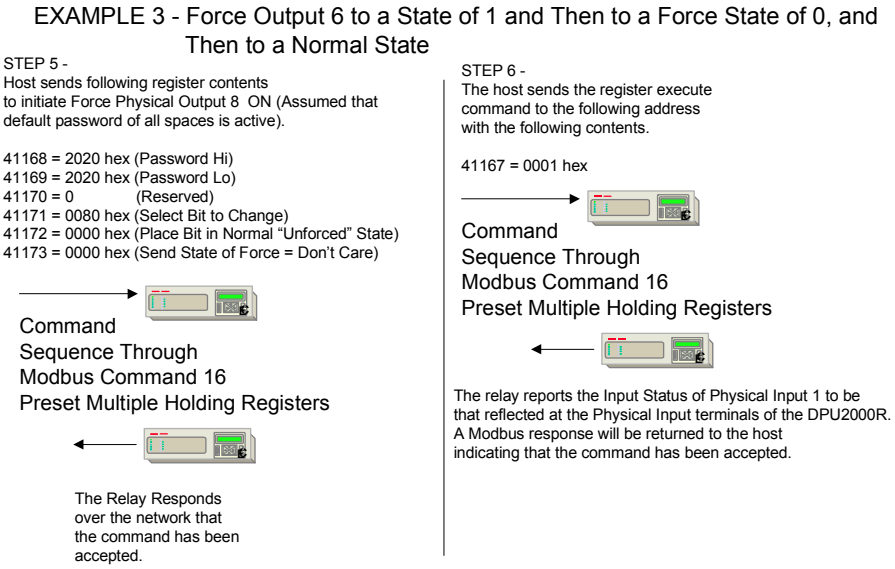


Figure 11-7c. Force Physical Output Example (Continued)

IMPLEMENTATION TIP – As is common practice with any control, after a control task has been completed via the network, the host should query the device to assure that control has been executed.

Group IV Control Features Explained

The DPU2000 and DPU1500R/DPU2000R have the capability of automation configuration to a generic Logical Input bit. These bits are generic in nature and can be mapped via ECP (External Communication Program) or WinECP (Windows External Communication Program). Mapping of the values occurs as such:

1. From ECP or WinECP select the menu item "FLI Index and User Name" selection.
2. A list of default mappings are shown as in Figure 11-8 (ECP Screen) In this case the user is viewing the screen in ECP as shown in the CHANGE SETTINGS Screen.
3. The default list corresponds to the Logical Input mapping of Logical Inputs (hereto referred as LI) as illustrated in Table 11-7.

4. If one would wish to change the relay protective function element mapped to the specific LI, depress the “ENTER” key. The display in Figure 11-9 shall result.

5. The user would then scroll down the list and highlight the element desired to be mapped to the specific LI within the edited list.

6. Depress the “ENTER” key to map the selected element into the table.

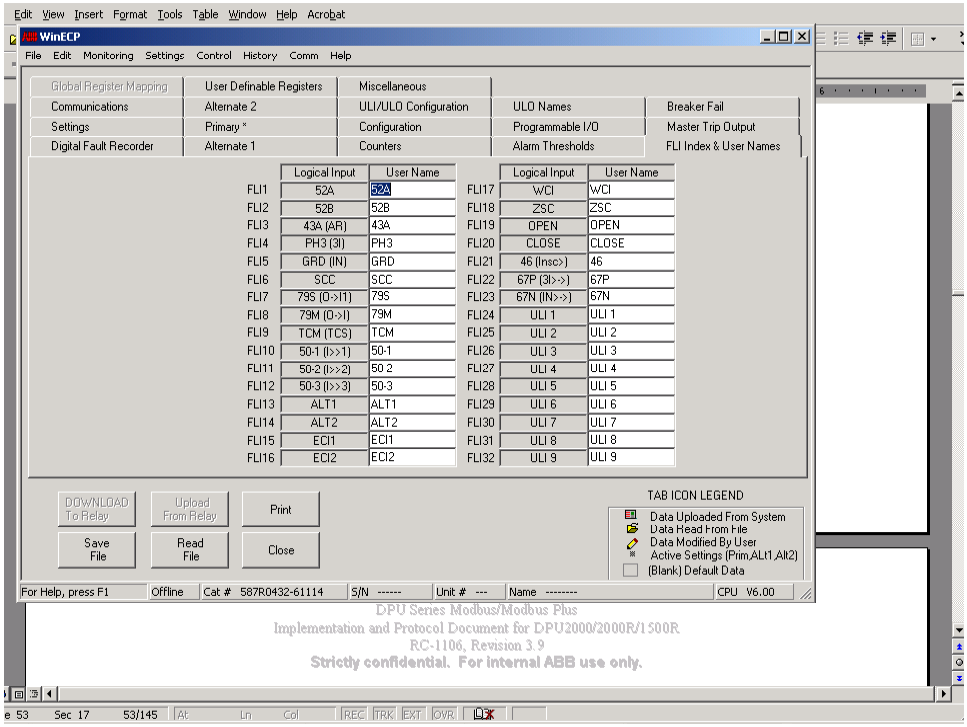


Figure 11-8. ECP Default Logical Input List

Table 11-7. ECP Default Correlation to Forced Logical Input Bit Map

FLI Number	Description	User Name	FLI Number	Description	User Name
FLI 01	Relay Status	52a	FLI 17	Initiate Close Output	CLOSE
FLI 02	Relay Status	52b	FLI 18	Event Capture Initiate	ECI 1
FLI 03	Reclosing Enable	43a	FLI 19	Event Capture Initiate	ECI 2
FLI 04	Trip Coil Monitor	TCM	FLI 20	Waveform Capture Initate	WCI
FLI 05	Ground Protection Overcurrent 51N/50N-1/50N-2 Enable	GRD	FLI 21	Negative Sequence Time Overcurrent Enable	46
FLI 06	Phase Protection Overcurrent 51P/50P-1/50P-2 Enable	PH3	FLI 22	Positive Sequential Directional Control Time Overcurrent Enable	67P
FLI 07	Phase & Ground Instantaneous Level 1 Enable	50-1	FLI 23	Negative Sequence Directional Control Ground Overcurrent Enable	67N
FLI 08	Phase & Ground Instantaneous Level 2 Enable	50-2	FLI 24	User Logical Input 1	ULI 1
FLI 09	Phase & Ground Instantaneous Level 3 Enable	50-3	FLI 25	User Logical Input 2	ULI 2
FLI 10	Alternate Relay Setting 1	ALT 1	FLI 26	User Logical Input 3	ULI 3
FLI 11	Alternate Relay Setting 2	ALT 2	FLI 27	User Logical Input 4	ULI 4
FLI 12	Zone Sequence Control	ZSC	FLI 28	User Logical Input 5	ULI 5
FLI 13	Spring Charging Contact	SCC	FLI 29	User Logical Input 6	ULI 6
FLI 14	Single Shot Reclosing Enable	79S	FLI 30	User Logical Input 7	ULI 7

FLI 15	Multi-Shot Reclosing Enable	79M	FLI 31	User Logical Input 8	ULI 8
FLI 16	Initiate Trip Output	OPEN	FLI 32	User Logical Input 9	ULI 9

The usefulness of this feature cannot be understated. Each one of these functions can be forced via a network control. Programming need not be done to allow for function control via a network. If the relaying feature "RECLOSING" were to be enabled, the bit FLI 03 could be forced to an "ON" condition via the network control. If a desired control function were to be controlled via the network, then ECP mapping would have to be configured as per Figure 11-9. The method employed to force the state of the function is similar to that of the Group II and III functions. As illustrated in Table 11-8, the mapping of each of the FLI's is illustrated. Registers 41174 through 41183 allow forcing of the desired feature.

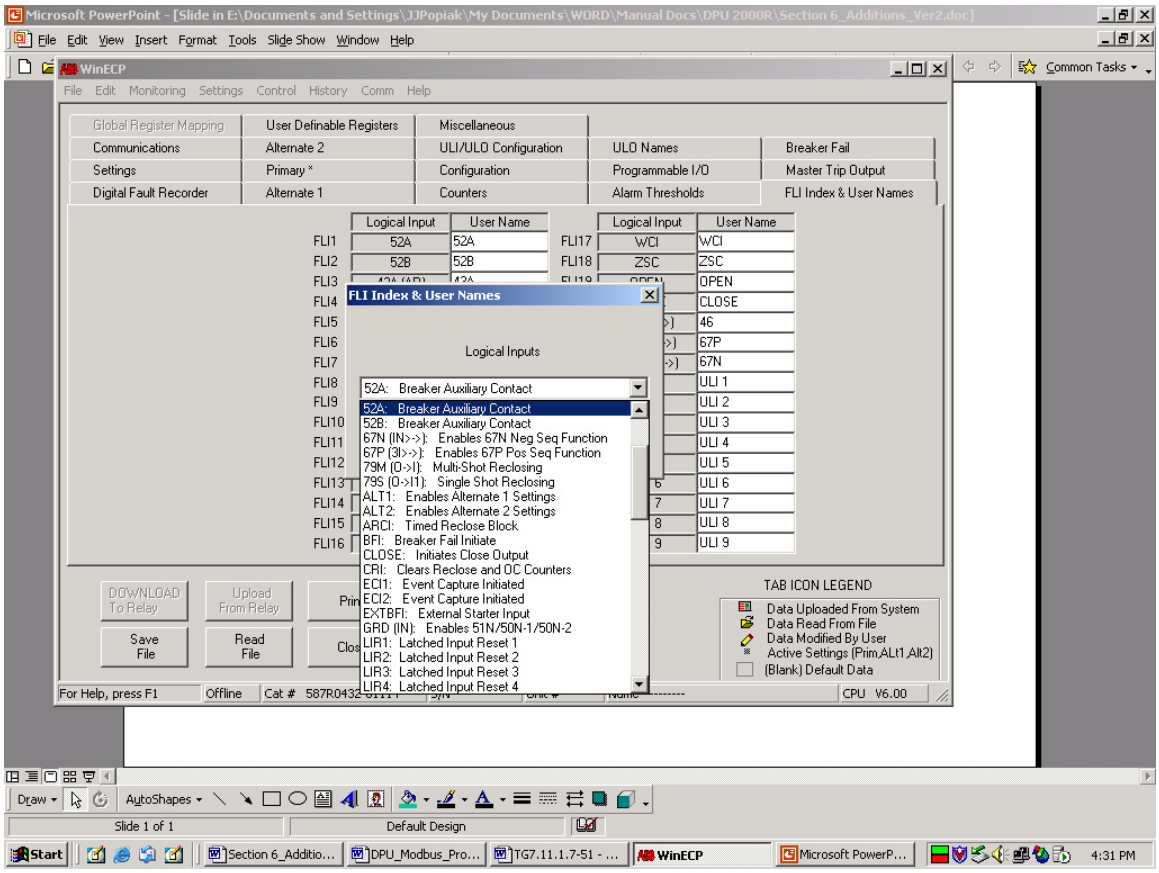


Figure 11-9. Mapping Function Screen for Logical Inputs

Group IV functions operate as follows:

Register 41178 = Force Physical Output Change Mask - Selects Control for FLI 17 – FLI 32.
Register 41179 = Force Physical Output Change Mask - Selects Control for FLI 01 – FLI 16.
Register 41180 = Force Physical Output Normal State Mask - Places FLI 17 – FLI 32 in Normal or Force Mode.
Register 41181 = Force Physical Output Normal State Mask - Places FLI 01 – FLI 16 in Normal or Force Mode.
Register 41182 = Physical Output Forcing State Mask – If Bit is in Force Mode, Determines Force State FLI 17 to FLI 32 (State 1 = energized State 0 = de-energized).
Register 41183 = Physical Output Forcing State Mask – If Bit is in Force Mode, Determines Force State FLI 01 to FLI 16 (State 1 = energized State 0 = de-energized).

A Truth Table for the aforementioned bits follows as illustrated in Table 11-8.

Table 11-8. State Truth Chart for Physical Input Forcing Function

Bit Value	Bit Value	Bit Value	Description

Change Mask Register 41178 and 41179	Normal/Forced Mask Register 41180 and 41181	Forced State Register 41182 and 41183	
0	X	X	Normal – State Unforced.
1	0	X	Normal – State Unforced.
1	1	0	Logical Input Forced – State = OFF
1	1	1	Logical Input Forced – State = ON
Note: X = Don't Care State			

There are three modes which a Physical Output may be placed:

- UNFORCED – The DPU2000R Logical Input is not forced to any state.
- FORCED ON – The DPU1500R/DPU2000R Logical Input is energized and associated mapped function is enabled. The Logical Input status is reported as a 1. If the point status is viewed via ECP or WIN ECP, the Logical point will show a forced status with a logical state of 1.
- FORCED OFF – The DPU1500R/DPU2000R Logical Input is de-energized. The Logical Input status is reported as a 0. If the point status is viewed via ECP or WinECP, the point will show a forced status with a logical state of 0.

Table 11-9. DPU2000 and DPU1500R/DPU2000R Bit Control Function Definitions

DPU2000	Register	Item	Description
		GROUP IV	
Y	41174	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
Y	41175	Password	ASCII – 2 Characters Leftmost Digits
Y	41176	Password	ASCII – 2 Characters Rightmost Digits
Y	41177	Spare	
Y	41178	Force Logical Input Change Mask FLI 17 to FLI 32	Unsigned (16 Bits) 1 = Control Bit State 0 = No Control
Y		Bit 0 FLI 17 (lsb)	1 = Control Bit State 0 = No Control
Y		Bit 1 FLI 18	1 = Control Bit State 0 = No Control
Y		Bit 2 FLI 19	1 = Control Bit State 0 = No Control
Y		Bit 3 FLI 20	1 = Control Bit State 0 = No Control
Y		Bit 4 FLI 21	1 = Control Bit State 0 = No Control
Y		Bit 5 FLI 22	1 = Control Bit State 0 = No Control
Y		Bit 6 FLI 23	1 = Control Bit State 0 = No Control
Y		Bit 7 FLI 24	1 = Control Bit State 0 = No Control
Y		Bit 8 FLI 25	1 = Control Bit State 0 = No Control
Y		Bit 9 FLI 26	1 = Control Bit State 0 = No Control
Y		Bit 10 FLI 27	1 = Control Bit State 0 = No Control
Y		Bit 11 FLI 28	1 = Control Bit State 0 = No Control
Y		Bit 12 FLI 29	1 = Control Bit State 0 = No Control
Y		Bit 13 FLI 30	1 = Control Bit State 0 = No Control
Y		Bit 14 FLI 31	1 = Control Bit State 0 = No Control
Y		Bit 15 FLI 32 (msb)	1 = Control Bit State 0 = No Control
Y	41179	Force Logical Input Change Mask FLI 01 to FLI 16	Unsigned (16 Bits) 1 = Control Bit State 0 = No Control
Y		Bit 0 FLI 01 (lsb)	1 = Control Bit State 0 = No Control
Y		Bit 1 FLI 02	1 = Control Bit State 0 = No Control
Y		Bit 2 FLI 03	1 = Control Bit State 0 = No Control
Y		Bit 3 FLI 04	1 = Control Bit State 0 = No Control
Y		Bit 4 FLI 05	1 = Control Bit State 0 = No Control
Y		Bit 5 FLI 06	1 = Control Bit State 0 = No Control
Y		Bit 6 FLI 07	1 = Control Bit State 0 = No Control

Y		Bit 7 FLI 08	1 = Control Bit State 0 = No Control
Y		Bit 8 FLI 09	1 = Control Bit State 0 = No Control
Y		Bit 9 FLI 10	1 = Control Bit State 0 = No Control
Y		Bit 10 FLI 11	1 = Control Bit State 0 = No Control
Y		Bit 11 FLI 12	1 = Control Bit State 0 = No Control
Y		Bit 12 FLI 13	1 = Control Bit State 0 = No Control
Y		Bit 13 FLI 14	1 = Control Bit State 0 = No Control
Y		Bit 14 FLI 15	1 = Control Bit State 0 = No Control
Y		Bit 15 FLI 16 (msb)	1 = Control Bit State 0 = No Control
Y	41180	Force Logical Input Normal State Mask	Unsigned (16 Bits)
Y		Bit 0 FLI 17 (lsb)	1 = Force State 0 = Normal State
Y		Bit 1 FLI 18	1 = Force State 0 = Normal State
Y		Bit 2 FLI 19	1 = Force State 0 = Normal State
Y		Bit 3 FLI 20	1 = Force State 0 = Normal State
Y		Bit 4 FLI 21	1 = Force State 0 = Normal State
Y		Bit 5 FLI 22	1 = Force State 0 = Normal State
Y		Bit 6 FLI 23	1 = Force State 0 = Normal State
Y		Bit 7 FLI 24	1 = Force State 0 = Normal State
Y		Bit 8 FLI 25	1 = Force State 0 = Normal State
Y		Bit 9 FLI 26	1 = Force State 0 = Normal State
Y		Bit 10 FLI 27	1 = Force State 0 = Normal State
Y		Bit 11 FLI 28	1 = Force State 0 = Normal State
Y		Bit 12 FLI 29	1 = Force State 0 = Normal State
Y		Bit 13 FLI 30	1 = Force State 0 = Normal State
Y		Bit 14 FLI 31	1 = Force State 0 = Normal State
Y		Bit 15 FLI 32 (msb)	1 = Force State 0 = Normal State
Y	41181	Force Logical Input Normal State Mask	Unsigned (16 Bits)
Y		Bit 0 FLI 01 (lsb)	1 = Force State 0 = Normal State
Y		Bit 1 FLI 02	1 = Force State 0 = Normal State
Y		Bit 2 FLI 03	1 = Force State 0 = Normal State
Y		Bit 3 FLI 04	1 = Force State 0 = Normal State
Y		Bit 4 FLI 05	1 = Force State 0 = Normal State
Y		Bit 5 FLI 06	1 = Force State 0 = Normal State
Y		Bit 6 FLI 07	1 = Force State 0 = Normal State
Y		Bit 7 FLI 08	1 = Force State 0 = Normal State
Y		Bit 8 FLI 09	1 = Force State 0 = Normal State
Y		Bit 9 FLI 10	1 = Force State 0 = Normal State
Y		Bit 10 FLI 11	1 = Force State 0 = Normal State
Y		Bit 11 FLI 12	1 = Force State 0 = Normal State
Y		Bit 12 FLI 13	1 = Force State 0 = Normal State
Y		Bit 13 FLI 14	1 = Force State 0 = Normal State
Y		Bit 14 FLI 15	1 = Force State 0 = Normal State
Y		Bit 15 FLI 16 (msb)	1 = Force State 0 = Normal State
Y	41182	Force Logical Input State Mask FLI 17 – FLI 32	Unsigned (16 Bits)
Y		Bit 0 FLI 17 (lsb)	1 = Force State 0 = Normal State
Y		Bit 1 FLI 18	1 = Force State 0 = Normal State
Y		Bit 2 FLI 19	1 = Force State 0 = Normal State
Y		Bit 3 FLI 20	1 = Force State 0 = Normal State
Y		Bit 4 FLI 21	1 = Force State 0 = Normal State
Y		Bit 5 FLI 22	1 = Force State 0 = Normal State
Y		Bit 6 FLI 23	1 = Force State 0 = Normal State
Y		Bit 7 FLI 24	1 = Force State 0 = Normal State

Y		Bit 8 FLI 25	1 = Force State 0 = Normal State
Y		Bit 9 FLI 26	1 = Force State 0 = Normal State
Y		Bit 10 FLI 27	1 = Force State 0 = Normal State
Y		Bit 11 FLI 28	1 = Force State 0 = Normal State
Y		Bit 12 FLI 29	1 = Force State 0 = Normal State
Y		Bit 13 FLI 30	1 = Force State 0 = Normal State
Y		Bit 14 FLI 31	1 = Force State 0 = Normal State
Y		Bit 15 FLI 32 (msb)	1 = Force State 0 = Normal State
Y	41183	Force Logical Input State Mask FLI 01 – FLI 16	Unsigned (16 Bits)
Y		Bit 0 FLI 01 (lsb)	1 = Force Set State 0 = Force Reset State
Y		Bit 1 FLI 02	1 = Force Set State 0 = Force Reset State
Y		Bit 2 FLI 03	1 = Force Set State 0 = Force Reset State
Y		Bit 3 FLI 04	1 = Force Set State 0 = Force Reset State
Y		Bit 4 FLI 05	1 = Force Set State 0 = Force Reset State
Y		Bit 5 FLI 06	1 = Force Set State 0 = Force Reset State
Y		Bit 6 FLI 07	1 = Force Set State 0 = Force Reset State
Y		Bit 7 FLI 08	1 = Force Set State 0 = Force Reset State
Y		Bit 8 FLI 09	1 = Force Set State 0 = Force Reset State
Y		Bit 9 FLI 10	1 = Force Set State 0 = Force Reset State
Y		Bit 10 FLI 11	1 = Force Set State 0 = Force Reset State
Y		Bit 11 FLI 12	1 = Force Set State 0 = Force Reset State
Y		Bit 12 FLI 13	1 = Force Set State 0 = Force Reset State
Y		Bit 13 FLI 14	1 = Force Set State 0 = Force Reset State
Y		Bit 14 FLI 15	1 = Force Set State 0 = Force Reset State
Y		Bit 15 FLI 16 (msb)	1 = Force Set State 0 = Force Reset State

A simple application example in Figure 11-10 follows, illustrating the method to force DPU2000 or DPU1500R/DPU2000R functions via the Group IV mapping.

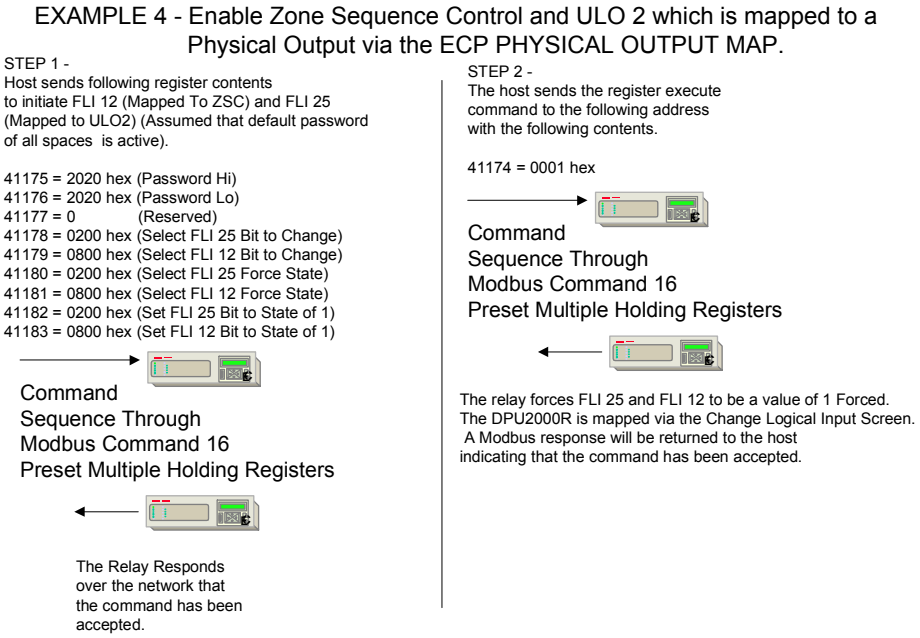


Figure 11-10. Application Example Illustrating the Use of FLI Group IV Methodology

Group V Control Features Explained

Group V control functions allow the resetting of specific alarms and/or the setting AND resetting of ULO states. Group I allows certain reset of alarms, targets, as well as other features. Group V allows reset of individual DPU2000 and DPU1500R/DPU2000R alarm status bits. Within Tables 11-10 and 11-11, the mapping is described for controlled reset of the specific elements. Table 11-11 contains a mapping of which bits only are controlled by reset commands.

Group V functions operate as follows:

Register 41188 = Set/Reset Change Mask - Features 1
Register 41189 = Set/Reset Change Mask - Features 2
Register 41190 = Set/Reset Change Mask - Features 3
Register 41191 = Set/Reset Change Mask - Features 4
Register 41192 = Set/Reset State Change - For Features 1
Register 41193 = Set/Reset State Change - For Features 2
Register 41194 = Set/Reset State Change - For Features 3
Register 41195 = Set/Reset State Change - For Features 4

A Truth Table for the aforementioned bits follows as illustrated in Table 11-10.

Table 11-10. State Truth Chart for Physical Input Forcing Function

Bit Value Change Mask Register 41188 through 41191	Bit Value Normal/Forced Mask Register 41192 through 41195	Description
0	X	Normal - State Unforced.
1	0	Logical Input Forced – State = OFF
1	1	Logical Input Forced – State = ON

There are three modes which a Physical Output may be placed:

- UNFORCED – The DPU2000R Logical Input is not forced to any state.
- SET – The DPU1500R/DPU2000R bit is set to a value of 1.
- RESET – The DPU1500R/DPU2000R is set to a value of 0.

It should be noted that certain bits within the table can only be reset when selected. Other bits may be set or reset at will. Once a bit is forced, the NORMAL LED (located at the faceplate of the DPU2000 and 2000R) shall flash. The Normal LED is green in color.

Table 11-11. DPU2000 and DPU1500R/DPU2000R Bit Control Function Definitions

DPU2000	Notes	Register	Item	Description
			GROUP V	
Y		41184	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
Y		41185	Password	ASCII – 2 Characters Leftmost Digits
Y		41186	Password	ASCII – 2 Characters Rightmost Digits
Y		41187	Spare	
Y		41188	Change Mask Register 1	
Y	R		Bit 15 - Under Voltage Trip 27	1 = Select bit 0 = Normal (msb)
Y	R		Bit 14 - Negative Sequence Overcurrent Trip – 46	1 = Select bit 0 = Normal
Y	R		Bit 13 - Phase Instantaneous Overcurrent Trip – 1 50P1	1 = Select bit 0 = Normal

Y	R		Bit 12 - Neutral Instantaneous Overcurrent Trip – 1 50N1	1 = Select bit 0 = Normal
Y	R		Bit 11 - Phase Instantaneous Overcurrent Trip – 2 50P2	1 = Select bit 0 = Normal
Y	R		Bit 10 - Neutral Instantaneous Overcurrent Trip – 2 50N2	1 = Select bit 0 = Normal
Y	R		Bit 9 - Phase Instantaneous Overcurrent Trip – 3 50P3	1 = Select bit 0 = Normal
Y	R		Bit 8 - Neutral Instantaneous Overcurrent Trip – 3 50N3	1 = Select bit 0 = Normal
Y	R		Bit 7 - Phase Time Overcurrent Trip – 51P	1 = Select bit 0 = Normal
Y	R		Bit 6 - Neutral Time Overcurrent Trip – 51N	1 = Select bit 0 = Normal
Y	R		Bit 5 - Over Voltage Trip – 59	1 = Select bit 0 = Normal
Y	R		Bit 4 - Directional Overcurrent Trip (Positive Sequence) – 67P	1 = Select bit 0 = Normal
Y	R		Bit 3 - Directional Overcurrent Trip (Negative Sequence) – 67N	1 = Select bit 0 = Normal
Y	R		Bit 2 - Frequency Shed (1st Stage) – 81 S-1	1 = Select bit 0 = Normal
Y	R		Bit 1 - Frequency Restore (1st Stage) – 81 R-1	1 = Select bit 0 = Normal
Y	R		Bit 0 - Over Frequency (1st Stage) – 81 O-1	1 = Select bit 0 = Normal (lsb)
		41189	Change Mask Register 2	
Y	R		Bit 15 - Phase Under Voltage Trip – 27-3P	1 = Select bit 0 = Normal (msb)
Y	R		Bit 14 - Single Pole Trip (Phase A) – TRIP A	1 = Select bit 0 = Normal
Y	R		Bit 13 - Single Pole Trip (Phase B) – TRIP B	1 = Select bit 0 = Normal
Y	R		Bit 12 - Single Pole Trip (Phase C) – TRIP C	1 = Select bit 0 = Normal
Y			Bit 11 - User Logical Output 1 – ULO 1	1 = Select bit 0 = Normal
Y			Bit 10 - User Logical Output 2 – ULO 2	1 = Select bit 0 = Normal
Y			Bit 9 - User Logical Output 3 – ULO 3	1 = Select bit 0 = Normal
Y			Bit 8 - User Logical Output 4 – ULO 4	1 = Select bit 0 = Normal
Y			Bit 7 - User Logical Output 5 – ULO 5	1 = Select bit 0 = Normal
Y			Bit 6 - User Logical Output 6 – ULO 6	1 = Select bit 0 = Normal
Y			Bit 5 - User Logical Output 7 – ULO 7	1 = Select bit 0 = Normal
Y			Bit 4 - User Logical Output 8 – ULO 8	1 = Select bit 0 = Normal
Y			Bit 3 - User Logical Output 9 – ULO 9	1 = Select bit 0 = Normal
Y	R		Bit 2 - Over Frequency (2nd Stage) – 81O-2	1 = Select bit 0 = Normal
Y	R		Bit 1 - Over Frequency Shed (2nd Stage) – 81S-2	1 = Select bit 0 = Normal
Y	R		Bit 0 - Over Frequency Restore (2nd Stage) – 81 R-2	1 = Select bit 0 = Normal (lsb)
		41190	Change Mask Register 3	
Y	R		Bit 15 - Reclose Counter Alarm 1 Energized – 79CA1	1 = Select bit 0 = Normal (msb)
Y	R		Bit 14 - Reclose Counter Alarm 2 Energized – 79CA2	1 = Select bit 0 = Normal
N	R		Bit 13 - SEF Block Asserted – SEF	1 = Select bit 0 = Normal
N	R		Bit 12 - Breaker Fail Trip Asserted – BF TRIP	1 = Select bit 0 = Normal

N	R		Bit 11- Breaker Fail Retrip Asserted – BF RETRIP	1 = Select bit 0 = Normal
N	R		Bit 10 - Phase Overvoltage Pickup Alarm Energized – 32P	1 = Select bit 0 = Normal
N	R		Bit 9 - Neutral Overvoltage Pickup Alarm Energized – 32N	1 = Select bit 0 = Normal
N	R		Bit 8 - Breaker Fail Alarm – BFA	1 = Select bit 0 = Normal
	R		Bit 7 - Synch Check 25 -	1 = Select bit 0 = Normal
	R		Bit 6 - Ground Overvoltage 59G	1 = Select bit 0 = Normal
N	R	41190	Bit 5 – 3 PH 59 – Phase Overvoltage Element Reset	1 = Select Bit 0 = Normal
			Bit 4 – 47 – Negative Sequence Voltage Element Reset	1 = Select Bit 0 = Normal
			Bit 3 – 21P-1 – Phase Distance Unit Zone 1 Element Reset	1 = Select Bit 0 = Normal
			Bit 2 – 21P-2 – Phase Distance Unit Zone 2 Element Reset	1 = Select Bit 0 = Normal
			Bit 1- 21P-3 – Phase Distance Unit Zone 3 Element Reset	1 = Select Bit 0 = Normal
			Bit 0 – 21P-4 – Phase Distance Unit Zone 4 Element Reset.	1 = Select Bit 0 = Normal
		41191	Change Mask Word 4	
			Bit 15 – ULO 10 – User Logical Output 10	1 = Select Bit 0 = Normal
			Bit 14 – ULO 11 - User Logical Output 11	1 = Select Bit 0 = Normal
			Bit 13- ULO 12 - User Logical Output 12	1 = Select Bit 0 = Normal
			Bit 12 – ULO 13 - User Logical Output 13	1 = Select Bit 0 = Normal
			Bit 11 – ULO 14 - User Logical Output 14	1 = Select Bit 0 = Normal
			Bit 10 – ULO 15 - User Logical Output 15	1 = Select Bit 0 = Normal
			Bit 9 – ULO 16 - User Logical Output 16	1 = Select Bit 0 = Normal
			Bit 8 – 46	1 = Select Bit 0 = Normal
			Bit 7 – (Reserved)	
			Bit 6 – (Reserved)	
			Bit 5 – (Reserved)	
			Bit 4 - (Reserved)	
			Bit 3 - (Reserved)	
			Bit 2 - (Reserved)	
			Bit 1 - (Reserved)	
			Bit 0 - (Reserved)	(lsb)
Y		41192	Set/Reset Mask Register 1	
Y	R		Bit 15 - Under Voltage Trip 27	0 = Reset (msb)
Y	R		Bit 14 - Negative Sequence Overcurrent Trip – 46	0 = Reset
Y	R		Bit 13 - Phase Instantaneous Overcurrent Trip – 1 50P1	0 = Reset
Y	R		Bit 12 - Neutral Instantaneous Overcurrent Trip – 1 50N1	0 = Reset
Y	R		Bit 11 - Phase Instantaneous Overcurrent Trip – 2 50P2	0 = Reset
Y	R		Bit 10 - Neutral Instantaneous	0 = Reset

			Overcurrent Trip – 2 50N2	
Y	R		Bit 9 - Phase Instantaneous Overcurrent Trip – 3 50P3	0 = Reset
Y	R		Bit 8 - Neutral Instantaneous Overcurrent Trip – 3 50N3	0 = Reset
Y	R		Bit 7 - Phase Time Overcurrent Trip – 51P	0 = Reset
Y	R		Bit 6 - Neutral Time Overcurrent Trip – 51N	0 = Reset
Y	R		Bit 5 - Over Voltage Trip – 59	0 = Reset
Y	R		Bit 4 - Directional Overcurrent Trip (Positive Sequence) – 67P	0 = Reset
Y	R		Bit 3 - Directional Overcurrent Trip (Negative Sequence) – 67N	0 = Reset
Y	R		Bit 2 - Frequency Shed (1^{st} Stage) – 81S-1	0 = Reset
Y	R		Bit 1 - Frequency Restore (1^{st} Stage) – 81R-1	0 = Reset
Y	R		Bit 0 - Over Frequency (1^{st} Stage) – 81O-1	0 = Reset
		41193	Set/Reset Mask Register 2	
Y	R		Bit 15 - Phase Under Voltage Trip – 27-3P	0 = Reset
Y	R		Bit 14 - Single Pole Trip (Phase A) – TRIP A	0 = Reset
Y	R		Bit 13 - Single Pole Trip (Phase B) – TRIP B	0 = Reset
Y	R		Bit 12 - Single Pole Trip (Phase C) – TRIP C	0 = Reset
Y			Bit 11 - User Logical Output 1 – ULO 1	1 = Set 0 = Reset
Y			Bit 10 - User Logical Output 2 – ULO 2	1 = Set 0 = Reset
Y			Bit 9 - User Logical Output 3 – ULO 3	1 = Set 0 = Reset
Y			Bit 8 - User Logical Output 4 – ULO 4	1 = Set 0 = Reset
Y			Bit 7 - User Logical Output 5 – ULO 5	1 = Set 0 = Reset
Y			Bit 6 - User Logical Output 6 – ULO 6	1 = Set 0 = Reset
Y			Bit 5 - User Logical Output 7 – ULO 7	1 = Set 0 = Reset
Y			Bit 4 - User Logical Output 8 – ULO 8	1 = Set 0 = Reset
Y			Bit 3 - User Logical Output 9 – ULO 9	1 = Set 0 = Reset
Y	R		Bit 2 - Over Frequency (2^{nd} Stage) – 81O-2	0 = Reset
Y	R		Bit 1 - Over Frequency Shed (2^{nd} Stage) – 81S-2	0 = Reset
Y	R		Bit 0 - Over Frequency Restore (2^{nd} Stage) – 81R-2	0 = Reset
		41194	Set/Reset Mask Register 3	
Y	R		Bit 15 - Reclose Counter Alarm 1 Energized – 79CA1	0 = Reset (msb)
Y	R		Bit 14 - Reclose Counter Alarm 1 Energized – 79CA1	0 = Reset
N	R		Bit 13 - SEF Block Asserted - SEF	0 = Reset
N	R		Bit 12 - Breaker Fail Trip Asserted – BF TRIP	0 = Reset
N	R		Bit 11 - Breaker Fail Retrip Asserted – BF RETRIP	0 = Reset
N	R		Bit 10 - Phase Overvoltage Pickup Alarm Energized – 32P	0 = Reset

N	R		Bit 9 - Neutral Overvoltage Pickup Alarm Energized – 32N	0 = Reset
N	R		Bit 8 - Breaker Fail Alarm – BFA	0 = Reset
	R		Bit 7 - Synch Check 25 -	1 = Select bit 0 = Normal
	R		Bit 6 - Ground Overvoltage 59G	1 = Select bit 0 = Normal
N	R	41194	Bit 5 – 3 PH 59 – Phase Overvoltage Element Reset	0 = Reset
			Bit 4 – 47 – Negative Sequence Voltage Element Reset	0 = Reset
			Bit 3 – 21P-1 – Phase Distance Unit Zone 1 Element Reset	0 = Reset
			Bit 2 – 21P-2 – Phase Distance Unit Zone 2 Element Reset	0 = Reset
			Bit 1- 21P-3 – Phase Distance Unit Zone 3 Element Reset	0 = Reset
			Bit 0 – 21P-4 – Phase Distance Unit Zone 4 Element Reset.	0 = Reset
		41195	Change Mask Word 4	
			Bit 15 – ULO 10 – User Logical Output 10	1 = Set 0 = Reset
			Bit 14 – ULO 11 - User Logical Output 11	1 = Set 0 = Reset
			Bit 13- ULO 12 - User Logical Output 12	1 = Set 0 = Reset
			Bit 12 – ULO 13 - User Logical Output 13	1 = Set 0 = Reset
			Bit 11 – ULO 14 - User Logical Output 14	1 = Set 0 = Reset
			Bit 10 – ULO 15 - User Logical Output 15	1 = Set 0 = Reset
			Bit 9 – ULO 16 - User Logical Output 16	1 = Set 0 = Reset
			Bit 8 – 46	0 = Reset
			Bit 7 – (Reserved)	
			Bit 6 – (Reserved)	
			Bit 5 – (Reserved)	
			Bit 4 - (Reserved)	
			Bit 3 - (Reserved)	
			Bit 2 - (Reserved)	
			Bit 1 - (Reserved)	
			Bit 0 - (Reserved)	(lsb)
	NOTE : R = A reset is only possible with these designated outputs. Attempting to set these will have no effect on the state of sealed alarms.			

A simple example illustrates the methodology for resetting of the trip contact alarms within the DPU2000 and DPU1500R/DPU2000R. Figure 11-11 details the control step procedure for a unit with the default password setting.

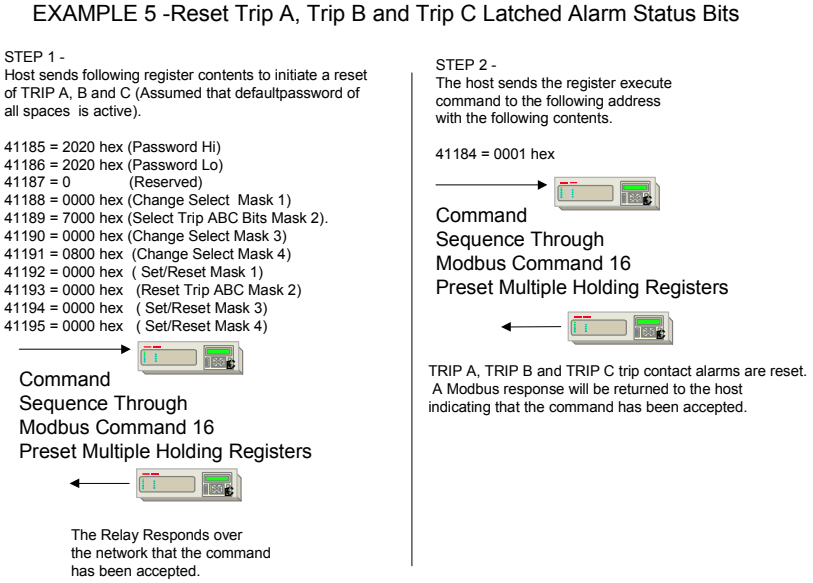


Figure 11-11. Reset Sequence for TRIP A, B, and C Latch Status Bits

Group VI Control Features Explained

Group VI is similar to the control provided in Group III. However, the control is not of the nature of a latched command control. The control type is of a momentary nature. The selected Physical Output is pulsed for a time duration set in the Breaker Failed To Trip Time Register. This register may be set to a value via ECP (External Communication Program) WinECP (Windows External Communications Program) or Register 61422 (only changeable via Modbus on the DPU1500R/DPU2000R).

As noted in Table 11-12, momentary pulse of a Physical Output is available on the DPU2000 and the DPU1500R/DPU2000R.

The Breaker Failed to Trip time register is configured a number representing the number of cycles which the breaker shall trip. The range is a number from 5 to 60. The amount of time for breaker failed to trip is, of course dependent upon whether the relay is a 50 or 60 Hz model.

Table 11-12. DPU1500R/DPU2000R Bit Control Function Definitions

DPU2000	Notes	Register	Item	Description
			GROUP VI	
Y		41196	Execute Register 0 = No Action 1 = Execute	Unsigned (16 Bits)
Y		41197	Password	ASCII – 2 Characters Leftmost Digits
Y		41198	Password	ASCII – 2 Characters Rightmost Digits
Y		41199	Spare	
Y		41200	Pulse Physical Output Change Mask	Unsigned (16 Bits)
Y			Bit 0 Trip(lsb)	1 = Pulse Output 0 = No Control
N			Bit 1 Close	1 = Pulse Output 0 = No Control
Y			Bit 2 Output 1 (Terminals 28,27)	1 = Pulse Output 0 = No Control
Y			Bit 3 Output 2 (Terminal 26,25)	1 = Pulse Output 0 = No Control
Y			Bit 4 Output 3 (Terminal 24,23)	1 = Pulse Output 0 = No Control
Y			Bit 5 Output 4 (Terminal 22,21)	1 = Pulse Output 0 = No Control
Y			Bit 6 Output 5 (Terminal 19,20)	1 = Pulse Output 0 = No Control
Y			Bit 7 Output 6 (Terminals 17,18)	1 = Pulse Output 0 = No Control
Y			Bit 8 Output 7 (DPU2000 ONLY)	1 = Pulse Output 0 = No Control

Y			Bit 9 Output 8 (DPU2000 ONLY)	1 = Pulse Output 0 = No Control
Y			Bit 10 Reserved	
Y			Bit 11 Reserved	
Y			Bit 12 Reserved	
Y			Bit 13 Reserved	
Y			Bit 14 Reserved	
Y			Bit 15 Reserved (msb)	
Y		41201	Pulse Physical Output Change Mask	Unsigned (16 Bits)
Y			Bit 0 Trip (lsb)	1 = Pulse Output 0 = No Control
N			Bit 1 Close	1 = Pulse Output 0 = No Control
Y			Bit 2 Output 1 (Terminals 28,27)	1 = Pulse Output 0 = No Control
Y			Bit 3 Output 2 (Terminal 26,25)	1 = Pulse Output 0 = No Control
Y			Bit 4 Output 3 (Terminal 24,23)	1 = Pulse Output 0 = No Control
Y			Bit 5 Output 4 (Terminal 22 21)	1 = Pulse Output 0 = No Control
Y			Bit 6 Output 5 (Terminal 19,20)	1 = Pulse Output 0 = No Control
Y			Bit 7 Output 6 (Terminals 17,18)	1 = Pulse Output 0 = No Control
Y			Bit 8 Output 7 (DPU2000 ONLY)	1 = Pulse Output 0 = No Control
Y			Bit 9 Output 8 (DPU2000 ONLY)	1 = Pulse Output 0 = No Control
Y			Bit 10 Reserved	
Y			Bit 11 Reserved	
Y			Bit 12 Reserved	
Y			Bit 13 Reserved	
Y			Bit 14 Reserved	
Y			Bit 15 Reserved (msb)	

Group VI functions operate as follows and detailed in Example 6:

Register 41200 = Pulse Physical Output Mask - Selects Control for the Function Specified.
Register 41201 = Confirm Pulse Physical Output Mask (Copy of Register 41200).

Control is processed in that Registers 41200 and 41201 are “ANDED” together. If the resultant logical operation is completed with the result being a “1” in that bit location, the control function is executed. The DPU2000 and the DPU1500R/2000R offers immediate control. No buffering of commands is attempted.

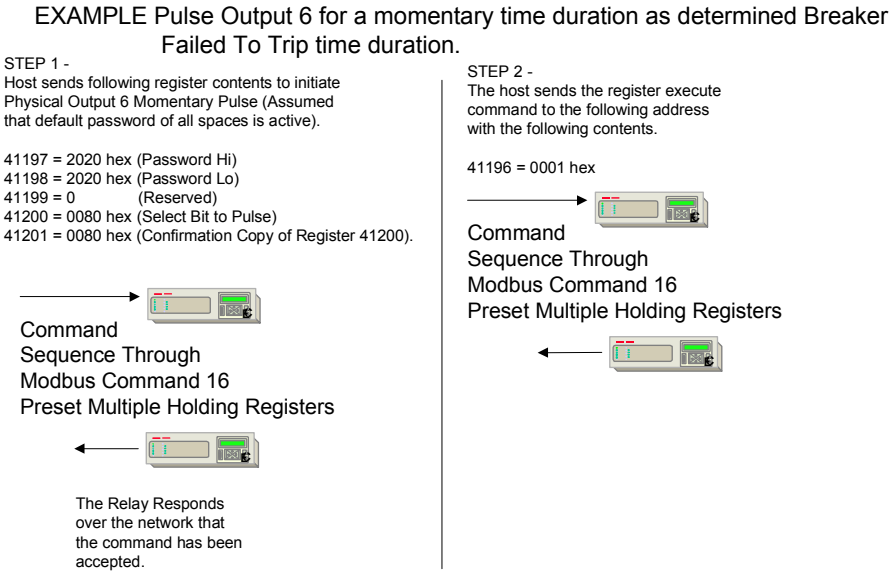


Figure 11-12. Momentary Pulse Control Illustrated

Section 12 - 6X Registers

General Relay settings are available for viewing via the DPU2000/DPU1500R/2000R front panel interface. All parameters accessible through the front panel are accessible through the Modbus 6X Registers.

A protective relay may have thousands of parameters stored in its configuration. The Modbus/Modbus Plus capable 984-680 programmable logic controllers (and earlier models) have historically only defined up to 1890 or 1920 registers for access within its products. Later definitions of the Modbus/Modbus Plus Protocol and programmable logic controllers allowed defined up to 10,000 4X Registers. Even with this improvement, this amount of registers was still too limited to store the vast amount of information available for retrieval and storage within a Modbus node (or protective relay for that matter).

Modbus protocol included a standard 6X Register type. The protocol defines this memory as extended memory. Modbus 6X memory is available in groups of 10,000 registers. Up to 10 groups may be defined within a node.

It is a standard ABB practice to store any configuration settings in 6X Register memory. The DPU2000/DPU1500R/2000R has all its parameters stored in Block 0 of the 6X memory definition (Blocks being defined from 0 through 9).

Generally, all configurable functions available through ECP or WinECP configuration package may be configured via the 6X Modbus Registers. However, ECP or WinECP configures the IED through the Standard Ten Byte protocol. ECP or WinECP configuration through the Modbus or Modbus Plus network is not possible at this time. The available configuration parameter functions via the 6X Registers are:

- Programmable Logic Input Configuration
- Programmable Logic Output Configuration
- Primary Relay Settings
- Alt 1 Relay Settings
- Alt 2 Relay Settings
- Relay Configuration Settings
- Counter Settings
- Alarm Settings
- Real Time Clock Configuration
- ULO Connection Settings and Name Assignment
- Forced Logical Input Configuration and Name Assignment
- Modbus Plus Global Data Configuration
- User Definable Register Configuration
- Password Security Mask Control Configuration
- User Display Front Panel Interface Message Transfer
- Oscillographics Control and Status

Each topic is covered in the sections following this discussion.

Function Code 20 (Read General Reference) and 21 (Write General Reference)

Modbus Protocol defines two commands 20 and 21 to read and write the registers within the 6X Register groups (or blocks). Figure 12-1 illustrates the frame sequence of function 20 and Figure 12-2 illustrates the frame sequence of Function 21.

Function 20 Read Gen.Ref.

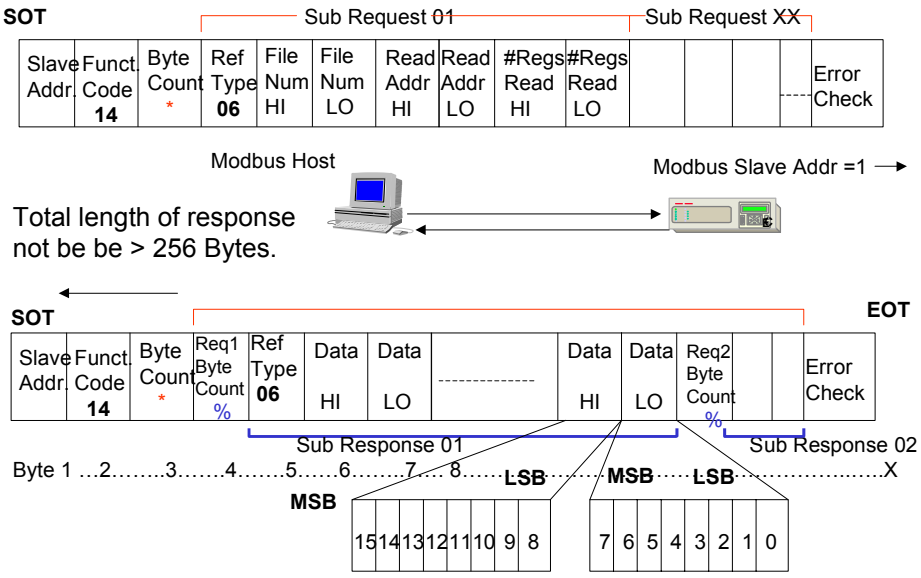


Figure 12-1. Function 20 Read 6X Register Frame Definition

Function 21 Read Gen.Ref.

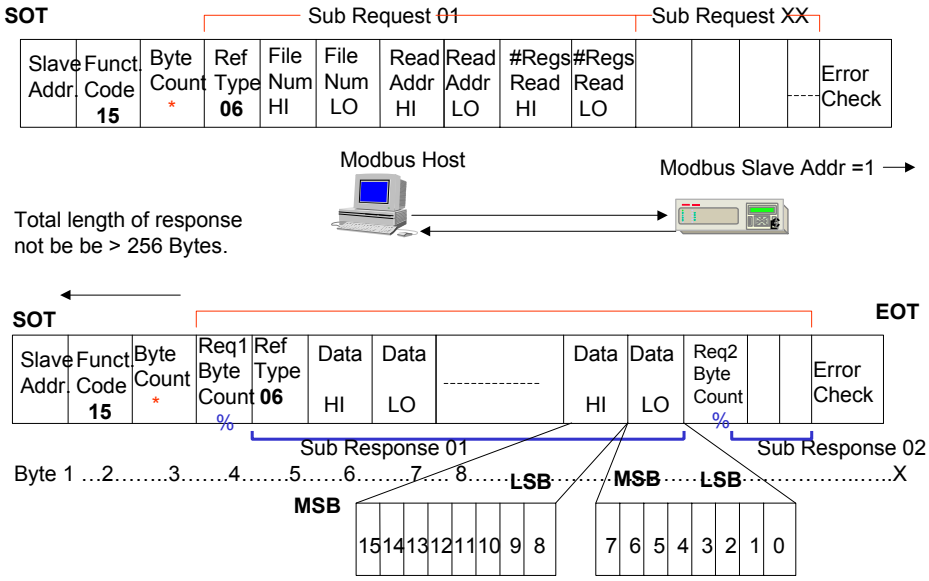


Figure 12-2. Modbus Command 21-Write General Reference Format

IMPLEMENTATION TIP - When 6X Registers are written, a 10 minute execute timer is initiated upon the first write to a 6X block. If the execute register is not written with a value of 1 within the 10 minutes of the initial write, the 6X viewable register segment will be restored to the original values from the "DPU2000/DPU1500R/DPU2000R'S" internal flash ram memory.

Programmable Input Configuration

The DPU2000/DPU1500R/DPU2000R allows for query or changing of Relay Configuration Data via the Modbus ASCII protocol. Table 12-1 further describes the register assignment for viewing or changing the DPU2000/DPU1500R/DPU2000R parameters.

Term Definitions

The parameterization may be configured via ECP or WinECP. However changing the Programmable Input Configuration is slightly more involved through Modbus Plus or Modbus. A few terms must be understood before discussing the procedure for changing the 6X memory Programmable Input parameters.

Physical Input: The opto-isolated binary input that allows external control by physically wiring the input terminals of the DPU2000R. Physical inputs are labeled (IN1, IN2, IN3, ..., 43A, 52A, 52B).

Logical Input:: An input equated by the boolean combination of the physical inputs. These inputs are used by the DPU2000R's state machine and control subroutines. Logical Inputs are labeled (PH3, GRD, TCM, ...). See later in this paragraph for additional labels.

Active Open: This defines the type of connection from the physical input or inputs and means the physical state of the opto-isolator's logic is inverted. Example: if the voltage across IN1's terminals equals zero, then the boolean equation will evaluate this term as a logical one. Likewise, when a voltage is applied to IN1, the boolean equation will evaluate this term as a logical zero.

Active Closed: This defines the type of connection from the physical input or inputs and means that the physical state of the opto-isolator's logic is the non-inverted. Example: if a voltage is applied across IN1's terminals, then the boolean equation will evaluate this term as a logical one. Likewise, when a voltage is applied to IN1, the boolean equation will evaluate this term as a logical zero.

Boolean Logic Input Equation:

Logical		ORed Physical
50-1	=	IN1 + IN2 + IN3

Logical		ANDed Physical
GRD	=	IN1 * IN2 * IN3

Input Select: The physical inputs are associated with a bit mask to determine which inputs are used when resolving the logical input's boolean equation. If the appropriate bit is set, the term will be included as part of the equation. Likewise, a cleared bit indicates that the physical input term will be ignored.

Negated AND Input: This is a bit mask that indicates if a selected input is inverted based on the active open or closed state. The bit mask uses the same associated physical inputs pattern as in the Input Select data.

AND/OR Select: The combination of the physical inputs' state used to resolve the boolean equation allows for the algebraic ANDing or ORing of all of the selected physical inputs.

User Definable Names: Physical inputs, IN1 - IN13, have memory allocated for an eight character (NULL is implied in character 9) user definable strings.

Methodology and Register Manipulation to Configure the Programmable Logical Input

Four protocol commands are required to view or change the DPU2000R's programmable input setting tables. The command order for viewing these tables can be retrieved in any sequence, but when the settings are sent to the DPU2000, the commands must be sent in the following sequence:

Receive Programmable Input Select and Index data.
Receive Programmable Negated AND Input data.
Receive Programmable Input AND/OR Select data.
Receive Programmable Input User Defined Name data.

Up to 29 logical inputs may be selected at any one time. The protocol document refers to these generic logical inputs as INPUT1 - INPUT29. The bit assignment mask for the physical inputs are as follows:

0 = IN3, 1 = IN4, 2 = IN9, 3 = IN2, 4 = IN10, 5 = 43A, 6 = 52B, 7 = 52A, 8 = IN1, 9 = IN11, 10 = IN8, 11 = IN7, 12 = IN6, 13 = IN5, 14 = IN13, 15 = IN12.

Tables 12-1 through 12-5 are used to configure the boolean algebraic equations for the desired configuration:

An example illustrating the configuration technique shall suffice:

EXAMPLE:

PH3 logical input is to be the combination of the physical inputs IN4 AND NOT IN3
ALT1 is to be selected through the logical input combination of the physical inputs IN1 OR IN3 OR NOT IN5.

The boolean logic representation of the above is derived to the following equations.
Equation 12-1 - 1 PH3 = IN4 * !IN3
Equation 12-2 2 ALT1 = IN1 + IN3 + !IN5

PH3 is desired to be mapped to physical input 3. Alternate 1 selection is desired to be mapped to physical input 8.

SOLUTION:

First, generic inputs must be selected to setup the logic equation and for this case INPUT3 is used for PH3 and INPUT8 is used for ALT1. Note, any inputs 1-29 could be valid selections. The data values required for these selections use the INDEX table defined in the protocol document.

Register	HexData	Comment
60007	0xFFFC	Selects IN3 and IN4 bits for INPUT3 Input Select low byte

Reference Figure 12-1 for the mapping of the input selection table (Bit 0 = lsb [rightmost bit] Bit 15 = msb [leftmost bit]). (Reference Table 12-1)

Input xxxxxx

60045	0x0300	Assigning PH3 offset to INPUT3 for Input Index high byte

The Physical Input 3 is to be mapped to the logical function PH3. The Logical Input function code definitions are given in Table 12-1 The codes are used to assign the logical function bytes listed in Table 12-2 Registers 60044 through 60058.

60012	0xDEFE	Selects IN1 and IN5 bits for INPUT8 Input Select high byte Selects IN3 bit for INPUT8 Input Select low byte

Reference Figure 12-1 for the mapping of the input selection table (Bit 0 = lsb [rightmost bit] Bit 15 = msb [leftmost bit]). (Reference Table 12-2)

60047	0x000C	Assigning ALT1 offset to INPUT8 for Input Index low byte

Reference Figure 12-1 for the mapping of the input selection table (Bit 0 = lsb [rightmost bit] Bit 15 = msb [leftmost bit]). (Reference Table 12-2 and 12-1).

60066	0xFFFE	This step inverts IN3's logical state for INPUT3 Negated AND Input low byte. (Reference Table 12-3 and Figure 12-1)
60071	0xDFFF	Inverts IN5's logical state for INPUT8 Negated AND Input high byte. (Reference Table 12-3 and Figure 12-1)
60128	0x0000	Boolean combination of INPUT3 selected physical logic are ANDed, all other (Reference Table 12-4)
60129	0x0004	INPUT1,2,4-29 are ORed together (Reference Table 12-4)

Table 12-1 lists the programmable Input Select and Index Bytes required for selecting the INPUT required as per Figure 12-1. (Note the table is inverted in that Bit 15 is the left most bit and bit 0 is actually the right most bit)

Bit Position:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPU2000:	IN3	IN4	IN9	IN2	IN10	43A	52B	52A	IN1	IN11	IN8	IN7	IN6	IN5	IN13	IN12
DPU2000R:	IN3	IN4	FB1	IN2	FB2	FB3	FB4	FB5	IN1	FB6	IN8	IN7	IN6	IN5	FB7	FB8
DPU1500R:	IN3	IN4	N/A	IN2	N/A	N/A	N/A	N/A	IN1	N/A	IN6	N/A	N/A	IN5	N/A	N/A

Bit Position:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	C1	C2	C3	C4	C5	C6	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Note: Bit positions 16 – 31 do not exist in the DPU2000 nor the DPU1500R.

Figure 12-1. Bit Input Mapping Definition for Registers

Table 12-1. Physical Logical Function Byte Configuration Codes for Registers 60044 to 60058

Index	Logical Input	Definition
00	52A	Breaker Position – Closed or Open per breaker
01	52B	Breaker Position – Open or Closed opposite of breaker
02	43A	Reclose Function – Enabled or Disabled
03	PH3	Phase Torque Control
04	GRD	Ground Torque Control
05	SCC	Spring Charging Contact
06	79S	Single Shot Reclosing
07	79M	Multi Shot Reclosing
08	TCM	Trip Coil Monitoring
09	50-1	Enables instantaneous over-currents: 50P-1, 50N-1
10	50-2	Enables instantaneous over-currents: 50P-2, 50N-2
11	50-3	Enables instantaneous overcurrents: 50P-3, 50N-3
12	ALT1	Enables ALT1 settings
13	ALT2	Enables ALT2 settings
14	ECI1	Event Capture Initiate - data recorded in fault record
15	ECI2	Event Capture Initiate – data recorded in fault record
16	WCI	Waveform Capture Initiate
17	ZSC	Zone Sequence Co-ordination
18	Open	Initiate a circuit breaker Trip
19	Close	Initiate a circuit breaker Close
20	46	Enables 46 protective function
21	67P	Enables 67P protective function (DPU2000/R)
22	67N	Enables 67N protective function (DPU2000/R)
23	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
24	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
25	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
26	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
27	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
28	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
29	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
30	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
31	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
32	CRI	Counter Reset Input – resets all over-current and recloser counters
33	ARCI	Timed reclose block
34	TARC	Initiate Trip and Automatic Reclose
35	SEF	Enables Sensitive Earth Fault
36	EXTBFI	External Starter Input (DPU2000/R)
37	BFI	Breaker Fail Initiate (DPU2000/R)
38	UDI	User-defined Display Input
39	25	Enables Synchronism Check function (DPU2000/R)
40	25 BYP	Synchronism Check Bypass
41	LOCAL	Local enable
42	TGT	Resets target alarms and target LEDs
43	SIA	Resets seal-in alarms
44	LIS1	Set #1 Latching Logical I/O
45	LIS2	Set #2 Latching Logical I/O
46	LIS3	Set #3 Latching Logical I/O
47	LIS4	Set #4 Latching Logical I/O
48	LIS5	Set #5 Latching Logical I/O
49	LIS6	Set #6 Latching Logical I/O
50	LIS7	Set #7 Latching Logical I/O
51	LIS8	Set #8 Latching Logical I/O
52	LIR1	Reset #1 Latching Logical I/O
53	LIR2	Reset #2 Latching Logical I/O

Index	Logical Input	Definition
54	LIR3	Reset #3 Latching Logical I/O
55	LIR4	Reset #4 Latching Logical I/O
56	LIR5	Reset #5 Latching Logical I/O
57	LIR6	Reset #6 Latching Logical I/O
58	LIR7	Reset #7 Latching Logical I/O
59	LIR8	Reset #8 Latching Logical I/O
60	TIS	Set Hot-Line-Tag function
61	TIR	Reset Hot-Line-Tag function
62	ULI10	User Logical Input 10
63	ULI11	User Logical Input 11
64	ULI12	User Logical Input 12
65	ULI13	User Logical Input 13
66	ULI14	User Logical Input 14
67	ULI15	User Logical Input 15
68	ULI16	User Logical Input 16
69	46A TC	46A Torque Control

Table 12-2. Relay Configuration Setting Definition

Register Address	Item	Description
60000	SPARE_1	
60001	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits Range 0-2
60002	Access Password	ASCII – 2 Characters Leftmost Digits
60003	Access Password	ASCII – 2 Characters Rightmost Digits
60004	SPARE_2	
60005	Input 1 Select Mask	Unsigned Integer 16 Bits
60006	Input 2 Select Mask	Unsigned Integer 16 Bits
60007	Input 3 Select Mask	Unsigned Integer 16 Bits
60008	Input 4 Select Mask	Unsigned Integer 16 Bits
60009	Input 5 Select Mask	Unsigned Integer 16 Bits
60010	Input 6 Select Mask	Unsigned Integer 16 Bits
60011	Input 7 Select Mask	Unsigned Integer 16 Bits
60012	Input 8 Select Mask	Unsigned Integer 16 Bits
60013	Input 9 Select Mask	Unsigned Integer 16 Bits
60014	Input 10 Select Mask	Unsigned Integer 16 Bits
60015	Input 11 Select Mask	Unsigned Integer 16 Bits
60016	Input 12 Select Mask	Unsigned Integer 16 Bits
60017	Input 13 Select Mask	Unsigned Integer 16 Bits
60018	Input 14 Select Mask	Unsigned Integer 16 Bits
60019	Input 15 Select Mask	Unsigned Integer 16 Bits
60020	Input 16 Select Mask	Unsigned Integer 16 Bits
60021	Input 17 Select Mask	Unsigned Integer 16 Bits
60022	Input 18 Select Mask	Unsigned Integer 16 Bits
60023	Input 19 Select Mask	Unsigned Integer 16 Bits
60024	Input 20 Select Mask	Unsigned Integer 16 Bits
60025	Input 21 Select Mask	Unsigned Integer 16 Bits
60026	Input 22 Select Mask	Unsigned Integer 16 Bits
60027	Input 23 Select Mask	Unsigned Integer 16 Bits
60028	Input 24 Select Mask	Unsigned Integer 16 Bits
60029	Input 25 Select Mask	Unsigned Integer 16 Bits
60030	Input 26 Select Mask	Unsigned Integer 16 Bits

60031	Input 27 Select Mask	Unsigned Integer 16 Bits
60032	Input 28 Select Mask	Unsigned Integer 16 Bits
60033	Input 29 Select Mask	Unsigned Integer 16 Bits
60034	Reserved (Writable)	Unsigned Integer 16 Bits
60035	Reserved (Writable)	Unsigned Integer 16 Bits
60036	Reserved (Writable)	Unsigned Integer 16 Bits
60037	Reserved (Writable)	Unsigned Integer 16 Bits
60038	Reserved (Writable)	Unsigned Integer 16 Bits
60039	Reserved (Writable)	Unsigned Integer 16 Bits
60040	Reserved (Writable)	Unsigned Integer 16 Bits
60041	Reserved (Writable)	Unsigned Integer 16 Bits
60042	Reserved (Writable)	Unsigned Integer 16 Bits
60043	Reserved (Writable)	Unsigned Integer 16 Bits
60044	Input 1 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 2 Index Byte	Unsigned Integer Lo byte 8 right most bits
60045	Input 3 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 4 Index Byte	Unsigned Integer Lo byte 8 right most bits
60046	Input 5 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 6 Index Byte	Unsigned Integer Lo byte 8 right most bits
60047	Input 7 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 8 Index Byte	Unsigned Integer Lo byte 8 right most bits
60048	Input 9 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 10 Index Byte	Unsigned Integer Lo byte 8 right most bits
60049	Input 11 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 12 Index Byte	Unsigned Integer Lo byte 8 right most bits
60050	Input 13 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 14 Index Byte	Unsigned Integer Lo byte 8 right most bits
60051	Input 15 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 16 Index Byte	Unsigned Integer Lo byte 8 right most bits
60052	Input 17 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 18 Index Byte	Unsigned Integer Lo byte 8 right most bits
60053	Input 19 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 20 Index Byte	Unsigned Integer Lo byte 8 right most bits
60054	Input 21 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 22 Index Byte	Unsigned Integer Lo byte 8 right most bits
60055	Input 23 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 24 Index Byte	Unsigned Integer Lo byte 8 right most bits
60056	Input 25 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 26 Index Byte	Unsigned Integer Lo byte 8 right most bits
60057	Input 27 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Input 28 Index Byte	Unsigned Integer Lo byte 8 right most bits
60058	Input 29 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Spare	

The inputs may be logically ANDed or logically NEGATED. The selection of these functions are configured through Registers 60064 to 60092. The configuration word designation is shown in Figure 12-1.

Table 12-3. Programmable Input "NEGATED" "AND" Input

Address	Item	Description
60064	Input 1 AND/NEGATE Mask	Unsigned Integer 16 Bits
60065	Input 2 AND/NEGATE Mask	Unsigned Integer 16 Bits
60066	Input 3 AND/NEGATE Mask	Unsigned Integer 16 Bits
60067	Input 4 AND/NEGATE Mask	Unsigned Integer 16 Bits
60068	Input 5 AND/NEGATE Mask	Unsigned Integer 16 Bits

60069	Input 6 AND/NEGATE Mask	Unsigned Integer 16 Bits
60070	Input 7AND/NEGATE Mask	Unsigned Integer 16 Bits
60071	Input 8 AND/NEGATE Mask	Unsigned Integer 16 Bits
60072	Input 9 AND/NEGATE Mask	Unsigned Integer 16 Bits
60073	Input 10 AND/NEGATE Mask	Unsigned Integer 16 Bits
60074	Input 11 AND/NEGATE Mask	Unsigned Integer 16 Bits
60075	Input 12 AND/NEGATE Mask	Unsigned Integer 16 Bits
60076	Input 13 AND/NEGATE Mask	Unsigned Integer 16 Bits
60077	Input 14 AND/NEGATE Mask	Unsigned Integer 16 Bits
60078	Input 15 AND/NEGATE Mask	Unsigned Integer 16 Bits
60079	Input 16 AND/NEGATE Mask	Unsigned Integer 16 Bits
60080	Input 17 AND/NEGATE Mask	Unsigned Integer 16 Bits
60081	Input 18 AND/NEGATE Mask	Unsigned Integer 16 Bits
60082	Input 19 AND/NEGATE Mask	Unsigned Integer 16 Bits
60083	Input 20 AND/NEGATE Mask	Unsigned Integer 16 Bits
60084	Input 21 AND/NEGATE Mask	Unsigned Integer 16 Bits
60085	Input 22 AND/NEGATE Mask	Unsigned Integer 16 Bits
60086	Input 23 AND/NEGATE Mask	Unsigned Integer 16 Bits
60087	Input 24 AND/NEGATE Mask	Unsigned Integer 16 Bits
60088	Input 25 AND/NEGATE Mask	Unsigned Integer 16 Bits
60089	Input 26 AND/NEGATE Mask	Unsigned Integer 16 Bits
60090	Input 27 AND/NEGATE Mask	Unsigned Integer 16 Bits
60091	Input 28 AND/NEGATE Mask	Unsigned Integer 16 Bits
60092	Input 29 AND/NEGATE Mask	Unsigned Integer 16 Bits

If the combination logic is to be logically ANDed or ORed, then the following two registers must be configured indicating the resultant logic combination.

Table 12-4. AND/OR Conditional Logic Table

Address	Item	Description
60128	Programmable Input AND/OR Select	Unsigned Integer 16 Bits
	Bit 0 = Input 17 AND/OR (lsb rightmost)	0 = Bits ANDed 1 = Bits ORed
	Bit 1 = Input 18 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 2 = Input 19 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 3 = Input 20 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 4 = Input 21 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 5 = Input 22 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 6 = Input 23 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 7 = Input 24 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 8 = Input 25 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 9 = Input 26 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 10 = Input 27 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 11 = Input 28 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 12 = Input 29 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 13 = Reserved AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 14 = Reserved AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 15 = Reserved AND/OR (msb leftmost)	0 = Bits ANDed 1 = Bits ORed
60129	Programmable Input AND/OR Select	Unsigned Integer 16 Bits
	Bit 0 = Input 1 AND/OR (lsb rightmost)	0 = Bits ANDed 1 = Bits ORed
	Bit 1 = Input 2 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 2 = Input 3 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 3 = Input 4 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 4 = Input 5 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 5 = Input 6 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 6 = Input 7 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 7 = Input 8 AND/OR	0 = Bits ANDed 1 = Bits ORed

	Bit 8 = Input 9 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 9 = Input 10 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 10 = Input 11 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 11 = Input 12 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 12 = Input 13 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 13 = Input 14 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 14 = Input 15 AND/OR	0 = Bits ANDed 1 = Bits ORed
	Bit 15 = Input 16 AND/OR (msb leftmost)	0 = Bits ANDed 1 = Bits ORed

Each programmable INPUT may be assigned a label of up to 8 characters Table 12-5 lists the register definition table which may be configured for each of the each characters. Please reference Appendix B for the ASCII conversion chart to aid in the configuration of these registers.

Table 12-5. Physical Input Mapping Table

Address	Item	Description
60256	Input 1 Rightmost 2 Characters	2 Digit ASCII Characters
60257	Input 1 Characters	2 Digit ASCII Characters
60258	Input 1 Characters	2 Digit ASCII Characters
60259	Input 1 Leftmost 2 Characters	2 Digit ASCII Characters
60260	Input 2 Rightmost 2 Characters	2 Digit ASCII Characters
60261	Input 2 Characters	2 Digit ASCII Characters
60262	Input 2 Characters	2 Digit ASCII Characters
60263	Input 2 Leftmost 2 Characters	2 Digit ASCII Characters
60264	Input 3 Rightmost 2 Characters	2 Digit ASCII Characters
60265	Input 3 Characters	2 Digit ASCII Characters
60266	Input 3 Characters	2 Digit ASCII Characters
60267	Input 3 Leftmost 2 Characters	2 Digit ASCII Characters
60268	Input 4 Rightmost 2 Characters	2 Digit ASCII Characters
60269	Input 4 Characters	2 Digit ASCII Characters
60270	Input 4 Characters	2 Digit ASCII Characters
60271	Input 4 Leftmost 2 Characters	2 Digit ASCII Characters
60272	Input 5 Rightmost 2 Characters	2 Digit ASCII Characters
60273	Input 5 Characters	2 Digit ASCII Characters
60274	Input 5 Characters	2 Digit ASCII Characters
60275	Input 5 Leftmost 2 Characters	2 Digit ASCII Characters
60276	Input 6 Rightmost 2 Characters	2 Digit ASCII Characters
60277	Input 6 Characters	2 Digit ASCII Characters
60278	Input 6 Characters	2 Digit ASCII Characters
60279	Input 6 Leftmost 2 Characters	2 Digit ASCII Characters
60280	Input 7 Rightmost 2 Characters	2 Digit ASCII Characters
60281	Input 7 Characters	2 Digit ASCII Characters
60282	Input 7 Characters	2 Digit ASCII Characters
60283	Input 7 Leftmost 2 Characters	2 Digit ASCII Characters
60284	Input 8 Rightmost 2 Characters	2 Digit ASCII Characters
60285	Input 8 Characters	2 Digit ASCII Characters
60286	Input 8 Characters	2 Digit ASCII Characters
60287	Input 8 Leftmost 2 Characters	2 Digit ASCII Characters
60288	Input 9 Rightmost 2 Characters	2 Digit ASCII Characters
60289	Input 9 Characters	2 Digit ASCII Characters
60290	Input 9 Characters	2 Digit ASCII Characters
60291	Input 9 Leftmost 2 Characters	2 Digit ASCII Characters
60292	Input 10 Rightmost 2 Characters	2 Digit ASCII Characters
60293	Input 10 Characters	2 Digit ASCII Characters
60294	Input 10 Characters	2 Digit ASCII Characters
60295	Input 10 Leftmost 2 Characters	2 Digit ASCII Characters

Address	Item	Description
60296	Input 11 Rightmost 2 Characters	2 Digit ASCII Characters
60297	Input 11 Characters	2 Digit ASCII Characters
60298	Input 11 Characters	2 Digit ASCII Characters
60299	Input 11 Leftmost 2 Characters	2 Digit ASCII Characters
60300	Input 12 Rightmost 2 Characters	2 Digit ASCII Characters
60301	Input 12 Characters	2 Digit ASCII Characters
60302	Input 12 Characters	2 Digit ASCII Characters
60303	Input 12 Leftmost 2 Characters	2 Digit ASCII Characters
60304	Input 13 Rightmost 2 Characters	2 Digit ASCII Characters
60305	Input 13 Characters	2 Digit ASCII Characters
60306	Input 13 Characters	2 Digit ASCII Characters
60307	Input 13 Leftmost 2 Characters	2 Digit ASCII Characters
60308	C1 Rightmost 2 Characters	2 Digit ASCII Characters
60309	C1 Characters	2 Digit ASCII Characters
60310	C1 Characters	2 Digit ASCII Characters
60311	C1 Leftmost 2 Characters	2 Digit ASCII Characters
60312	C2 Rightmost 2 Characters	2 Digit ASCII Characters
60313	C2 Characters	2 Digit ASCII Characters
60314	C2 Characters	2 Digit ASCII Characters
60315	C2 Leftmost 2 Characters	2 Digit ASCII Characters
60316	C3 Rightmost 2 Characters	2 Digit ASCII Characters
60317	C3 Characters	2 Digit ASCII Characters
60318	C3 Characters	2 Digit ASCII Characters
60319	C3 Leftmost 2 Characters	2 Digit ASCII Characters
60320	C4 Rightmost 2 Characters	2 Digit ASCII Characters
60321	C4 Characters	2 Digit ASCII Characters
60322	C4 Characters	2 Digit ASCII Characters
60323	C4 Leftmost 2 Characters	2 Digit ASCII Characters
60324	C5 Rightmost 2 Characters	2 Digit ASCII Characters
60325	C5 Characters	2 Digit ASCII Characters
60326	C5 Characters	2 Digit ASCII Characters
60327	C5 Leftmost 2 Characters	2 Digit ASCII Characters
60328	C6 Rightmost 2 Characters	2 Digit ASCII Characters
60329	C6 Characters	2 Digit ASCII Characters
60330	C6 Characters	2 Digit ASCII Characters
60331	C6 Leftmost 2 Characters	2 Digit ASCII Characters

NOTE : “C” Control Keys are only available in the Front Panel Interface Enhanced Display DPU 2000R Units.

Programmable Input Select for OCI Control Buttons

The select mask is used in the previous tables . Bit Positions 16-31 are defined by the select mask in this group of registers.

TABLE 12- 5a – Programmable Input Select for OCI Control Buttons

Address	Item	Description
60384	Input 1 SELECT Mask	Unsigned Integer 16 Bits
60385	Input 2 SELECT Mask	Unsigned Integer 16 Bits
60386	Input 3 SELECT Mask	Unsigned Integer 16 Bits
60387	Input 4 SELECT Mask	Unsigned Integer 16 Bits
60388	Input 5 SELECT Mask	Unsigned Integer 16 Bits
60389	Input 6 SELECT Mask	Unsigned Integer 16 Bits
60390	Input 7SELECT Mask	Unsigned Integer 16 Bits
60391	Input 8 SELECT Mask	Unsigned Integer 16 Bits

60392	Input 9 SELECT Mask	Unsigned Integer 16 Bits
60393	Input 10 SELECT Mask	Unsigned Integer 16 Bits
60394	Input 11 SELECT Mask	Unsigned Integer 16 Bits
60395	Input 12 SELECT Mask	Unsigned Integer 16 Bits
60396	Input 13 SELECT Mask	Unsigned Integer 16 Bits
60397	Input 14 SELECT Mask	Unsigned Integer 16 Bits
60398	Input 15 SELECT Mask	Unsigned Integer 16 Bits
60399	Input 16 SELECT Mask	Unsigned Integer 16 Bits
60400	Input 17 SELECT Mask	Unsigned Integer 16 Bits
60401	Input 18 SELECT Mask	Unsigned Integer 16 Bits
60402	Input 19 SELECT Mask	Unsigned Integer 16 Bits
60403	Input 20 SELECT Mask	Unsigned Integer 16 Bits
60404	Input 21 SELECT Mask	Unsigned Integer 16 Bits
60405	Input 22 SELECT Mask	Unsigned Integer 16 Bits
60406	Input 23 SELECT Mask	Unsigned Integer 16 Bits
60407	Input 24 SELECT Mask	Unsigned Integer 16 Bits
60408	Input 25 SELECT Mask	Unsigned Integer 16 Bits
60409	Input 26 SELECT Mask	Unsigned Integer 16 Bits
60410	Input 27 SELECT Mask	Unsigned Integer 16 Bits
60411	Input 28 SELECT Mask	Unsigned Integer 16 Bits
60412	Input 29 SELECT Mask	Unsigned Integer 16 Bits

Not available for the DPU 1500 or DPU 2000 Models

Programmable Extended Input Negated AND Input

Negated Programmable input data is transferred to the PC as such:

When Bit = 0 then Input is open.
When Bit = 1 then Input is closed.

The mask designation is found in Table 12-5b.
TABLE 12-5b: Programmable Extended Input Negated AND Input Select for OCI control Buttons

Address	Item	Description
60413	Input 1 Not SELECT Mask	Unsigned Integer 16 Bits
60414	Input 2 Not SELECT Mask	Unsigned Integer 16 Bits
60415	Input 3 Not SELECT Mask	Unsigned Integer 16 Bits
60416	Input 4 Not SELECT Mask	Unsigned Integer 16 Bits
60417	Input 5 Not SELECT Mask	Unsigned Integer 16 Bits
60418	Input 6 Not SELECT Mask	Unsigned Integer 16 Bits
60419	Input 7 Not SELECT Mask	Unsigned Integer 16 Bits
60420	Input 8 Not SELECT Mask	Unsigned Integer 16 Bits
60421	Input 9 Not SELECT Mask	Unsigned Integer 16 Bits
60422	Input 10 Not SELECT Mask	Unsigned Integer 16 Bits
60423	Input 11 Not SELECT Mask	Unsigned Integer 16 Bits
60424	Input 12 Not SELECT Mask	Unsigned Integer 16 Bits
60425	Input 13 Not SELECT Mask	Unsigned Integer 16 Bits
60426	Input 14 Not SELECT Mask	Unsigned Integer 16 Bits
60427	Input 15 Not SELECT Mask	Unsigned Integer 16 Bits
60428	Input 16 Not SELECT Mask	Unsigned Integer 16 Bits
60429	Input 17 Not SELECT Mask	Unsigned Integer 16 Bits
60430	Input 18 Not SELECT Mask	Unsigned Integer 16 Bits
60431	Input 19 Not SELECT Mask	Unsigned Integer 16 Bits
60432	Input 20 Not SELECT Mask	Unsigned Integer 16 Bits
60433	Input 21 Not SELECT Mask	Unsigned Integer 16 Bits

60434	Input 22 Not SELECT Mask	Unsigned Integer 16 Bits
60435	Input 23 Not SELECT Mask	Unsigned Integer 16 Bits
60436	Input 24 Not SELECT Mask	Unsigned Integer 16 Bits
60437	Input 25 Not SELECT Mask	Unsigned Integer 16 Bits
60438	Input 26 Not SELECT Mask	Unsigned Integer 16 Bits
60439	Input 27 Not SELECT Mask	Unsigned Integer 16 Bits
60440	Input 28 Not SELECT Mask	Unsigned Integer 16 Bits
60441	Input 29 Not SELECT Mask	Unsigned Integer 16 Bits

Programmable Output Select Configuration

The configuration of the DPU1500R/2000R Output contacts follow the same philosophy as is the case with the programmable user inputs. Figure 12-3 lists the mask bit designation for each of the bits for the mask.

If bit = 0, the selected logical outputs are ORed together to drive the assigned output.
If bit = 1, the selected logical outputs are ANDed together to drive the assigned output.

Bit Position:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
DPU2000:	Trip	Close	Out6	Out4	Out5	Out3	Out2	Out1	Out7	Out8	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	FB1	FB2	FB3	FB4	FB5	FB6	FB7	FB8
DPU1500R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit Position:	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit Position:	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	T17	T18	T19	T20	T21	T22	T23	T24	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Figure 12-3. Bit Output Mapping Definition for Registers

Table 12-6. Relay Configuration Setting Definition

Register Address	Item	Description
60512	SPARE_1	
60513	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits Range 0-2
60514	Access Password	ASCII – 2 Characters Leftmost Digits
60515	Access Password	ASCII – 2 Characters Rightmost Digits
60516	SPARE_2	
60517	Output 1 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60518	Output 1 Select Mask	Unsigned Integer 16 Bits

		Lo Bit Mask
60519	Output 2 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60520	Output 2 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60521	Output 3 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60522	Output 3 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60523	Output 4 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60524	Output 4 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60525	Output 5 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60526	Output 5 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60527	Output 6 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60528	Output 6 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60529	Output 7 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60530	Output 7 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60531	Output 8 Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60532	Output 8 Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60533	Feedback 3 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60534	Feedback 3 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60535	Feedback 4 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60536	Feedback 4 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60537	Feedback 5 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60538	Feedback 5 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60539	Feedback 6 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60540	Feedback 6 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60541	Feedback 7 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60542	Feedback 7 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask
60543	Feedback 8 Output Select Mask	Unsigned Integer 16 Bits Hi Bit Mask
60544	Feedback 8 Output Select Mask	Unsigned Integer 16 Bits Lo Bit Mask

Table 12-6 lists the programmable Output Select and Index Bytes required for selecting the Output required as per Figure 12-5 (Note the table is inverted in that Bit 15 is the left most bit and bit 0 is actually the right most bit)

If bit = 0, the logical output is selected. If the bit = 1, the logical output is not selected.

Bit Position	Definition
0	TRIP (Fixed, not programmable)
1	CLOSE (Fixed in DPU2000, mapping NOT permitted by DPU2000R or DPU1500R)
2	OUTPUT1
3	OUTPUT2
4	OUTPUT3
5	OUTPUT4
6	OUTPUT5
7	OUTPUT6
8	OUTPUT7
9	OUTPUT8
10	OUTPUT9
11	OUTPUT10
12	OUTPUT11
13	OUTPUT12
14	OUTPUT13
15	OUTPUT14
16	OUTPUT15
17	OUTPUT16
18	OUTPUT17
19	OUTPUT18
20	OUTPUT19
21	OUTPUT20
22	OUTPUT21
23	OUTPUT22
24	OUTPUT23
25	OUTPUT24
26	OUTPUT25
27	OUTPUT26
28	OUTPUT27
29	OUTPUT28
30	OUTPUT29
31	OUTPUT30

Figure 12-4. Bit Output Mapping Definition for Registers

Table 12-7. Physical Logical Function Byte Configuration Codes for Registers 60044 to 60058

Index	Output	Definitions
00	TRIP	Fixed Trip
01	CLOSE	Fixed Close
02	ALARM	Self Check Alarm
03	27-1P	Single Phase Under Voltage
04	46	Negative Sequence Overcurrent
05	50P-1	Phase Inst. Overcurrent
06	50N-1	Neutral Inst. Overcurrent
07	50P-2	Phase Inst. Overcurrent
08	50N-2	Neutral Inst. Overcurrent
09	50P-3	Phase Inst. Overcurrent
10	50N-3	Neutral Inst. Overcurrent
11	51P	Phase Time Overcurrent
12	51N	Neutral Time Overcurrent
13	59	Over Voltage
14	67P	Directional Overcurrent (pos seq)
15	67N	Directional Overcurrent (neg seq)
16	81S-1	Frequency Shed (First stage)
17	81R-1	Frequency Restore (First stage)
18	PATA	Phase A Target
19	PBTA	Phase B Target
20	PCTA	Phase C Target
21	TCFA	Trip Circuit Fail
22	TCC	Tap Changer Cutout
23	79DA	Recloser Disable
24	PUA	Pickup
25	79LOA	Recloser Lockout
26	BFA	Breaker Fail
27	PDA	Phase Peak Demand
28	NDA	Neutral Peak Demand
29	BFUA	Blown Fuse
30	KSI	KiloAmp Summation
31	79CA-1	Reclose Counter1
32	HPFA	High Power Factor
33	LPFA	Low Power Factor
34	OCTC	Overcurrent Trip Counter
35	50-1D	50-1 Element Disable
36	50-2D	50-2 Element Disable
37	STCA	Setting Table Change
38	ZSC	Zone Sequence
39	PH3-D	Phase Torque Control Disable
40	GRD-D	Neutral Torque Control Disable
41	32PA	Directional Pickup (pos seq)
42	32NA	Directional Pickup (neg seq)
43	27-3P	3 Phase Under Voltage
44	VarDA	Var Demand
45	79CA-2	Reclose Counter2
46	TRIPA	Single Pole Trip Phase A
47	TRIPB	Single Pole Trip Phase B
48	TRIPC	Single Pole Trip Phase C
49	27-1P*	Single Phase Under Voltage
50	46*	Negative Sequence Overcurrent
51	50P-1*	Phase Inst. Overcurrent
52	50N-1*	Neutral Inst. Overcurrent
53	50P-2*	Phase Inst. Overcurrent
54	50N-2*	Neutral Inst. Overcurrent
55	50P-3*	Phase Inst. Overcurrent
56	50N-3*	Neutral Inst. Overcurrent
57	51P*	Phase Time Overcurrent
58	51N*	Neutral Time Overcurrent
59	59*	Over Voltage
60	67P*	Directional Overcurrent (pos seq)
61	67N*	Directional Overcurrent (neg seq)
62	81S-1*	Frequency Shed (First stage)
63	81R-1*	Frequency Restore (First stage)
64	81O-1*	Over Frequency (First stage)

Index	Output	Definitions
65	27-3P*	3 Phase Under Voltage
66	TRIPA*	Single Pole Trip Phase A
67	TRIPB*	Single Pole Trip Phase B
68	TRIPC*	Single Pole Trip Phase C
69	ULO1	User Logical Output 1
70	ULO2	User Logical Output 2
71	ULO3	User Logical Output 3
72	ULO4	User Logical Output 4
73	ULO5	User Logical Output 5
74	ULO6	User Logical Output 6
75	ULO7	User Logical Output 7
76	ULO8	User Logical Output 8
77	ULO9	User Logical Output 9
78	PVArA	Positive Var
79	NVArA	Negative Var
80	LOADA	Load Current
81	81O-1	Over Frequency (First Stage)
82	81O-2	Over Frequency (2nd Stage)
83	81S-2	Frequency Shed (2nd Stage)
84	81R-2	Frequency Restore (2nd Stage)
85	81O-2*	Over Frequency (2nd Stage)
86	81S-2*	Frequency Shed (2nd Stage)
87	81R-2*	Frequency Restore (2nd Stage)
88	CLTA	Cold Load Timer
89	Pwatt1	Positive Watt Alarm 1
90	Pwatt2	Positive Watt Alarm 2
91	79CA1*	Recloser Counter 1 Alarm
92	79CA2*	Recloser Counter 2 Alarm
93	SEF*	Sensitive Earth Fault Trip
94	SEF	Sensitive Earth Fault Trip
95	BZA	Bus Zone Alarm
96	BF Trip	Breaker Fail Trip
97	BF Retrip	Breaker Fail Re-Trip
98	BF Trip*	Breaker Fail Trip
99	BF Retrip*	Breaker Fail Re-Trip
100	32P	Phase Directionality Alarm
101	32N	Neutral Directionality Alarm
102	32P*	Phase Directionality Alarm
103	32N*	Neutral Directionality Alarm
104	BFA*	Breaker Failure Alarm
105	25*	In Synchronism
106	25	In Synchronism
107	SBA	Slow Breaker Alarm
108	79V	Recloser
109	Rclin	Recloer init
110	59G	V0 Over Voltage
111	59G*	V0 Over Voltage seal-in
112	LO1	Latching output1
113	LO2	Latching output2
114	LO3	Latching output3
115	LO4	Latching output4
116	LO5	Latching output5
117	LO6	Latching output6
118	LO7	Latching output7
119	LO8	Latching output8
120	TR_ON	Hot Hole Tagging On
121	TR_OFF	Hot Hole Tagging Off
122	TR_TAG	Hot Hole Tagging Tagged
123	59-3P	3 Phase Over Voltage
124	59-3P*	3 Phase Over Voltage Seal-in
125	47	Neg Seq Over Voltage
126	47*	Net Seq Over Voltage Seal-in
127	50-3D	50-3 Element Disable
128	21P-1	Fwd Reach Zone 1 Distance Alarm
129	21P-1*	Fwd Reach Zone 1 Distance Seal-in Alarm

Index	Output	Definitions
130	21P-2	Fwd Reach Zone 2 Distance Alarm
131	21P-2*	Fwd Reach Zone 2 Distance Seal-in Alarm
132	21P-3	Fwd Reach Zone 3 Distance Alarm
133	21P-3*	Fwd Reach Zone 3 Distance Seal-in Alarm
134	21P-4	Fwd Reach Zone 4 Distance Alarm
135	21P-4*	Fwd Reach Zone 4 Distance Seal-in Alarm
136	C1	Control Button 1
137	C2	Control Button 2
138	C3	Control Button 3
139	C4	Control Button 4
140	C5	Control Button 5
141	C6	Control Button 6
142	TripT	Trip Target
143	NTA	Neutral Target
144	TimeT	Time Target
145	InstT	Inst Target
146	NeqSeqT	Negative Seq Target
147	FreqT	Frequency Target
148	DirT	Direction Target
149	VoltT	Volt Target
150	DistT	Distance Target
151	SEFT	Sensitve Earth Fault Target
152	ULO10	User Logical Output 10
153	ULO11	User Logical Output 11
154	ULO12	User Logical Output 12
155	ULO13	User Logical Output 13
156	ULO14	User Logical Output 14
157	ULO15	User Logical Output 15
158	ULO16	User Logical Output 16
159	LBLL	Live Bus Live Line for 25 function
160	LBDL	Live Bus Dead Line for 25 function
161	DBLL	Dead Bus Live Line for 25 function
162	DBDL	Dead Bus Dead Line for 25 function
163	46A	46A
164	46A*	46A Seal In
165	REMOTE – D	Control through Communications Disabled.
166	PRI-ON	Primary Settings Active
167	ALT1-ON	ALT1 Settings Active
168	ALT2-ON	ALT2 Settings Active
169	SHIFTA-1	Barrel Shift-A Output No. 1
170	SHIFTA-2	Barrel Shift-A Output No. 2
171	SHIFTA-3	Barrel Shift-A Output No. 3
172	SHIFTA-4	Barrel Shift-A Output No. 4
173	SHIFTB-1	Barrel Shift-B Output No. 1
174	SHIFTB-2	Barrel Shift-B Output No. 2
175	SHIFTB-3	Barrel Shift-B Output No. 3
176	SHIFTB-4	Barrel Shift-B Output No. 4

The Outputs may be ANDed/Ored with a selection function placed in the index byte. The bits to be anded/ored are designated by the following axiom. If the selected bit in the pattern designated in Figure 12-4 is a 0, then the bit is OR'ed. If the selected bit is a 1 then the bits are AND'ed together. NOTE * indicated Latched Element Bit Status.

Table 12-8. Programmable Output AND/OR Select

Address	Item	Description
60576	Reserved	Unsigned Integer 16 Bits
60577	AND/OR Selection Bits	Unsigned Integer 16 Bits (See Figure 12-4 for Designation)
60578	Output 1 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 2 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60579	Output 3 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 4 Index Byte	Unsigned Integer Lo byte 8 rightmost bits

Address	Item	Description
60580	Output 5 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 6 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60581	Output 7 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 8 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60582	Output 9 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 10 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60583	Output 11 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 12 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60584	Output 13 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 14 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60585	Output 15 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 16 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60586	Output 17 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 18 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60587	Output 19 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 20 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60588	Output 21 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 22 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60589	Output 23 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 24 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60590	Output 25 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 26 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60591	Output 27 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 28 Index Byte	Unsigned Integer Lo byte 8 rightmost bits
60592	Output 29 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	Output 30 Index Byte	Unsigned Integer Lo byte 8 rightmost bits

Programmable Output User Defined String Block

Each one of the Output contacts may be assigned an eight character name. The registers for configuration of the text name are Registers 60640 through 60695. The name is programmed similarly to the Input name designation. Table 12-9 lists the address assignment for the Programmable Output User Defined Strings

Table 12-9. ASCII Descriptor Matrix

Address	Item	Description
60640	Output 1 Rightmost 2 Characters	2 Digit ASCII Characters
60641	Output 1 Characters	2 Digit ASCII Characters
60642	Output 1 Characters	2 Digit ASCII Characters
60643	Output 1 Leftmost 2 Characters	2 Digit ASCII Characters
60644	Output 2 Rightmost 2 Characters	2 Digit ASCII Characters
60645	Output 2 Characters	2 Digit ASCII Characters
60646	Output 2 Characters	2 Digit ASCII Characters
60647	Output 2 Leftmost 2 Characters	2 Digit ASCII Characters
60648	Output 3 Rightmost 2 Characters	2 Digit ASCII Characters
60649	Output 3 Characters	2 Digit ASCII Characters
60650	Output 3 Characters	2 Digit ASCII Characters
60651	Output 3 Leftmost 2 Characters	2 Digit ASCII Characters
60652	Output 4 Rightmost 2 Characters	2 Digit ASCII Characters
60653	Output 4 Characters	2 Digit ASCII Characters
60654	Output 4 Characters	2 Digit ASCII Characters
60655	Output 4 Leftmost 2 Characters	2 Digit ASCII Characters

Address	Item	Description
60656	Output 5 Rightmost 2 Characters	2 Digit ASCII Characters
60657	Output 5 Characters	2 Digit ASCII Characters
60658	Output 5 Characters	2 Digit ASCII Characters
60659	Output 5 Leftmost 2 Characters	2 Digit ASCII Characters
60660	Output 6 Rightmost 2 Characters	2 Digit ASCII Characters
60661	Output 6 Characters	2 Digit ASCII Characters
60662	Output 6 Characters	2 Digit ASCII Characters
60663	Output 6 Leftmost 2 Characters	2 Digit ASCII Characters
60664	Output 7 Rightmost 2 Characters	2 Digit ASCII Characters
60665	Output 7 Characters	2 Digit ASCII Characters
60666	Output 7 Characters	2 Digit ASCII Characters
60667	Output 7 Leftmost 2 Characters	2 Digit ASCII Characters
60668	Output 8 Rightmost 2 Characters	2 Digit ASCII Characters
60669	Output 8 Characters	2 Digit ASCII Characters
60670	Output 8 Characters	2 Digit ASCII Characters
60671	Output 8 Leftmost 2 Characters	2 Digit ASCII Characters
60672	Output 9 Rightmost 2 Characters	2 Digit ASCII Characters
60673	Output 9 Characters	2 Digit ASCII Characters
60674	Output 9 Characters	2 Digit ASCII Characters
60675	Output 9 Leftmost 2 Characters	2 Digit ASCII Characters
60676	Output 10 Rightmost 2 Characters	2 Digit ASCII Characters
60677	Output 10 Characters	2 Digit ASCII Characters
60678	Output 10 Characters	2 Digit ASCII Characters
60679	Output 10 Leftmost 2 Characters	2 Digit ASCII Characters
60680	Output 11 Rightmost 2 Characters	2 Digit ASCII Characters
60681	Output 11 Characters	2 Digit ASCII Characters
60682	Output 11 Characters	2 Digit ASCII Characters
60683	Output 11 Leftmost 2 Characters	2 Digit ASCII Characters
60684	Output 12 Rightmost 2 Characters	2 Digit ASCII Characters
60685	Output 12 Characters	2 Digit ASCII Characters
60686	Output 12 Characters	2 Digit ASCII Characters
60687	Output 12 Leftmost 2 Characters	2 Digit ASCII Characters
60688	Output 13 Rightmost 2 Characters	2 Digit ASCII Characters
60689	Output 13 Characters	2 Digit ASCII Characters
60690	Output 13 Characters	2 Digit ASCII Characters
60691	Output 13 Leftmost 2 Characters	2 Digit ASCII Characters
60692	Output 14 Rightmost 2 Characters	2 Digit ASCII Characters
60693	Output 14 Characters	2 Digit ASCII Characters
60694	Output 14 Characters	2 Digit ASCII Characters
60695	Output 14 Leftmost 2 Characters	2 Digit ASCII Characters

Each of the Programmable Output's may be delayed to operate on a time setting. The timer configuration settings are configured by the settings transferred to Registers 60768 through 60775.

Table 12-10. Timer Delay Definitions

Address	Item	Description
60768	OUT 6 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60769	OUT 4 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60770	OUT 5 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60771	OUT 3 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60772	OUT 2 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60773	OUT 1 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
60774	OUT 7 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)

60775	OUT 8 delay in 0.01 sec inc	Unsigned Integer 16 Bits (See Note 1)
Note 1: Range is as Such 0.00 <= Range <=60 * 100 for DPU2000 0.00 <=Range <=250 * 100 for DPU1500R/DPU2000R		

PROGRAMMABLE LED USER NAMES

Within the DPU 2000R Enhanced OCI version there are 24 LED's set aside for target and visual information. 22 of the 24 LED's are programmable. Table 12-10a lists the User Name Storage Information for the DPU 2000R.

TABLE 12-10 a

Register Address	ITEM	DESCRIPTION
60776	USER NAME LED 1 Rightmost 2 Characters – NOT PROGRAMMABLE – NORMAL LED)	2 Digit ASCII Characters
60777	USER NAME LED 1 Characters – NOT PROGRAMMABLE – NORMAL LED)	2 Digit ASCII Characters
60778	USER NAME LED 1 Characters – NOT PROGRAMMABLE – NORMAL LED)	2 Digit ASCII Characters
60779	USER NAME LED 1 Leftmost 2 Characters – NOT PROGRAMMABLE – NORMAL LED)	2 Digit ASCII Characters
60780	USER NAME LED 2 Rightmost 2 Characters	2 Digit ASCII Characters
60781	USER NAME LED 2 Characters	2 Digit ASCII Characters
60782	USER NAME LED 2 Characters	2 Digit ASCII Characters
60783	USER NAME LED 2 Leftmost 2 Characters	2 Digit ASCII Characters
60784	USER NAME LED 3 Rightmost 2 Characters	2 Digit ASCII Characters
60785	USER NAME LED 3 Characters	2 Digit ASCII Characters
60786	USER NAME LED 3 Characters	2 Digit ASCII Characters
60787	USER NAME LED 3 Leftmost 2 Characters	2 Digit ASCII Characters
60788	USER NAME LED 4 Rightmost 2 Characters	2 Digit ASCII Characters
60789	USER NAME LED 4 Characters	2 Digit ASCII Characters
60790	USER NAME LED 4 Characters	2 Digit ASCII Characters
60791	USER NAME LED 4 Leftmost 2 Characters	2 Digit ASCII Characters
60792	USER NAME LED 5 Rightmost 2 Characters	2 Digit ASCII Characters
60793	USER NAME LED 5 Characters	2 Digit ASCII Characters
60794	USER NAME LED 5 Characters	2 Digit ASCII Characters
60795	USER NAME LED 5 Leftmost 2 Characters	2 Digit ASCII Characters
60796	USER NAME LED 6 Rightmost 2 Characters	2 Digit ASCII Characters
60797	USER NAME LED 6 Characters	2 Digit ASCII Characters
60798	USER NAME LED 6 Characters	2 Digit ASCII Characters
60799	USER NAME LED 6 Leftmost 2	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
	Characters	
60800	USER NAME LED 7 Rightmost 2 Characters	2 Digit ASCII Characters
60801	USER NAME LED 7 Characters	2 Digit ASCII Characters
60802	USER NAME LED 7 Characters	2 Digit ASCII Characters
60803	USER NAME LED 7 Leftmost 2 Characters	2 Digit ASCII Characters
60804	USER NAME LED 8 Rightmost 2 Characters	2 Digit ASCII Characters
60805	USER NAME LED 8 Characters	2 Digit ASCII Characters
60806	USER NAME LED 8 Characters	2 Digit ASCII Characters
60807	USER NAME LED 8 Leftmost 2 Characters	2 Digit ASCII Characters
60808	USER NAME LED 9 Rightmost 2 Characters	2 Digit ASCII Characters
60809	USER NAME LED 9 Characters	2 Digit ASCII Characters
60810	USER NAME LED 9 Characters	2 Digit ASCII Characters
60811	USER NAME LED 9 Leftmost 2 Characters	2 Digit ASCII Characters
60812	USER NAME LED 10 Rightmost 2 Characters	2 Digit ASCII Characters
60813	USER NAME LED 10 Characters	2 Digit ASCII Characters
60814	USER NAME LED 10 Characters	2 Digit ASCII Characters
60815	USER NAME LED 10 Leftmost 2 Characters	2 Digit ASCII Characters
60816	USER NAME LED 11 Rightmost 2 Characters	2 Digit ASCII Characters
60817	USER NAME LED 11 Characters	2 Digit ASCII Characters
60818	USER NAME LED 11 Characters	2 Digit ASCII Characters
60819	USER NAME LED 11 Leftmost 2 Characters	2 Digit ASCII Characters
60820	USER NAME LED 12 Rightmost 2 Characters	2 Digit ASCII Characters
60821	USER NAME LED 12 Characters	2 Digit ASCII Characters
60822	USER NAME LED 12 Characters	2 Digit ASCII Characters
60823	USER NAME LED 12 Leftmost 2 Characters	2 Digit ASCII Characters
60824	USER NAME LED 13 Rightmost 2 Characters	2 Digit ASCII Characters
60825	USER NAME LED 13 Characters	2 Digit ASCII Characters
60826	USER NAME LED 13 Characters	2 Digit ASCII Characters
60827	USER NAME LED 13 Leftmost 2 Characters	2 Digit ASCII Characters
60828	USER NAME LED 14 Rightmost 2 Characters NOT PROGRAMMABLE – TRIP LED	2 Digit ASCII Characters
60829	USER NAME LED 14 Characters NOT PROGRAMMABLE – TRIP LED	2 Digit ASCII Characters
60830	USER NAME LED 14 Characters NOT PROGRAMMABLE – TRIP LED	2 Digit ASCII Characters
60831	USER NAME LED 14 Leftmost 2 Characters NOT PROGRAMMABLE – TRIP LED	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
60832	USER NAME LED 15 Rightmost 2 Characters	2 Digit ASCII Characters
60833	USER NAME LED 15 Characters	2 Digit ASCII Characters
60834	USER NAME LED 15 Characters	2 Digit ASCII Characters
60835	USER NAME LED 15 Leftmost 2 Characters	2 Digit ASCII Characters
60836	USER NAME LED 16 Rightmost 2 Characters	2 Digit ASCII Characters
60837	USER NAME LED 16 Characters	2 Digit ASCII Characters
60838	USER NAME LED 16 Characters	2 Digit ASCII Characters
60839	USER NAME LED 16 Leftmost 2 Characters	2 Digit ASCII Characters
60840	USER NAME LED 17 Rightmost 2 Characters	2 Digit ASCII Characters
60841	USER NAME LED 17 Characters	2 Digit ASCII Characters
60842	USER NAME LED 17 Characters	2 Digit ASCII Characters
60843	USER NAME LED 17 Leftmost 2 Characters	2 Digit ASCII Characters
60844	USER NAME LED 18 Rightmost 2 Characters	2 Digit ASCII Characters
60845	USER NAME LED 18 Characters	2 Digit ASCII Characters
60846	USER NAME LED 18 Characters	2 Digit ASCII Characters
60847	USER NAME LED 18 Leftmost 2 Characters	2 Digit ASCII Characters
60848	USER NAME LED 19 Rightmost 2 Characters	2 Digit ASCII Characters
60849	USER NAME LED 19 Characters	2 Digit ASCII Characters
60850	USER NAME LED 19 Characters	2 Digit ASCII Characters
60851	USER NAME LED 19 Leftmost 2 Characters	2 Digit ASCII Characters
60852	USER NAME LED 20 Rightmost 2 Characters	2 Digit ASCII Characters
60853	USER NAME LED 20 Characters	2 Digit ASCII Characters
60854	USER NAME LED 20 Characters	2 Digit ASCII Characters
60855	USER NAME LED 20 Leftmost 2 Characters	2 Digit ASCII Characters
60856	USER NAME LED 21 Rightmost 2 Characters	2 Digit ASCII Characters
60857	USER NAME LED 21 Characters	2 Digit ASCII Characters
60858	USER NAME LED 21 Characters	2 Digit ASCII Characters
60859	USER NAME LED 21 Leftmost 2 Characters	2 Digit ASCII Characters
60860	USER NAME LED 22 Rightmost 2 Characters	2 Digit ASCII Characters
60861	USER NAME LED 22 Characters	2 Digit ASCII Characters
60862	USER NAME LED 22 Characters	2 Digit ASCII Characters
60863	USER NAME LED 22 Leftmost 2 Characters	2 Digit ASCII Characters
60864	USER NAME LED 23 Rightmost 2 Characters	2 Digit ASCII Characters
60865	USER NAME LED 23 Characters	2 Digit ASCII Characters
60866	USER NAME LED 23 Characters	2 Digit ASCII Characters
60867	USER NAME LED 23 Leftmost 2 Characters	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
60868	USER NAME LED 24 Rightmost 2 Characters	2 Digit ASCII Characters
60869	USER NAME LED 24 Characters	2 Digit ASCII Characters
60870	USER NAME LED 24 Characters	2 Digit ASCII Characters
60871	USER NAME LED 24 Characters Rightmost 2 Characters	2 Digit ASCII Characters

PROGRAMMABLE DROP OUT AFTER OPERATE TIMERS FOR PHYSICAL OUTPUT AND FEEDBACK OUTPUTS

Within Version 5.0 DPU 2000R additional timer capabilities have been offered. Instead of On delay timers as was the implementation in IED's previously designed, there are off-delay timers. These off delay timer data configuration and storage elements are stored in the registers designated in TABLE 12-10b

TABLE 12-10b:Drop Out After Operate Timer Definitions

Address	Item	Description
60872	OUT 6 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60873	OUT 4 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60874	OUT 5 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60875	OUT 3 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60876	OUT 2 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60877	OUT 1 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60878	Feedback Output 1 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60879	Feedback Output 2 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60880	Feedback Output 3 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60881	Feedback Output 4 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60882	Feedback Output 5 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60883	Feedback Output 6 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60884	Feedback Output 7 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60885	Feedback Output 8 Drop Out After Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60886	Feedback Output 1 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60887	Feedback Output 2 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60888	Feedback Output 3 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60889	Feedback Output 4 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits

60890	Feedback Output 5 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60891	Feedback Output 6 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60892	Feedback Output 7 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
60893	Feedback Output 8 Pickup Before Operate in 0.01 sec inc	Unsigned Integer 16 Bits
Note 1: Range is as Such 0.00 <= Range <=60 * 100 for DPU2000 0.00 <=Range <=250 * 100 for DPU1500R/DPU2000R		

TRANSMIT PROGRAMMABLE EXTENDED OUTPUT SELECT

The extended OCI DPU 2000R interface has the ability to perform logic on the LED outputs. This table 12-10c lists the mapping registers for AND/OR output select for the LED bits.

The AND OR SELECTION BITS ARE DESIGNATED BY THE FOLLOWING BIT PATTERN
If bit = 0, the selected logical outputs are ORed together to drive the assigned output.
If bit = 1, the selected logical outputs are ANDed together to drive the assigned output.

Bit Position:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
DPU2000:	Trip	Close	Out6	Out4	Out5	Out3	Out2	Out1	Out7	Out8	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	FB1	FB2	FB3	FB4	FB5	FB6	FB7	FB8
DPU1500R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit Position:	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit Position:	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	T17	T18	T19	T20	T21	T22	T23	T24	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

THE LATCH OUTPUT SELECTION FOR THE LEDS ARE DESIGNATED BY THE FOLLOWING BIT PATTERN

Bit Position	Definition
0	TRIP (Fixed, not programmable)
1	CLOSE (Fixed in DPU2000, mapping NOT permitted by DPU2000R or DPU1500R)
2	OUTPUT1
3	OUTPUT2
4	OUTPUT3
5	OUTPUT4
6	OUTPUT5
7	OUTPUT6
8	OUTPUT7
9	OUTPUT8
10	OUTPUT9
11	OUTPUT10
12	OUTPUT11
13	OUTPUT12
14	OUTPUT13
15	OUTPUT14
16	OUTPUT15
17	OUTPUT16
18	OUTPUT17
19	OUTPUT18
20	OUTPUT19
21	OUTPUT20
22	OUTPUT21
23	OUTPUT22
24	OUTPUT23
25	OUTPUT24
26	OUTPUT25
27	OUTPUT26
28	OUTPUT27
29	OUTPUT28
30	OUTPUT29
31	OUTPUT30

TABLE 12 –10c

Register Address	Item	Description
60896	AND/OR Selection Bits 47 – 32	Unsigned Integer 16 Bits
60897	AND/OR Selection Bits 31 - 16	Unsigned Integer 16 Bits
60898	Logical Output Selection for Programmable LED 1 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60899	Logical Output Selection for Programmable LED 1 (Bits 31-16)	Unsigned Integer 16 Bit Lo Bit Mask
60900	Logical Output Selection for Programmable LED 2 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60901	Logical Output Selection for Programmable LED 2 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60902	Logical Output Selection for Programmable LED 3 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60903	Logical Output Selection for Programmable LED 3 (Bits 31-	Unsigned Integer 16 Bits Lo Bit Mask

	16)	
60904	Logical Output Selection for Programmable LED 4 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60905	Logical Output Selection for Programmable LED 4 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60906	Logical Output Selection for Programmable LED 5 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60907	Logical Output Selection for Programmable LED 5 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60908	Logical Output Selection for Programmable LED 6 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60909	Logical Output Selection for Programmable LED 6 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60910	Logical Output Selection for Programmable LED 7 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60911	Logical Output Selection for Programmable LED 7 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60912	Logical Output Selection for Programmable LED 8 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60913	Logical Output Selection for Programmable LED 8 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60914	Logical Output Selection for Programmable LED 9 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60915	Logical Output Selection for Programmable LED 9 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60916	Logical Output Selection for Programmable LED 10 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60917	Logical Output Selection for Programmable LED 10 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60918	Logical Output Selection for Programmable LED 11 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60919	Logical Output Selection for Programmable LED 11 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60920	Logical Output Selection for Programmable LED 12 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60921	Logical Output Selection for Programmable LED 12 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60922	Logical Output Selection for Programmable LED 13 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask

60923	Logical Output Selection for Programmable LED 13 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60924	Logical Output Selection for Programmable LED 14 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60925	Logical Output Selection for Programmable LED 14 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60926	Logical Output Selection for Programmable LED 15 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60927	Logical Output Selection for Programmable LED 15 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60928	Logical Output Selection for Programmable LED 16 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60929	Logical Output Selection for Programmable LED 16 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60930	Logical Output Selection for Programmable LED 17 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60931	Logical Output Selection for Programmable LED 17 (Bits 31-16)	Unsigned Integer 16 Bit Lo Bit Mask
60932	Logical Output Selection for Programmable LED 18 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60933	Logical Output Selection for Programmable LED 18 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60934	Logical Output Selection for Programmable LED 19 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60935	Logical Output Selection for Programmable LED 19 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60936	Logical Output Selection for Programmable LED 20 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60937	Logical Output Selection for Programmable LED 20 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60938	Logical Output Selection for Programmable LED 21 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60939	Logical Output Selection for Programmable LED 21 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask
60940	Logical Output Selection for Programmable LED 22 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60941	Logical Output Selection for Programmable LED 22 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60942	Logical Output Selection for	Unsigned Integer 16 Bits

	Programmable LED 23 (Bits 15 – 0)	Hi Bit Mask
60943	Logical Output Selection for Programmable LED 23 (Bits 31- 16)	Unsigned Integer 16 Bits Lo Bit Mask
60944	Logical Output Selection for Programmable LED 24 (Bits 15 – 0)	Unsigned Integer 16 Bits Hi Bit Mask
60945	Logical Output Selection for Programmable LED 24 (Bits 31-16)	Unsigned Integer 16 Bits Lo Bit Mask

Settings

There are three setting groups possible in the DPU2000 and DPU1500R/DPU2000R. The selections are determined by the control bits set for group selection (reference Section 11). The relay settings are configured via a selected Curve Selection Type. These are based on different functions such as:

- CURVE SELECTION
- RECLOSER OPTIONS

The curve selection types are based upon whether the relay is an ANSI or IEC type. The following is the description of the codes to select the curve and recloser curves.

High byte consists of bits 15 through 8.
Low byte consists of bits 7 through 0.
(Note Bit 0 is the right most bit whereas bit 15 is the left most bit)

ANSI Curve Selection Type I
0 = Extremely Inverse
1 = Very Inverse
2 = Inverse
3 = Short Time Inverse
4 = Definite Time
5 = Long Time Extremely Inverse
6 = Long Time Very Inverse
7 = Long Time Inverse
8 = Recloser Curve
9 = User Curve 1
10 = User Curve 2
11 = User Curve 3

ANSI Curve Selection Type II
0 = Disable
1 = Extremely Inverse
2 = Very Inverse
3 = Inverse
4 = Short Time Inverse
5 = Definite Time
6 = Long Time Extremely Inverse
7 = Long Time Very Inverse
8 = Long Time Inverse
9 = Recloser Curve
10 = User Curve 1
11 = User Curve 2
12 = User Curve 3

ANSI Curve Selection Type III
0 = Disable
1 = Standard
2 = Inverse
3 = Definite Time
4 = Short Time Inverse
5 = Short Time Extremely Inverse
6 = User Curve 1
7 = User Curve 2
8 = User Curve 3

67N Polarization Table Type IV
0=Disable
1=Enable Zero Sequence
2=Lockout Zero Sequence
3=Enable Neg Sequrnce
4=Lockout Zero Sequence

NOTE: Catalog Numbers XXXXXXXX-XX2XX and XXXXXXXX-XX3XX use the following curve types for 51P, 50P-1, 51N, and 50N-1 functions.

NOTE: The Minimum Response bytes are found in units with additional software that includes special Recloser Curves.

Recloser Curve Selection Type I
0 = A
1 = B
2 = C
3 = D
4 = E
5 = K
6 = N
7 = R
8 = W
9 = User Curve 1
10 = User Curve 2
11 = User Curve 3

Recloser Curve Selection Type II
0 = 2
1 = 3
2 = 8
3 = 8*
4 = 8+
5 = 9
6 = 11
7 = Disable
8 = User Curve 1
9 = User Curve 2
10 = User Curve 3

Recloser Curve SelectionType III
0 = Disable
1 = A
2 = B
3 = C
4 = D
5 = E
6 = K
7 = N
8 = R
9 = W
10 = User Curve 1
11 = User Curve 2
12 = User Curve 3

Recloser Curve SelectionType IV
0 = Disable
1 = 2
2 = 3
3 = 8
4 = 8*
5 = 8+
6 = 9
7 = 11
8 = User Curve 1
9 = User Curve 2
10 = User Curve 3

NOTE: The following curves are available in the IEC version of DPU2000.

IEC Curve Selection Type I
0 = Extremely Inverse
1 = Very Inverse
2 = Inverse
3 = Long Time Inverse
4 = Definite Time
5 = User Curve 1
6 = User Curve 2
7 = User Curve 3

IEC Curve Selection Type II
0 = Disabled
1 = Extremely Inverse
2 = Very Inverse
3 = Inverse
4 = Long Time Inverse
5 = Definite Time
6 = User Curve 1
7 = User Curve 2
8 = User Curve 3

IEC Curve Selection Type III
0 = Disable
1 = Standard
2 = Inverse
3 = Definite Time
4 = User Curve 1
5 = User Curve 2
6 = User Curve 3

NOTE: The following curve types are defined as ANSI/IEC curves for DPU1500R. All IEC type curves, use Time Multipliers in place of Time Dials.

ANSI/IEC Selection Type I
0 = Extremely Inverse
1 = Very Inverse
2 = Inverse
3 = Short Time Inverse
4 = Definite Time
5 = Long Time Extremely Inverse
6 = Long Time Very Inverse
7 = Long Time Inverse
8 = Recloser Curve
9 = IEC Extremely Inverse
10 = IEC Very Inverse
11 = IEC Inverse
12 = IEC Long Time Inverse
13 = User Curve 1
14 = User Curve 2
15 = User Curve 3

ANSI/IEC Selection Type II
0 = Disable
1 = Extremely Inverse
2 = Very Inverse
3 = Inverse
4 = Short Time Inverse
5 = Definite Time
6 = Long Time Extremely Inverse
7 = Long Time Very Inverse
8 = Long Time Inverse
9 = Recloser Curve
10 = IEC Extremely Inverse
11 = IEC Very Inverse
12 = IEC Inverse
13 = IEC Long Time Inverse
14 = User Curve 1
15 = User Curve 2
16 = User Curve 3

ANSI/IEC Selection Type III
0 = Disable
1 = Standard
2 = Inverse
3 = Definite Time
4 = Short Time Inverse
5 = Short Time Extremely Inverse
6 = User Curve 1
7 = User Curve 2
8 = User Curve 3

79 Lockout and Enable/Disable bit pattern
Low Byte: 0 = No Lockout/Disable, 1 = Enabled
High Byte: 0 = Enable, 1 = Lockout

bit 0: 50N-1	bit 8: 50N-1
bit 1: 50N-2	bit 9: 50N-2
bit 2: 50N-3	bit 10: 50N-3
bit 3: 51N	bit 11: 51N
bit 4: 50P-1	bit 12: 50P-1
bit 5: 50P-2	bit 13: 50P-2
bit 6: 50P-3	bit 14: 50P-3
bit 7: Reserved	bit 15: Reserved

Table 12-11 lists the register assignments for the 6X Registers for the Primary Settings Group Functions.

Table 12-11. Primary Settings Register Definition

Register Address	Item	Description
61024	SPARE_1	
61025	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61026	Access Password	ASCII – 2 Characters Leftmost Digits
61027	Access Password	ASCII – 2 Characters Rightmost Digits

Register Address	Item	Description
61028	SPARE_2	
61029	51P Curve Select (Type I or Type I Recloser)	Unsigned 16 Bits Range 0-12 (See Text Above)
61030	51P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61031	51P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51P Time Multiplier (0.05 <=Range <=1.00 * 200)
61032	50P-1 Curve Select Byte (Type III or Type III Recloser)	Unsigned Integer 16 bits 0<=Range<=12 (See Text Above)
61033	51P-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61034	51P-1 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range <=1.00 * 200)
61035	50P-2 Curve Select Byte	Unsigned Integer 16 bits 0 = Disable 1 = Enable
61036	51P-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61037	51P-2 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range <=1.00 * 200)
61038	50P-3 Curve Select Byte	Unsigned Integer 16 bits 0 = Disable 1 = Enable
61039	51P-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61040	46 Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)
61041	46 Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61042	46 Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 46 Time Multiplier (0.05 <=Range <=1.00 * 200)
61043	51N Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)
61044	51N Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61045	51N Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51N Time Multiplier (0.05 <=Range <=1.00 * 200)
61046	50N-1 Curve Select Byte (Type III or Type IV Recloser)	Unsigned Integer 16 Bits 0<=Range<=12 (See Text Above)
61047	51N-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61048	51N-1 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51N-1 Time Multiplier (0.05 <=Range <=1.00 * 200)
61049	50N-2 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (or Standard if Sensitive Earth Model)

Register Address	Item	Description
		2 = Sensitive Earth Fault (if Sensitive Earth Model) 3 = Directional Sensitive Earth Fault (if Sensitive Earth Model)
61050	51N-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61051	51N-2 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version+51N-2 Time Multiplier (0.05 <=Range<=1.00 * 200)
61052	50N-3 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61053	51N-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61054	79 Reset Time Byte	Unsigned 16 Bits 3<=Range<=200
61055	79-1 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8- 5) (See 79 Lockout/Recloser Type description above)
	79-1 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61056	79-1 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001= Lockout) 0.1<=Range<=1800 *10 (18001= “) if Sensitive Earth Model
61057	79-2 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61058	79-2 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
	79-2 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001= Lockout) 0.1<=Range<=1800 *10 (18001= “) if Sensitive Earth Model
61059	79-3 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61060	79-3 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
	79-3 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001= Lockout) 0.1<=Range<=1800 *10 (18001= “) if Sensitive Earth Model
61061	79-4 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61062	79-4 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
	79-4 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001= Lockout) 0.1<=Range<=1800 *10 (18001= “) if Sensitive Earth Model
61063	79-5 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61064	79-5 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
	79-5 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 2001 = Lockout 18001 = “
61065	79 Cutout Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)

Register Address	Item	Description
61066	Cold load Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)
61067	2 Phase Voting Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61068	67P Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable 2 = Lockout
61069	67P Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61070	67P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61071	67P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05 <=Range<=1.00 * 200)
61072	67P Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61073	67N Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (if SEF – Enable Neg. Seq.) 2 = Lockout (if SEF – Lockout Neg. Seq.) 5 = SEF Only – Enable Pos. Sequence 6 = Lockout Pos. Sequence
61074	67N Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61075	67N Pickup Amps	Unsigned 16 Bits 1<=Range<= 12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61076	67N Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05 <=Range<=1.00 * 200)
61077	67N Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61078	81 Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = 81-1 Function 2 = 81-2 Function 3 = Special
61079	81-S Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61080	81S-1 Time Delay	Unsigned Integer 16 Bits 0.08<=Range<=9.98 * 100
61081	81R-1 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61082	81R-1 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61083	81V Voltage	Unsigned Integer 16 Bits 40<=Range<=200

Register Address	Item	Description
61084	27 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61085	27 Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61086	27 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61087	79V Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61088	79V Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61089	79V Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200 Seconds
61090	59 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61091	59 Pickup Voltage	Unsigned Integer 16 Bits 70<=Range<=250
61092	59 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61093	51P Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61094	51N Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61095	51P-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61096	51N-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61097	Unit Configuration Byte Bit 0 = Neutral Tap Range Bit 1 = Phase Tap Range Bit 2 = Frequency Range Bit 3 = Cold Load Timer Bit 4 = User Definable Curves Bit 5 = Recloser Curves Bit 6 = Version Select Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Unsigned Integer 16 Bits 0 = 1-12A, 1 = 0.2 – 2.4 A 0 = 1-12A, 1 = 0.2 – 2.4 A 0 = 60 Hz, 1 = 50 Hz 0 = seconds, 1 = minutes 0 = Disabled, 1 = Enabled 0 = Disabled, 1 = Enabled 0 = ANSI, 1 = IEC
61098	81S-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401=Disable)
61099	81S-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61100	81R-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable)

Register Address	Item	Description
		If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61101	81R-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61102	SEF Torque Angle (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61103	SEF 50N-2 Pickup (Sensitive Earth Model)	Unsigned Integer 16 Bits 0.005<=Range 0.060 * 2000 (mA)
61104	Neutral Cold Load (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=254 (255 Disabled)
61105	32P Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61106	32P Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61107	32N Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61108	32N Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61109	25 Select Bit 0 = Sync Check Bit 1 = DBLL (Dead Bus Live Line) Bit 2 = LBLL (Live Bus Live Line) Bit 3 = LBDL (Live Bus Dead Line) Bit 4 = Reclose Supv.	Unsigned Integer 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable
61110	25 Voltage Difference	Unsigned Integer 5<=Range 80
61111	25 Angle Difference	Unsigned Integer 16 Bits 1<=Range<=90
61112	25 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61113	25 Slip Frequency	Unsigned Integer 16 Bits 0.005<=Range<=1
61114	25 Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200
61115	25 Breaker Close Time	Unsigned Integer 16 Bits 0<=Range<=20, 21 = Disabled
61116	25 Phase Select	Unsigned Integer 16 Bits 0 = Phase A 1 = Phase B 2 = Phase C
61117	25 Dead Voltage	Unsigned Integer 16 Bits 10<=Range<=150
61118	25 Live Voltage	Unsigned Integer 16 Bits 10<=Range<=150
61119	25 Dead Time	Unsigned Integer 16 Bits 0<=Range<=120
61120	25 Fail Time	Unsigned Integer 16 Bits 0<=Range<=600
61121	59G Enable	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61122	3VO Pickup	Unsigned Integer 16 Bits 1<=Range<=50 V * 10 : Step = 0.5*10
61123	Time Delay	Unsigned Integer 16 Bits

Register Address	Item	Description
		0<=Range<=60
61124	47 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61125	47 Pickup	Unsigned Integer 16 Bits 5<=Range<=25 V
61126	47 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61127	21P-1 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61128	21P-1 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61129	21P-1 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61130	21P-1 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61131	21P-1 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61132	21P-2 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61133	21P-2 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61134	21P-2 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61135	21P-2 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61136	21P-2 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61137	21P-3 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61138	21P-3 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61139	21P-3 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61140	21P-3 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61141	21P-3 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61142	21P-4 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61143	21P-4 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61144	21P-4 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61145	21P-4 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61146	21P-4 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61147	46A Curve Select Byte	TYPE II Unsigned Integer 16 Bits
61148	46 A of 51P Pickup Amps	Unsigned Integer – 16 Bits 5<=X <=15 Step 5 Scale * 1 in Percent
61149	46A Time Dial	Unsigned Integer – 16 Bits 1<=X<= 20 : Step 1 Scale * 20

If the Alternate Settings 1 command is selected (as per Section 11 in this document), the settings are configured as follows in Table 12-12).

Table 12-12. ALT 1 Settings Register Definition

Register Address	Item	Description
61152	SPARE_1	
61153	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61154	Access Password	ASCII – 2 Characters Leftmost Digits
61155	Access Password	ASCII – 2 Characters Rightmost Digits
61156	SPARE_2	
61157	51P Curve Select Byte (Type I or Recloser Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61158	51P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61159	51P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51P Time Multiplier (0.05 <=Range<=1.00 * 200)
61160	50P-1 Curve Select Byte (Type III or Recloser Type III)	Unsigned Integer 16 Bits 0<=Range<=12 (See Text Above)
61161	51P-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61162	51P-1 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range<=1.00 * 200)
61163	50P-2 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61164	51P-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61165	51P-2 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range<=1.00 * 200)
61166	50P-3 Curve Select Byte	Unsigned Integer 16 bits 0 = Disable 1 = Enable
61167	51P-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61168	46 Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)
61169	46 Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61170	46 Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 46 Time Multiplier (0.05 <=Range<=1.00 * 200)
61171	51N Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)
61172	51N Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61173	51N Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51N Time Multiplier (0.05 <=Range<=1.00 * 200)

Register Address	Item	Description
61174	50N-1 Curve Select Byte (Type III or Recloser Type IV)	Unsigned Integer 16 Bits 0<=Range<=12 (See Text Above)
61175	51N-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
	51N-1 Time Dial	Unsigned 16 Bits 1<=Range<=10 /Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51N-1 Time Multiplier (0.05 <=Range<=1.00 * 200)
61176	50N-2 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (or Standard if Sensitive Earth Model) 2 = Sensitive Earth Fault (if Sensitive Earth Model) 3 = Directional Sensitive Earth Fault (if Sensitive Earth Model)
61177	51N-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61178	51N-2 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51N-2 Time Multiplier (0.05 <=Range<=1.00 * 200)
	50N-3 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61179	51N-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61180	79 Reset Time Byte	Unsigned 16 Bits 3<=Range<=200
	79-1 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61181	79-1 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61182	79-1 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
	79-2 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61183	79-2 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61184	79-2 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
	79-3 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61185	79-3 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61186	79-3 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61187	79-4 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61188	79-4 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61189	79-4 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout)

Register Address	Item	Description
		0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61190	79-5 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61191	79-5 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61192	79-5 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 2001 = Lockout 18001 = “
61193	79 Cutout Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)
61194	Cold load Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)
61195	2 Phase Voting Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61196	67P Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable 2 = Lockout
61197	67P Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61198	67P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61199	67P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05 <=Range<=1.00 * 200)
61200	67P Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61201	67N Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (if SEF – Enable Neg. Seq.) 2 = Lockout (if SEF – Lockout Neg. Seq.) 5 = SEF Only – Enable Pos. Sequence 6 = Lockout Pos. Sequence
61202	67N Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61203	67N Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61204	67N Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05 <=Range<=1.00 * 200)
61205	67N Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61206	81 Select Byte	Unsigned Integer 16 Bits 1 = 81-1 Function 2 = 81-2 Function 3 = Special
61207	81-S Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)

Register Address	Item	Description
61208	81S-1 Time Delay	Unsigned Integer 16 Bits 0.08<=Range<=9.98 * 100
61209	81R-1 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61210	81R-1 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61211	81V Voltage	Unsigned Integer 16 Bits 40<=Range<=200
61212	27 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61213	27 Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61214	27 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61215	79V Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61216	79V Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61217	79V Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200 Seconds
61218	59 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61219	59 Pickup Voltage	Unsigned Integer 16 Bits 70<=Range<=250
61220	59 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61221	51P Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61222	51N Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61223	51P-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61224	51N-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61225	Unit Configuration Byte Bit 0 = Neutral Tap Range Bit 1 = Phase Tap Range Bit 2 = Frequency Range Bit 3 = Cold Load Timer Bit 4 = User Definable Curves Bit 5 = Recloser Curves Bit 6 = Version Select Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved	Unsigned Integer 16 Bits 0 = 1-12A, 1 = 0.2-2.4 A 0 = 1-12A, 1 = 0.2-2.4 A 0 = 60 Hz, 1 = 50 Hz 0 = seconds, 1 = minutes 0 = Disabled, 1= Enabled 0 = Disabled, 1= Enabled 0 = ANSI, 1= IEC

Register Address	Item	Description
	Bit 15 = Reserved	
61226	81S-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61227	81S-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61228	81R-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61229	81R-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61230	SEF Torque Angle (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61231	SEF 50N-2 Pickup (Sensitive Earth Model)	Unsigned Integer 16 Bits 0.005<=Range 0.060 * 2000 (mA)
61232	Neutral Cold Load (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=254 (255 Disabled)
61233	32P Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61234	32P Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61235	32N Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61236	32N Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61237	25 Select Bit 0 = Sync Check Bit 1 = DBLL (Dead Bus Live Line) Bit 2 = LBLL (Live Bus Live Line) Bit 3 = LBDL (Live Bus Dead Line) Bit 4 = Reclose Supv.	Unsigned Integer 16 Bits 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable
61238	25 Voltage Difference	Unsigned Integer 16 Bits 5<=Range 80
61239	25 Angle Difference	Unsigned Integer 16 Bits 1<=Range<=90
61240	25 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61241	25 Slip Frequency	Unsigned Integer 16 Bits 0.005<=Range<=1
61242	25 Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200
61243	25 Breaker Close Time	Unsigned Integer 16 Bits 0<=Range<=20, 21 = Disabled
61244	25 Phase Select	Unsigned Integer 16 Bits 0 = Phase A 1 = Phase B 2 = Phase C
61245	25 Dead Voltage	Unsigned Integer 16 Bits 10<=Range<=150

Register Address	Item	Description
61246	25 Live Voltage	Unsigned Integer 16 Bits 10<=Range<=150
61247	25 Dead Time	Unsigned Integer 16 Bits 0<=Range<=120
61248	25 Fail Time	Unsigned Integer 16 Bits 0<=Range<=600
61249	59G Enable	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61250	3VO Pickup	Unsigned Integer 16 Bits 1<=Range<=50 V * 10 : Step = 0.5*10
61251	Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61252	47 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61253	47 Pickup	Unsigned Integer 16 Bits 5<=Range<=25 V
61254	47 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61255	21P-1 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61256	21P-1 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61257	21P-1 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61258	21P-1 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61259	21P-1 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61260	21P-2 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61261	21P-2 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61262	21P-2 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61263	21P-2 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61264	21P-2 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61265	21P-3 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61266	21P-3 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61267	21P-3 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61268	21P-3 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61269	21P-3 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61270	21P-4 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61271	21P-4 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61272	21P-4 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90

Register Address	Item	Description
61273	21P-4 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61274	21P-4 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61275	46A Curve Select Byte	TYPE II Unsigned Integer 16 Bits
61276	46 A of 51P Pickup Amps	Unsigned Integer – 16 Bits 5<=X <=15 Step 5 Scale * 1 in Percent
61277	46A Time Dial	Unsigned Integer – 16 Bits 1<=X<= 20 : Step 1 Scale * 20

If the Alternate Settings 2 command is selected (as per Section 11 in this document), the settings are configured as follows in Table 12-13).

Table 12-13. ALT 2 Settings Register Definition

Register Address	Item	Description
61280	SPARE_1	
61281	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61282	Access Password	ASCII – 2 Characters Leftmost Digits
61283	Access Password	ASCII – 2 Characters Rightmost Digits
61284	SPARE_2	
61285	51P Curve Select (Type I or Recloser Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61286	51P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61287	51P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51P Time Multiplier (0.05 <=Range<=1.00 * 200)
61288	50P-1 Curve Select Byte (Type III or Recloser Type III)	Unsigned Integer 16 Bits 0<=Range<=12 (See Text Above)
61289	51P-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61290	51P-1 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range<=1.00 * 200)
61291	50P-2 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61292	51P-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61293	51P-2 Time Dial	Unsigned 16 Bits 1<=Range<=10 /Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51P-1 Time Multiplier (0.05 <=Range<=1.00 * 200)
61294	50P-3 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61295	51P-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
	46 Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)

Register Address	Item	Description
61296	46 Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61297	46 Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 46 Time Multiplier (0.05 <=Range<=1.00 * 200)
61298	51N Curve Select (Type II)	Unsigned 16 Bits Range 0-12 (See Text Above)
	51N Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61299	51N Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 51N Time Multiplier (0.05 <=Range<=1.00 * 200)
61300	50N-1 Curve Select Byte (Type III or Recloser Type IV)	Unsigned Integer 16 Bits 0<=Range<=12 (See Text Above)
	51N-1 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61301	51N-1 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51N-1 Time Multiplier (0.05<=Range<=1.00 * 200)
61302	50N-2 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (or Standard if Sensitive Earth Model) 2 = Sensitive Earth Fault (if Sensitive Earth Model) 3 = Directional Sensitive Earth Fault (if Sensitive Earth Model)
	51N-2 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61303	51N-2 Time Dial	Unsigned 16 Bits 1<=Range<=10/Delay Byte 0<=Range<=9.99 * 100 or IEC Version 51N-2 Time Multiplier (0.05<=Range<=1.00 * 200)
61304	50N-3 Curve Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
	51N-3 Pickup Amps	Unsigned 16 Bits 0.5<=Range<= 20 *10
61305	79 Reset Time Byte	Unsigned 16 Bits 3<=Range<=200
61306	79-1 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61307	79-1 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61308	79-1 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61309	79-2 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61310	79-2 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61311	79-2 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61312	79-3 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15)

Register Address	Item	Description
		(See 79 Lockout/Recloser Type description above)
61313	79-3 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61314	79-3 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61315	79-4 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61316	79-4 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61317	79-4 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 0.1<=Range<=200 * 10 (2001 = Lockout) 0.1<=Range<=1800 *10 (18001 = “) if Sensitive Earth Model
61318	79-5 Select Hi Byte	Unsigned 16 Bits (Hi Byte Bits 8-15) (See 79 Lockout/Recloser Type description above)
61319	79-5 Select Lo Byte	Unsigned 16 Bits (Lo Byte Bits 0-7) (See 79 Lockout/Recloser Type description above)
61320	79-5 Open Interval Time (Seconds)	Unsigned Integer 16 Bits 2001 = Lockout 18001 = “
61321	79 Cutout Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)
61322	Cold Load Time Byte	Unsigned Integer 16 Bits 1<=Range<=201 (201 = Lockout)
61323	2 Phase Voting Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61324	67P Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable 2 = Lockout
61325	67P Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61326	67P Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)
61327	67P Time Dial	Unsigned 16 Bits 1<=Range<=20/Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05<=Range<=1.00 * 200)
61328	67P Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61329	67N Select Byte	Unsigned Integer 16 Bits 0 = Disable 1 = Enable (if SEF – Enable Neg. Seq.) 2 = Lockout (if SEF – Lockout Neg. Seq.) 5 = SEF Only – Enable Pos. Sequence 6 = Lockout Pos. Sequence
61330	67N Curve Select (Type I)	Unsigned 16 Bits Range 0-12 (See Text Above)
61331	67N Pickup Amps	Unsigned 16 Bits 1<=Range<=12 *10 0.2<=Range<=2.4 Amp * 50 (See Note)

Register Address	Item	Description
61332	67N Time Dial	Unsigned 16 Bits 1<=Range<=20 /Delay Byte 0<=Range<=10 * 20 or IEC Version 67P Time Multiplier (0.05 <=Range<=1.00 * 200)
61333	67N Torque Angle Byte	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61334	81 Select Byte	Unsigned Integer 16 Bits 1 = 81-1 Function 2 = 81-2 Function 3 = Special
61335	81-S Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61336	81S-1 Time Delay	Unsigned Integer16 Bits 0.08<=Range<=9.98 * 100
61337	81R-1 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61338	81R-1 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61339	81V Voltage	Unsigned Integer 16 Bits 40<=Range<=200
61340	27 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61341	27 Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61342	27 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61343	79V Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61344	79V Pickup Voltage	Unsigned Integer 16 Bits 10<=Range<=200
61345	79V Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200 Seconds
61346	59 Select Byte	Unsigned Integer 16 Bits 0 = Disabled 1 = Enabled
61347	59 Pickup Voltage	Unsigned Integer 16 Bits 70<=Range<=250
61348	59 Time Delay Byte	Unsigned Integer 16 Bits 0<=Range<=60 Seconds
61349	51P Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61350	51N Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61351	51P-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61352	51N-1 Minimum Response (Cycles)	Unsigned Integer 16 Bits 0<=Range<=60 Cycles
61353	Unit Configuration Byte	Unsigned Integer 16 Bits

Register Address	Item	Description
	Bit 0 = Neutral Tap Range Bit 1 = Phase Tap Range Bit 2 = Frequency Range Bit 3 = Cold Load Timer Bit 4 = User Definable Curves Bit 5 = Recloser Curves Bit 6 = Version Select Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	0 = 1-12A, 1= 0.2 – 2.4 A 0 = 1-12A, 1= 0.2 – 2.4 A 0 = 60 Hz, 1 = 50 Hz 0 = seconds, 1 = minutes 0 = Disabled, 1= Enabled 0 = Disabled, 1= Enabled 0 = ANSI, 1= IEC
61354	81S-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61355	81S-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61356	81R-2 Pickup Frequency	Unsigned Integer 16 Bits If 60 Hz 56<=Range<=64 *100 (6401 = Disable) If 50 Hz 46<=Range<=54 *100 (5401 = Disable)
61357	81R-2 Time Delay	Unsigned Integer 16 Bits 0<=Range<=999 Seconds
61358	SEF Torque Angle (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61359	SEF 50N-2 Pickup (Sensitive Earth Model)	Unsigned Integer 16 Bits 0.005<=Range0.060 * 2000 (mA)
61360	Neutral Cold Load (Sensitive Earth Model)	Unsigned Integer 16 Bits 0<=Range<=254 (255 Disabled)
61361	32P Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61362	32P Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61363	32N Select	Unsigned Integer 16 Bits 0 = Disable 1 = Enable
61364	32N Torque Angle	Unsigned Integer 16 Bits 0<=Range<=355 (Step 5) Degrees
61365	25 Select Bit 0 = Sync Check Bit 1 = DBLL (Dead Bus Live Line) Bit 2 = LBLL (Live Bus Live Line) Bit 3 = LBDL (Live Bus Dead Line) Bit 4 = Reclose Supv.	Unsigned Integer 16 Bits 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable 0 = Disable, 1 = Enable
61366	25 Voltage Difference	Unsigned Integer 16 Bits 5<=Range 80
61367	25 Angle Difference	Unsigned Integer 16 Bits 1<=Range<=90

Register Address	Item	Description
61368	25 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61369	25 Slip Frequency	Unsigned Integer 16 Bits 0.005<=Range<=1
61370	25 Time Delay Byte	Unsigned Integer 16 Bits 4<=Range<=200
61371	25 Breaker Close Time	Unsigned Integer 16 Bits 0<=Range<=20, 21 = Disabled
61372	25 Phase Select	Unsigned Integer 16 Bits 0 = Phase A 1 = Phase B 2 = Phase C
61373	25 Dead Voltage	Unsigned Integer 16 Bits 10<=Range<=150
61374	25 Live Voltage	Unsigned Integer 16 Bits 10<=Range<=150
61375	25 Dead Time	Unsigned Integer 16 Bits 0<=Range<=120
61376	25 Fail Time	Unsigned Integer 16 Bits 0<=Range<=600
61377	59G Enable	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61278	3VO Pickup	Unsigned Integer 16 Bits 1<=Range<=50 V * 10 : Step = 0.5*10
61379	Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61380	47 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61381	47 Pickup	Unsigned Integer 16 Bits 5<=Range<=25 V
61382	47 Time Delay	Unsigned Integer 16 Bits 0<=Range<=60
61383	21P-1 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61384	21P-1 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61385	21P-1 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61386	21P-1 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61387	21P-1 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61278	21P-2 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61389	21P-2 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61390	21P-2 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61391	21P-2 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61392	21P-2 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61393	21P-3 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61394	21P-3 Forward Reach	Unsigned Integer 16 Bits

Register Address	Item	Description
		1<=Range 500: step 1 – Scale *10
61395	21P-3 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61396	21P-3 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61397	21P-3 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61278	21P-4 Select	Unsigned Integer 16 Bits 0 = Disable : 1 = Enable
61399	21P-4 Forward Reach	Unsigned Integer 16 Bits 1<=Range 500: step 1 – Scale *10
61400	21P-4 Characteristic Angle	Unsigned Integer 16 Bits 0<=Range<=90
61401	21P-4 Time Delay	Unsigned Integer 16 Bits 1<=Range<100 : Step 1 , Scale * 10
61402	21P-4 Positive Sequence Supervision	Unsinged Integer – 16 Bits 100<=Range <=600 : Step 1 Scale * 10
61403	46A Curve Select Byte	TYPE II Unsigned Integer 16 Bits
61404	46 A of 51P Pickup Amps	Unsigned Integer – 16 Bits 5<=X <=15 Step 5 Scale * 1 in Percent
61405	46A Time Dial	Unsigned Integer – 16 Bits 1<=X<= 20 : Step 1 Scale * 20

Configuration Settings

The DPU2000 and DPU1500R/DPU2000R has configuration settings which may be set through the unit's Front Panel Interface (FPI), ECP (External Communication Program), WinECP (Windows External Communication Program) or via Modbus/Modbus Plus via Registers 61408 through 61443. Table 12-14 lists the register definitions for the DPU2000 and DPU1500R/DPU 2000R configuration settings.

Table 12-14. Configuration Settings Register Definitions

Register Address	Item	Description
61408	SPARE_1	
61409	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61410	Access Password	ASCII – 2 Characters Leftmost Digits
61411	Access Password	ASCII – 2 Characters Rightmost Digits
61412	SPARE_2	
61413	Phase CT Ratio	Unsigned Integer 16 Bits 1<=Range<=2000
61414	Neutral CT Ratio	Unsigned Integer 16 Bits 1<=Range<=2000
61415	VT Ratio	Unsigned Integer 16 Bits 1<=Range<=2000
61416	VT Connection	Unsigned Integer 16 Bits 0 = 69 V Wye 1 = 120 V Wye 2 = 120 V Delta 3 = 208 V Delta
61417	Positive Sequence Reactance	Unsigned Integer 16 Bits 0.01<=Range<=4 * 1000

61418	Positive Sequence Resistance	Unsigned Integer 16 Bits 0.01<=Range<=4 * 1000
61419	Zero Sequence Reactance	Unsigned Integer 16 Bits 0.01<=Range<=4 * 1000
61420	Zero Sequence Resistance	Unsigned Integer 16 Bits 0.01<=Range<=4 * 1000
61421	Distance In Miles IEC Distance In KM	Unsigned Integer 16 Bits 0.1<=Range<=125 *10 0.1<=Range<=200 * 10
61422	Trip Failure Time	Unsigned Integer 16 Bits 5<=Range<=60
61423	Close Failure Time	Unsigned Integer 16 Bits 18<=Range<= 999
61424	Phase Rotation	Unsigned Integer 16 Bits 0 = ABC 1 = ACB
61425	Configuration Flag Bit 1 = Protection Mode Bit 2 = Reset Mode Bit 3 = Zone Sequence Bit 4 = Local Edit Bit 5 = Remote Edit Bit 6 = Whr/VarHr Mtr Mode Bit 7 = LCD light Bit 8 = Multi-Device Trip Bit 9 = VCN Special Mode Bit 10 = Cold Load Timer Bit 11 = IEC Mode Bit Bit 12 = 79V Timer Mode Bit 13 = Voltage Disp Mode Bit 14 = Reserved Bit 15 = Reserved	Unsigned Integer 16 Bits 0 = Fundamental, 1= RMS 0 = Instant, 1 = Delayed 0 = Disabled, 1 = Enabled 0 = Disabled, 1 = Enabled 0 = Disabled, 1 = Enabled 0 = Kwh, 1 = MwHr 0 =Timer, 1= On 0 = Disabled, 1 = Enabled 0 = Normal, 1 = Inverted 0 = Seconds, 1 = Minutes 0 = ANSI, 1 = IEC 0 = Seconds, 1 = Minutes 0 = Vln, 1 = Vline to line Reserved Reserved
61426	ALT 1 Setting Enable	Unsigned Integer 16 Bits 1 = Enabled, 0 = Disabled
61427	ALT 2 Setting Enable	Unsigned Integer 16 Bits 1 = Enabled, 0 = Disabled
61428	Demand Time Constant	Unsigned Integer 16 Bits 0 = 5 Min 1 = 15 Min 2 = 30 Min 3 = 60 Min
61429	Sensitive Earth CT Ratio	Unsigned Integer 16 Bits 1<=Range<=2000
61430	Unit Name	ASCII – 2 Characters Leftmost Digits
61431	Unit Name	ASCII – 2 Characters Digits
61432	Unit Name	ASCII – 2 Characters Digits
61433	Unit Name	ASCII – 2 Characters Digits
61434	Unit Name	ASCII – 2 Characters Digits
61435	Unit Name	ASCII – 2 Characters Digits
61436	Unit Name	ASCII – 2 Characters Digits
61437	Unit Name	ASCII – 2 Characters Rightmost Digits
61438	Sensitive Earth V0 PT Ratio	Unsigned Integer 16 Bits 1<=Range<=2000
61439	LCD Contrast Adjustment	Unsigned Integer 16 Bits 0<=Range<=63
61440	Relay Password	ASCII – 2 Characters Leftmost Digits
61441	Relay Password	ASCII – 2 Characters Rightmost Digits

61442	Test Password	ASCII – 2 Characters Leftmost Digits
61443	Test Password	ASCII – 2 Characters Rightmost Digits
61444	Cx ACTIVE Bit 0 = C1 Bit 1 = C2 Bit 2 = C3 Bit 3 = C4 Bit 4 = C5 Bit 5 = C6 Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Unsigned Integer C1 0= Key Inactive 1 = Key Active (LSB) C2 0= Key Inactive 1 = Key Active C3 0= Key Inactive 1 = Key Active C4 0= Key Inactive 1 = Key Active C5 0= Key Inactive 1 = Key Active C6 0= Key Inactive 1 = Key Active Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved (MSB)
61445	BkrCtlActive	Unsigned Integer 0 = Disable Circuit Breaker Control buttons. 1 = Enable Circuit Breaker Control buttons. 2 = Set Circuit Breaker Control buttons to LEDs Only.
61446	BF_Enable	Unsigned Integer – Breaker Fail Enable
61447	BF_PUDelay	Unsigned Integer – Breaker Fail Pickup Delay
61448	BF_Drop Delay	Unsigned Integer- Breaker Fail Dropout Delay
61449	BF_Starters	Unsigned Integer –Breaker Fail Start Delay
61450	ReTripPU_Delay	Unsigned Integer Retrip Pickup Delay
61451	ReTripDropDelay	Unsigned Integer – Retrip Dropout Delay
61452	ReTrip_Starters	Unsigned Integer – Retrip Start Delay
61453	BF_Ph_Pickup	Unsinged Integer – Breaker Fail Phase Pickup
61454	Gnd_Pickup	Unsigned Integer – Ground Pickup Time
61455	Slow Trip Time	Unsigned Integer – Slow Breaker Trip Config Time
61456	SHIFTA No. of Outputs	Unsigned Integer – Test Shifter Output Assigment Shifter A.
61457	SHIFTB No. of Outputs	Unsigned Integer – Test Shifter Output Assigment Shifter B.
61458	CX Key Action Bit 0 = C1 Bit 1 = C2 Bit 2 = C3 Bit 3 = C4 Bit 4 = C5 Bit 5 = C6 Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Unsigned Integer – C1 1= Momentary 0 = Maintained (LSB) C2 1= Momentary 0 = Maintained C3 1= Momentary 0 = Maintained C4 1= Momentary 0 = Maintained C5 1= Momentary 0 = Maintained C6 1= Momentary 0 = Maintained Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved (MSB)

Breaker Counters (21 Registers Defined)

DPU2000/DPU1500R/2000R has the ability to count breaker operations in a variety of modes. The same registers can be accessed via a Modbus Code 03 (Read Holding Registers). For 4X read access, refer to Table 12-15. The same information can be read via the refresh register capability through Register 61922. To reset the Breaker Counters, write the value of 0 to Registers 61926 through 61936.

Table 12-15. Breaker Counter Register Assignment

Register Address	Item	Description
61536	SPARE_1	
61537	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61538	Access Password	ASCII – 2 Characters Leftmost Digits
61539	Access Password	ASCII – 2 Characters Rightmost Digits
61540	SPARE_2	
61541	KSIA	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ia – Current existing when breaker opened on Phase A.
61542	KSIB	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ib – Current existing when breaker opened on Phase B.
61543	KSIC	Unsigned 16 Bits 0 – 9999 Kiloamps Symmetrical Ic – Current existing when breaker opened on Phase C.
61544	Overcurrent Trip Counter	Unsigned 16 Bits 0 – 9999
61545	Breaker Operation Counter	Unsigned 16 Bits 0 – 9999
61546	Reclose Counter 1	Unsigned 16 Bits 0 – 9999
61547	First Reclose Counter	Unsigned 16 Bits 0 – 9999
61548	Second Reclose Counter	Unsigned 16 Bits 0 – 9999
61549	Third Reclose Counter	Unsigned 16 Bits 0 – 9999
61550	Fourth Reclose Counter	Unsigned 16 Bits 0 – 9999
61551	Reclose Counter 2	Unsigned 16 Bits 0 – 9999
61552	Overcurrent Trip A Counter	Unsigned 16 Bits 0 – 9999
61553	Overcurrent Trip B Counter	Unsigned 16 Bits 0 – 9999
61554	Overcurrent Trip C Counter	Unsigned 16 Bits 0 – 9999
61555	Overcurrent Trip N Counter	Unsigned 16 Bits 0 – 9999

Alarm Settings

Counter and Metering settings may be set and configured via the registers from 61664 through 61682. Setting of the quantities is relatively straightforward. It should be noted that Positive Watt Alarm 1 and Positive Watt Alarm 2 units are displayed in either KWhr or MWhr according to bit 6 of Configuration Flag in the Configuration Settings Group. If bit is set to one, use MWhr, if bit is zero, use KWhr.

Table 12-16. Alarm Setting Table

Register Address	Item	Description
61664	SPARE_1	
61665	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61666	Access Password	ASCII – 2 Characters Leftmost Digits
61667	Access Password	ASCII – 2 Characters Rightmost Digits
61668	SPARE_2	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61669	KSI Summation Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61670	Overcurrent Trip Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61671	Reclosure Counter 1 Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61672	Phase Demand Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61673	Neutral Demand Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61674	Low PF Alarm	Unsigned Integer 0.5<=Range<=1.0 * 100, 101 Disables
61675	Hi PF Alarm	Unsigned Integer 0.5<=Range<=1.0 * 100, 101 Disables
61676	Reclosure Counter 2 Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61677	3 Phase Kvar Alarm	Unsigned Integer 16 Bits 10<=Range<=9999 , 10000 Disables
61678	Load Current Alarm	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61679	Positive KVAR Alarm	Unsigned Integer 16 Bits 10<=Range<=99990/10, 10000 Disables
61670	Negative KVAR Alarm	Unsigned Integer 16 Bits 10<=Range<=99990/10, 10000 Disables
61681	Positive Watt Alarm 1	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables
61682	Positive Watt Alarm 2	Unsigned Integer 16 Bits 0<=Range<=9999, 10000 Disables

Real Time Clock (13 Registers Defined)

The real time clock data can be set via the network. This clock is the master which is used to time stamp operational records and event records in Registers 41029 through 41036 (as defined in Table 12-17) and Registers 41284 through 41291 (as defined in Table 12-20). It should be noted that the clock registers have been updated to reflect the four digit year required for Y2K compliance in time reporting.

If the month is set to 0, the real time clock is disabled. The real time clock cannot be enabled or disabled via Modbus. The real time clock may only be disabled via DPU2000/DPU1500R/2000R Native ASCII or DPU2000/DPU1500R/2000R Fast ASCII.

Table 12-17 lists the register definition for Real Time Clock configuration.

Table 12-17. Real Time Clock Register Definition Assignment

Register Address	Item	Description
61792	SPARE_1	
61793	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61794	Access Password	ASCII – 2 Characters Leftmost Digits
61795	Access Password	ASCII – 2 Characters Rightmost Digits
61796	SPARE_2	
61797	Hour	Unsigned 16 Bits Hour Range 0-23
61798	Minute	Unsigned 16 Bits Minute Range 0-59
61799	Second	Unsigned 16 Bits Second Range 0-59
61800	Day	Unsigned 16 Bits Day Range 1-31
61801	Month	Unsigned 16 Bits Month Range 1-12
61802	Year	Unsigned 16 Bits Year Range 00-99

ULO Connection Settings and User Names

The DPU1500R/2000R has internal Soft Bits, which are used for logical boolean programming. Please reference the IL bulletin for a more detailed explanation of the use of these bits.

Table 12-18 describes the register designation.

Registers 61924 designate whether the ULO is connected to the corresponding ULI. Registers 61926 through 61958 contain the 8 characters, which make up the ULI Name. Note: Version 5.X base firmware has increased the number of ULO's from 9 to 16.

Table 12-18. ULOTable Map for Character Name Assignment

Address	Item	Description
61920	SPARE_1	
61921	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
61922	Access Password	ASCII – 2 Characters Leftmost Digits
61923	Access Password	ASCII – 2 Characters Rightmost Digits
61924	SPARE_2	
61925	ULO/ULI Connection Designation Bit 0 = ULO9 Bit 1 = ULO8 Bit 2 = ULO7 Bit 3 = ULO6 Bit 4 = ULO5 Bit 5 = ULO4 Bit 6 = ULO3 Bit 7 = ULO2 Bit 8 = ULO1 Bit 9 = Reserved	Unsigned Integer 16 Bits 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. 0 = Connected 1 = Not Con. Reserved

Address	Item	Description
	Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Reserved Reserved Reserved Reserved Reserved Reserved
61926	ULO 1 Rightmost 2 Characters	2 Digit ASCII Characters
61927	ULO 1 Characters	2 Digit ASCII Characters
61928	ULO 1 Characters	2 Digit ASCII Characters
61929	ULO 1 Leftmost 2 Characters	2 Digit ASCII Characters
61930	ULO 2 Rightmost 2 Characters	2 Digit ASCII Characters
61931	ULO 2 Characters	2 Digit ASCII Characters
61932	ULO 2 Characters	2 Digit ASCII Characters
61933	ULO 2 Leftmost 2 Characters	2 Digit ASCII Characters
61934	ULO 3 Rightmost 2 Characters	2 Digit ASCII Characters
61935	ULO 3 Characters	2 Digit ASCII Characters
61936	ULO 3 Characters	2 Digit ASCII Characters
61937	ULO 3 Leftmost 2 Characters	2 Digit ASCII Characters
61938	ULO 4 Rightmost 2 Characters	2 Digit ASCII Characters
61939	ULO 4 Characters	2 Digit ASCII Characters
61940	ULO 4 Characters	2 Digit ASCII Characters
61941	ULO 4 Leftmost 2 Characters	2 Digit ASCII Characters
61942	ULO 5 Rightmost 2 Characters	2 Digit ASCII Characters
61943	ULO 5 Characters	2 Digit ASCII Characters
61944	ULO 5 Characters	2 Digit ASCII Characters
61945	ULO 5 Leftmost 2 Characters	2 Digit ASCII Characters
61946	ULO 6 Rightmost 2 Characters	2 Digit ASCII Characters
61947	ULO 6 Characters	2 Digit ASCII Characters
61948	ULO 6 Characters	2 Digit ASCII Characters
61949	ULO 6 Leftmost 2 Characters	2 Digit ASCII Characters
61950	ULO 7 Rightmost 2 Characters	2 Digit ASCII Characters
61951	ULO 7 Characters	2 Digit ASCII Characters
61952	ULO 7 Characters	2 Digit ASCII Characters
61953	ULO 7 Leftmost 2 Characters	2 Digit ASCII Characters
61954	ULO 8 Rightmost 2 Characters	2 Digit ASCII Characters
61955	ULO 8 Characters	2 Digit ASCII Characters
61956	ULO 8 Characters	2 Digit ASCII Characters
61957	ULO 8 Leftmost 2 Characters	2 Digit ASCII Characters
61958	ULO 9 Rightmost 2 Characters	2 Digit ASCII Characters
61959	ULO 9 Characters	2 Digit ASCII Characters
61960	ULO 9 Characters	2 Digit ASCII Characters
61961	ULO 9 Leftmost 2 Characters	2 Digit ASCII Characters
61962	ULO 10 Rightmost 2 Characters	2 Digit ASCII Characters
61963	ULO 10 Characters	2 Digit ASCII Characters
61964	ULO 10 Characters	2 Digit ASCII Characters
61965	ULO 10 Leftmost 2 Characters	2 Digit ASCII Characters
61966	ULO 11 Rightmost 2 Characters	2 Digit ASCII Characters
61967	ULO 11 Characters	2 Digit ASCII Characters
61968	ULO 11 Characters	2 Digit ASCII Characters
61969	ULO 11 Leftmost 2 Characters	2 Digit ASCII Characters
61970	ULO 12 Rightmost 2 Characters	2 Digit ASCII Characters
61971	ULO 12 Characters	2 Digit ASCII Characters
61972	ULO 12 Characters	2 Digit ASCII Characters
61973	ULO 12 Leftmost 2 Characters	2 Digit ASCII Characters

Address	Item	Description
61974	ULO 13 Rightmost 2 Characters	2 Digit ASCII Characters
61975	ULO 13 Characters	2 Digit ASCII Characters
61976	ULO 13 Characters	2 Digit ASCII Characters
61977	ULO 13 Leftmost 2 Characters	2 Digit ASCII Characters
61978	ULO 14 Rightmost 2 Characters	2 Digit ASCII Characters
61979	ULO 14 Characters	2 Digit ASCII Characters
61980	ULO 14 Characters	2 Digit ASCII Characters
61981	ULO 14 Leftmost 2 Characters	2 Digit ASCII Characters
61982	ULO 15 Rightmost 2 Characters	2 Digit ASCII Characters
61983	ULO 15 Characters	2 Digit ASCII Characters
61984	ULO 15 Characters	2 Digit ASCII Characters
61985	ULO 15 Leftmost 2 Characters	2 Digit ASCII Characters
61986	ULO 16 Rightmost 2 Characters	2 Digit ASCII Characters
61987	ULO 16 Characters	2 Digit ASCII Characters
61988	ULO 16 Characters	2 Digit ASCII Characters
61989	ULO 16 Leftmost 2 Characters	2 Digit ASCII Characters

ULI Connection Settings and User Names

The DPU1500R/2000R has internal Soft Bits, which are used for logical boolean programming. Please reference the IL bulletin for a more detailed explanation of the use of these bits.

Table 12-19 describes the register designation.

Registers 61926 through 61958 contain the 8 characters, which make up the ULI Name.

Table 12-19. ULI Table Map for Character Name Assignment

Address	Item	Description
62048	SPARE_1	
62049	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
62050	Access Password	ASCII – 2 Characters Leftmost Digits
62051	Access Password	ASCII – 2 Characters Rightmost Digits
62052	SPARE_2	
62053	ULI 1 Rightmost 2 Characters	2 Digit ASCII Characters
62054	ULI 1 Characters	2 Digit ASCII Characters
62055	ULI 1 Characters	2 Digit ASCII Characters
62056	ULI 1 Leftmost 2 Characters	2 Digit ASCII Characters
62057	ULI 2 Rightmost 2 Characters	2 Digit ASCII Characters
62058	ULI 2 Characters	2 Digit ASCII Characters
62059	ULI 2 Characters	2 Digit ASCII Characters
62060	ULI 2 Leftmost 2 Characters	2 Digit ASCII Characters
62061	ULI 3 Rightmost 2 Characters	2 Digit ASCII Characters
62062	ULI 3 Characters	2 Digit ASCII Characters
62063	ULI 3 Characters	2 Digit ASCII Characters
62064	ULI 3 Leftmost 2 Characters	2 Digit ASCII Characters
62065	ULI 4 Rightmost 2 Characters	2 Digit ASCII Characters
62066	ULI 4 Characters	2 Digit ASCII Characters
62067	ULI 4 Characters	2 Digit ASCII Characters
62068	ULI 4 Leftmost 2 Characters	2 Digit ASCII Characters
62069	ULI 5 Rightmost 2 Characters	2 Digit ASCII Characters

Address	Item	Description
62070	ULI 5 Characters	2 Digit ASCII Characters
62071	ULI 5 Characters	2 Digit ASCII Characters
62072	ULI 5 Leftmost 2 Characters	2 Digit ASCII Characters
62073	ULI 6 Rightmost 2 Characters	2 Digit ASCII Characters
62074	ULI 6 Characters	2 Digit ASCII Characters
62075	ULI 6 Characters	2 Digit ASCII Characters
62076	ULI 6 Leftmost 2 Characters	2 Digit ASCII Characters
62077	ULI 7 Rightmost 2 Characters	2 Digit ASCII Characters
62078	ULI 7 Characters	2 Digit ASCII Characters
62079	ULI 7 Characters	2 Digit ASCII Characters
62080	ULI 7 Leftmost 2 Characters	2 Digit ASCII Characters
62081	ULI 8 Rightmost 2 Characters	2 Digit ASCII Characters
62082	ULI 8 Characters	2 Digit ASCII Characters
62083	ULI 8 Characters	2 Digit ASCII Characters
62084	ULI 8 Leftmost 2 Characters	2 Digit ASCII Characters
62085	ULI 9 Rightmost 2 Characters	2 Digit ASCII Characters
62086	ULI 9 Characters	2 Digit ASCII Characters
62087	ULI 9 Characters	2 Digit ASCII Characters
62088	ULI 9 Leftmost 2 Characters	2 Digit ASCII Characters
62089	ULI 10 Rightmost 2 Characters	2 Digit ASCII Characters
62090	ULI 10 Characters	2 Digit ASCII Characters
62091	ULI 10 Characters	2 Digit ASCII Characters
62092	ULI 10 Leftmost 2 Characters	2 Digit ASCII Characters
62093	ULI 11 Rightmost 2 Characters	2 Digit ASCII Characters
62094	ULI 11 Characters	2 Digit ASCII Characters
62095	ULI 11 Characters	2 Digit ASCII Characters
62096	ULI 11 Leftmost 2 Characters	2 Digit ASCII Characters
62097	ULI 12 Rightmost 2 Characters	2 Digit ASCII Characters
62098	ULI 12 Characters	2 Digit ASCII Characters
62099	ULI 12 Characters	2 Digit ASCII Characters
62100	ULI 12 Leftmost 2 Characters	2 Digit ASCII Characters
62101	ULI 13 Rightmost 2 Characters	2 Digit ASCII Characters
62102	ULI 13 Characters	2 Digit ASCII Characters
62103	ULI 13 Characters	2 Digit ASCII Characters
62104	ULI 13 Leftmost 2 Characters	2 Digit ASCII Characters
62105	ULI 14 Rightmost 2 Characters	2 Digit ASCII Characters
62106	ULI 14 Characters	2 Digit ASCII Characters
62107	ULI 14 Characters	2 Digit ASCII Characters
62108	ULI 14 Leftmost 2 Characters	2 Digit ASCII Characters
62109	ULI 15 Rightmost 2 Characters	2 Digit ASCII Characters
62110	ULI 15 Characters	2 Digit ASCII Characters
62111	ULI 15 Characters	2 Digit ASCII Characters
62112	ULI 15 Leftmost 2 Characters	2 Digit ASCII Characters
62113	ULI 16 Rightmost 2 Characters	2 Digit ASCII Characters
62114	ULI 16 Characters	2 Digit ASCII Characters
62115	ULI 16 Characters	2 Digit ASCII Characters
62116	ULI 16 Leftmost 2 Characters	2 Digit ASCII Characters

Force Logical Input Allocation and Name Assignment

The DPU1500R/2000R has the capability to assign input functions to “soft bits”. These “soft bits” are designated as Forced Logical Input Bit (FLI’s). The FLI bits may be forced through the network protocol as described in Section 11 of this document. However, the FLI’s must be mapped to a protective function to be controlled when

the bit is set. Register addresses 62180 through 62196 allocate a byte containing a code thus mapping the desired function to the bit. Registers 62197 through 62321 lists the addresses assigned for the character string assignments to each of the "soft bit" FLI controls. The register lists are contained in Table 12-20 below.

Table 12-20. FLI Soft Bit Table Map and Character Name Assignment Register Map

Register Address	ITEM	DESCRIPTION
62176	SPARE_1	
62177	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
62178	Access Password	ASCII – 2 Characters Leftmost Digits
62179	Access Password	ASCII – 2 Characters Rightmost Digits
62180	SPARE_2	
62181	FLI 1 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 2 Index Byte	Unsigned Integer Lo byte 8 right most bits
62182	FLI 3 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 4 Index Byte	Unsigned Integer Lo byte 8 right most bits
62183	FLI 5 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 6 Index Byte	Unsigned Integer Lo byte 8 right most bits
62184	FLI 7 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 8 Index Byte	Unsigned Integer Lo byte 8 right most bits
62185	FLI 9 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 10 Index Byte	Unsigned Integer Lo byte 8 right most bits
62186	FLI 11 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 12 Index Byte	Unsigned Integer Lo byte 8 right most bits
62187	FLI 13 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 14 Index Byte	Unsigned Integer Lo byte 8 right most bits
62188	FLI 15 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 16 Index Byte	Unsigned Integer Lo byte 8 right most bits
62189	FLI 17 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 18 Index Byte	Unsigned Integer Lo byte 8 right most bits
62190	FLI 19 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 20 Index Byte	Unsigned Integer Lo byte 8 right most bits
62191	FLI 21 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 22 Index Byte	Unsigned Integer Lo byte 8 right most bits
62192	FLI 23 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 24 Index Byte	Unsigned Integer Lo byte 8 right most bits
62193	FLI 25 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 26 Index Byte	Unsigned Integer Lo byte 8 right most bits
62194	FLI 27 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 28 Index Byte	Unsigned Integer Lo byte 8 right most bits
62195	FLI 29 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 30 Index Byte	Unsigned Integer Lo byte 8 right most bits
62196	FLI 31 Index Byte	Unsigned Integer Hi byte 8 leftmost bits
	FLI 32 Index Byte	Unsigned Integer Lo byte 8 right most bits
62197	FLI 1 Rightmost 2 Characters	2 Digit ASCII Characters
62198	FLI 1 Characters	2 Digit ASCII Characters
62199	FLI 1 Characters	2 Digit ASCII Characters
62200	FLI 1 Leftmost 2 Characters	2 Digit ASCII Characters
62201	FLI 2 Rightmost 2 Characters	2 Digit ASCII Characters
62202	FLI 2 Characters	2 Digit ASCII Characters
62203	FLI 2 Characters	2 Digit ASCII Characters
62204	FLI 2 Leftmost 2 Characters	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
62205	FLI 3 Rightmost 2 Characters	2 Digit ASCII Characters
62206	FLI 3 Characters	2 Digit ASCII Characters
62207	FLI 3 Characters	2 Digit ASCII Characters
62208	FLI 3 Leftmost 2 Characters	2 Digit ASCII Characters
62209	FLI 4 Rightmost 2 Characters	2 Digit ASCII Characters
62210	FLI 4 Characters	2 Digit ASCII Characters
62211	FLI 4 Characters	2 Digit ASCII Characters
62212	FLI 4 Leftmost 2 Characters	2 Digit ASCII Characters
62213	FLI 5 Rightmost 2 Characters	2 Digit ASCII Characters
62214	FLI 5 Characters	2 Digit ASCII Characters
62215	FLI 5 Characters	2 Digit ASCII Characters
62216	FLI 5 Leftmost 2 Characters	2 Digit ASCII Characters
62217	FLI 6 Rightmost 2 Characters	2 Digit ASCII Characters
62218	FLI 6 Characters	2 Digit ASCII Characters
62219	FLI 6 Characters	2 Digit ASCII Characters
62220	FLI 6 Leftmost 2 Characters	2 Digit ASCII Characters
62221	FLI 7 Rightmost 2 Characters	2 Digit ASCII Characters
62222	FLI 7 Characters	2 Digit ASCII Characters
62223	FLI 7 Characters	2 Digit ASCII Characters
62224	FLI 7 Leftmost 2 Characters	2 Digit ASCII Characters
62225	FLI 8 Rightmost 2 Characters	2 Digit ASCII Characters
62226	FLI 8 Characters	2 Digit ASCII Characters
62227	FLI 8 Characters	2 Digit ASCII Characters
62228	FLI 8 Leftmost 2 Characters	2 Digit ASCII Characters
62229	FLI 9 Rightmost 2 Characters	2 Digit ASCII Characters
62230	FLI 9 Characters	2 Digit ASCII Characters
62231	FLI 9 Characters	2 Digit ASCII Characters
62232	FLI 9 Leftmost 2 Characters	2 Digit ASCII Characters
62233	FLI 10 Rightmost 2 Characters	2 Digit ASCII Characters
62234	FLI 10 Characters	2 Digit ASCII Characters
62235	FLI 10 Characters	2 Digit ASCII Characters
62236	FLI 10 Leftmost 2 Characters	2 Digit ASCII Characters
62237	FLI 11 Rightmost 2 Characters	2 Digit ASCII Characters
62238	FLI 11 Characters	2 Digit ASCII Characters
62239	FLI 11 Characters	2 Digit ASCII Characters
62240	FLI 11 Leftmost 2 Characters	2 Digit ASCII Characters
62241	FLI 12 Rightmost 2 Characters	2 Digit ASCII Characters
62242	FLI 12 Characters	2 Digit ASCII Characters
62243	FLI 12 Characters	2 Digit ASCII Characters
62244	FLI 12 Leftmost 2 Characters	2 Digit ASCII Characters
62245	FLI 13 Rightmost 2 Characters	2 Digit ASCII Characters
62246	FLI 13 Characters	2 Digit ASCII Characters
62247	FLI 13 Characters	2 Digit ASCII Characters
62248	FLI 13 Leftmost 2 Characters	2 Digit ASCII Characters
62249	FLI 14 Rightmost 2 Characters	2 Digit ASCII Characters
62250	FLI 14 Characters	2 Digit ASCII Characters
62251	FLI 14 Characters	2 Digit ASCII Characters
62252	FLI 14 Leftmost 2 Characters	2 Digit ASCII Characters
62253	FLI 15 Rightmost 2 Characters	2 Digit ASCII Characters
62254	FLI 15 Characters	2 Digit ASCII Characters
62255	FLI 15 Characters	2 Digit ASCII Characters
62256	FLI 15 Leftmost 2 Characters	2 Digit ASCII Characters
62257	FLI 16 Rightmost 2 Characters	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
62258	FLI 16 Characters	2 Digit ASCII Characters
62259	FLI 16 Characters	2 Digit ASCII Characters
62260	FLI 16 Leftmost 2 Characters	2 Digit ASCII Characters
62261	FLI 17 Rightmost 2 Characters	2 Digit ASCII Characters
62262	FLI 17 Characters	2 Digit ASCII Characters
62263	FLI 17 Characters	2 Digit ASCII Characters
62264	FLI 17 Leftmost 2 Characters	2 Digit ASCII Characters
62265	FLI 18 Rightmost 2 Characters	2 Digit ASCII Characters
62266	FLI 18 Characters	2 Digit ASCII Characters
62267	FLI 18 Characters	2 Digit ASCII Characters
62268	FLI 18 Leftmost 2 Characters	2 Digit ASCII Characters
62269	FLI 19 Rightmost 2 Characters	2 Digit ASCII Characters
62270	FLI 19 Characters	2 Digit ASCII Characters
62271	FLI 19 Characters	2 Digit ASCII Characters
62272	FLI 19 Leftmost 2 Characters	2 Digit ASCII Characters
62273	FLI 20 Rightmost 2 Characters	2 Digit ASCII Characters
62274	FLI 20 Characters	2 Digit ASCII Characters
62275	FLI 20 Characters	2 Digit ASCII Characters
62276	FLI 20 Leftmost 2 Characters	2 Digit ASCII Characters
62277	FLI 21 Rightmost 2 Characters	2 Digit ASCII Characters
62278	FLI 21 Characters	2 Digit ASCII Characters
62279	FLI 21 Characters	2 Digit ASCII Characters
62280	FLI 21 Leftmost 2 Characters	2 Digit ASCII Characters
62281	FLI 22 Rightmost 2 Characters	2 Digit ASCII Characters
62282	FLI 22 Characters	2 Digit ASCII Characters
62283	FLI 22 Characters	2 Digit ASCII Characters
62284	FLI 22 Leftmost 2 Characters	2 Digit ASCII Characters
62285	FLI 23 Rightmost 2 Characters	2 Digit ASCII Characters
62286	FLI 23 Characters	2 Digit ASCII Characters
62287	FLI 23 Characters	2 Digit ASCII Characters
62288	FLI 23 Leftmost 2 Characters	2 Digit ASCII Characters
62289	FLI 24 Rightmost 2 Characters	2 Digit ASCII Characters
62290	FLI 24 Characters	2 Digit ASCII Characters
62291	FLI 24 Characters	2 Digit ASCII Characters
62292	FLI 24 Leftmost 2 Characters	2 Digit ASCII Characters
62293	FLI 25 Rightmost 2 Characters	2 Digit ASCII Characters
62294	FLI 25 Characters	2 Digit ASCII Characters
62295	FLI 25 Characters	2 Digit ASCII Characters
62296	FLI 25 Leftmost 2 Characters	2 Digit ASCII Characters
62297	FLI 26 Rightmost 2 Characters	2 Digit ASCII Characters
62298	FLI 26 Characters	2 Digit ASCII Characters
62299	FLI 26 Characters	2 Digit ASCII Characters
62300	FLI 26 Leftmost 2 Characters	2 Digit ASCII Characters
62301	FLI 27 Rightmost 2 Characters	2 Digit ASCII Characters
62302	FLI 27 Characters	2 Digit ASCII Characters
62303	FLI 27 Characters	2 Digit ASCII Characters
62304	FLI 27 Leftmost 2 Characters	2 Digit ASCII Characters
62305	FLI 28 Rightmost 2 Characters	2 Digit ASCII Characters
62306	FLI 28 Characters	2 Digit ASCII Characters
62307	FLI 28 Characters	2 Digit ASCII Characters
62308	FLI 28 Leftmost 2 Characters	2 Digit ASCII Characters
62309	FLI 29 Rightmost 2 Characters	2 Digit ASCII Characters
62310	FLI 29 Characters	2 Digit ASCII Characters

Register Address	ITEM	DESCRIPTION
62311	FLI 29 Characters	2 Digit ASCII Characters
62312	FLI 29 Leftmost 2 Characters	2 Digit ASCII Characters
62313	FLI 30 Rightmost 2 Characters	2 Digit ASCII Characters
62314	FLI 30 Characters	2 Digit ASCII Characters
62315	FLI 30 Characters	2 Digit ASCII Characters
62316	FLI 30 Leftmost 2 Characters	2 Digit ASCII Characters
62317	FLI 31 Rightmost 2 Characters	2 Digit ASCII Characters
62318	FLI 31 Characters	2 Digit ASCII Characters
62319	FLI 31 Characters	2 Digit ASCII Characters
62320	FLI 31 Leftmost 2 Characters	2 Digit ASCII Characters
62321	FLI 32 Rightmost 2 Characters	2 Digit ASCII Characters
62322	FLI 32 Characters	2 Digit ASCII Characters
62323	FLI 32 Characters	2 Digit ASCII Characters
62324	FLI 32 Leftmost 2 Characters	2 Digit ASCII Characters

Modbus Plus Global Register Mapping (37 Registers Defined) DPU2000R Only

Modbus Plus has the unique protocol characteristic that up to 32 registers of data may be attached to the token and seen by all the nodes on the Modbus Plus Network. The register configuration can be done through ECP or WinECP or via Modbus Plus. Global Mapping requires that the Modbus/Modbus Plus DPU2000 Register Address from 40001 through 40921 (The read only defined registers) may be mapped to the Global Register Mapping Table. The leading 4X is deleted from the required register mapped to the block. An example is shown in Figure 12-6. The register definitions for configuring Global Data are shown in Table 12-20.

Additionally, a security mask configuration register has been included within the configuration block. If the bit of Register 62598 assigned to the function is set to a 0. Then a password must be used when controlling a function in Groups 1 through Groups 6 as described in Section 11. The status of control being password protected/unprotected is indicated in Register 41153. If a password section is unprotected, then the password requested in Groups 1 through 6 may be any arbitrary value corresponding to the bit state.

If one were to configure the global registers via ECP or WinECP, a configuration screen is available to parameterize each of the 32 global Modbus Plus registers. An example of the global register configuration screen is shown in Figures 12-6 through 12-8. If a Modbus Plus DPU2000R capable relay was configured (Model # 587XXXX6- XXXX4 or 587XXXX7-XXXX4), the following screen would be shown on WinECP. Note the Global Register Tab (accessed from the “SETTINGS” Menu header) is visible and available as an option.

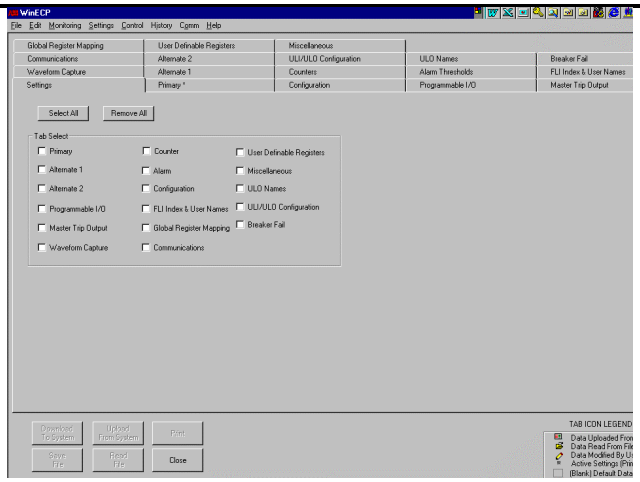


Figure 12-6. Setting Tab Display Screen with Modbus Plus Global Register Configuration Option

Depressing the Global Register Configuration tab allows the screen shown in Figure 12-7 to be visible. The Global Register Access screen and the Write Control Block (which is Register 41153, reference the section DPU Control Functionality for a complete description). Depress the Set Global Registers pushbutton to access the register configuration screen.

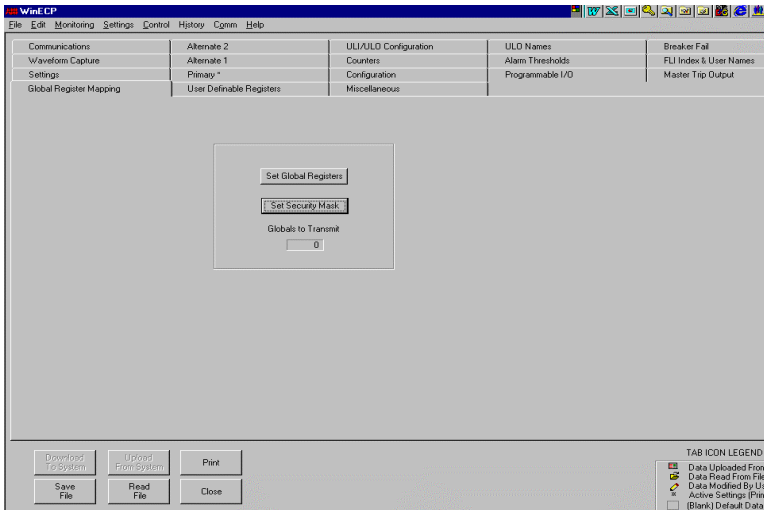


Figure 12-7. Global Register Configuration Option Screen

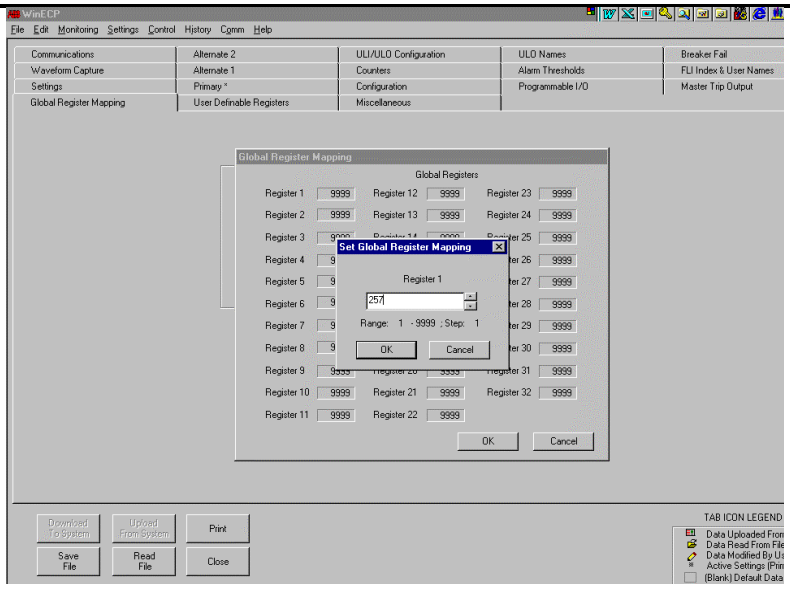


Figure 12-8. Global Register Configuration Screen

The screen shown in Figure 12-8 is visible once the Set Global Register Screen is depressed. Double clicking the area over the register assignment field then allows the sub "window" to be visible. In this example, Ia (Phase A Current Register 257) is mapped to Global Register 1. The register address is found by referencing Table 12-21 of this document.

Table 12-21. Modbus Plus Global Register Map Configuration Definition

Register Address	Item	Description
62560	SPARE_1	
62561	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
62562	Access Password	ASCII – 2 Characters Leftmost Digits
62563	Access Password	ASCII – 2 Characters Rightmost Digits
62564	SPARE_2	
62565	Number of Global Register To Transmit	Unsigned Integer 16 Bits 0<=Range<=32
62566	Modbus Plus Global Register 1 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62567	Modbus Plus Global Register 2 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62568	Modbus Plus Global Register 3 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62569	Modbus Plus Global Register 4 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62570	Modbus Plus Global Register 5 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62571	Modbus Plus Global Register 6 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62572	Modbus Plus Global Register 7 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62573	Modbus Plus Global Register 8 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62574	Modbus Plus Global Register 9 Mapped	Unsigned Integer 16 Bits

	Address	1<=Range<=921
62575	Modbus Plus Global Register 10 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62576	Modbus Plus Global Register 11 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62577	Modbus Plus Global Register 12 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62578	Modbus Plus Global Register 13 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62579	Modbus Plus Global Register 14 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62580	Modbus Plus Global Register 15 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62581	Modbus Plus Global Register 16 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62582	Modbus Plus Global Register 17 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62583	Modbus Plus Global Register 18 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62584	Modbus Plus Global Register 19 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62585	Modbus Plus Global Register 20 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62586	Modbus Plus Global Register 21 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62587	Modbus Plus Global Register 22 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62588	Modbus Plus Global Register 23 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62589	Modbus Plus Global Register 24 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62590	Modbus Plus Global Register 25 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62591	Modbus Plus Global Register 26 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62592	Modbus Plus Global Register 27 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62593	Modbus Plus Global Register 28 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62594	Modbus Plus Global Register 29 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62595	Modbus Plus Global Register 30 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62596	Modbus Plus Global Register 31 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62597	Modbus Plus Global Register 32 Mapped Address	Unsigned Integer 16 Bits 1<=Range<=921
62598	Security Mask For Control Block (See Section 11) Bit 0 (Rightmost Bit) Initiate Input Bit 1 Force Physical Input Bit 2 Force Physical Output Bit 3 Force Logical Output Bit 4 Set/Reset Output Bit 5 Pulse Outputs Bit 6 Reserved Bit 7 Reserved	Unsigned Integer 16 Bits 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. Reserved Reserved

	Bit 8 Reserved	Reserved
	Bit 9 Reserved	Reserved
	Bit 10 Reserved	Reserved
	Bit 11 Reserved	Reserved
	Bit 12 Reserved	Reserved
	Bit 13 Reserved	Reserved
	Bit 14 Reserved	Reserved
	Bit 15 Reserved	Reserved

User Definable Register Configuration Block

As described in Section 11, the DPU2000 and DPU1500R/2000R has the capability to scale and remap the Modbus registers within the unit. As shown in Table 12-11.

The following registers support modification and scaling of information contained in the Modbus user register set. The information in the 4xxxx registers can be tailored to the users needs with the following options:

1. Register: Register needed can be programmed.
2. Scalability: Data in the registers can be scaled.
3. Destination register data type: This supports multiple data types to match the destination systems needs.
4. Destination register data size: This supports multiple data sizes to match the destination systems needs.
5. MSB/LSB bit justification: This allows users to shift the bits contained in the 4xxxx Register into the *Most* significant bits or the *Least* significant bits.

Here is an example of how to set up the Modbus/Modbus Plus/DNP 3.0 Registers to exploit the above facilities. Consider a situation where the destination system is a SCADA. Suppose the user's SCADA system is setup to read the System Frequency on Register 40001 and requires the data be in the 12 Most significant bits. Also, let us suppose that the scale required on the system frequency is hex 0a (10 decimal) and the SCADA stores the value in a bipolar data type. The user would adopt the following procedure to setup Register 40001 to meet the specifications of the destination system. Now write hex 0a (decimal 10) which is the scale we need into Register 62693. Next write hex 0147 (327 decimal) on Register 62694 which fetches the value from the Register 40327 (the source register for system frequency). Setting the data size (12), the data type (bipolar) and shifting data (into Most significant bits) is done as follows:

Register Size (12 bits)

Bit 7	Bit 6	Bit 5	Bit 4
0	0	1	1

MSB/LSB (Justified to the left i.e. data in the the Most Significant Bits)

Bit 3
1

Register Type (Bipolar)

Bit 2	Bit 1	Bit 0
0	0	1

So, write hex 039 (decimal 57) into Register 62695 and the registers should look like:

Register 62692 hex 0000
Register 62693 hex 000a
Register 62694 hex 0147
Register 62695 hex 0039

Now when the command is executed, the data is transferred to the DPU2000/2000R and subsequent data transmissions from Register 40001 of the unit will be

- 12 bit wide with the bits justified to the left (in the Most Significant Bits)
- The data type will be bipolar and compatible with the destination register type
- The value will be scaled by 10

Table 12-22. User Definable Register Configuration Table

Register Address	Item	Description
62688	SPARE_1	
62689	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
62690	Access Password	ASCII – 2 Characters Leftmost Digits
62691	Access Password	ASCII – 2 Characters Rightmost Digits
62692	SPARE_2	
62693	User Reg. 40001 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62694	User Reg. 40001 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62695	User Reg. 40001 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62696	User Register 40001 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62697	User Reg. 40002 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62698	User Reg. 40002 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62699	User Reg. 40002 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits

Register Address	Item	Description
		0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62700	User Register 40002 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62701	User Reg. 40003 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62702	User Reg. 40003 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62703	User Reg. 40003 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62704	User Register 40003 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62705	User Reg. 40004 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62706	User Reg. 40004 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62707	User Reg. 40004 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62708	User Register 40004 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal

Register Address	Item	Description
	Data Type (Rightmost Byte)	1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62709	User Reg. 40005 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62710	User Reg. 40005 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62711	User Reg. 40005 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62712	User Register 40005 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4= Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62713	User Reg. 40006 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62714	User Reg. 40006 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62715	User Reg. 40006 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62716	User Register 40006 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage

Register Address	Item	Description
	Data Type (Rightmost Byte)	5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62717	User Reg. 40007 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62718	User Reg. 40007 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62719	User Reg. 40007 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62720	User Register 40007 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62721	User Reg. 40008 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62722	User Reg. 40008 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62723	User Reg. 40008 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62724	User Register 40008 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits

Register Address	Item	Description
		3 = Signed 32 Bits
62725	User Reg. 40009 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62726	User Reg. 40009 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62727	User Reg. 40009 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1= Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62728	User Register 40009 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62729	User Reg. 40010 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62730	User Reg. 40010 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62731	User Reg. 40010 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62732	User Register 40010 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62733	User Reg. 40011 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62734	User Reg. 40011 Source Register Address	Unsigned Integer 16 Bits

Register Address	Item	Description
		1<=Range<=922
62735	User Reg. 40011 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1= Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62736	User Register 40011 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62737	User Reg. 40012 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62738	User Reg. 40012 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62739	User Reg. 40012 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62740	User Register 40012 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62741	User Reg. 40013 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62742	User Reg. 40013 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62743	User Reg. 40013 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar

Register Address	Item	Description
		0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62744	User Register 40013 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62745	User Reg. 40014 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62746	User Reg. 40014 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62747	User Reg. 40014 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62748	User Register 40014 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62749	User Reg. 40015 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62750	User Reg. 40015 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62751	User Reg. 40015 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3) **Destination Scale Bit Size**	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits

Register Address	Item	Description
	Bits 7 – 6- 5- 4	0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62752	User Register 40015 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62753	User Reg. 40016 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62754	User Reg. 40016 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62755	User Reg. 40016 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62756	User Register 40016 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62757	User Reg. 40017 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62758	User Reg. 40017 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62759	User Reg. 40017 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits

Register Address	Item	Description
62760	User Register 40017 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62761	User Reg. 40018 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62762	User Reg. 40018 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62763	User Reg. 40018 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62764	User Register 40018 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62765	User Reg. 40019 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62766	User Reg. 40019 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62767	User Reg. 40019 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62768	User Register 40019 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current

Register Address	Item	Description
		3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62769	User Reg. 40020 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62770	User Reg. 40020 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62771	User Reg. 40020 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62772	User Register 40020 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62773	User Reg. 40021 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62774	User Reg. 40021 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62775	User Reg. 40021 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62776	User Register 40021 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits

Register Address	Item	Description
		1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62777	User Reg. 40022 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62778	User Reg. 40022 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62779	User Reg. 40022 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62780	User Register 40022 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62781	User Reg. 40023 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62782	User Reg. 40023 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62783	User Reg. 40023 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62784	User Register 40023 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62785	User Reg. 40024 Scale	Unsigned Integer 16 Bits

Register Address	Item	Description
		0<=Range<=65535
62786	User Reg. 40024 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62787	User Reg. 40024 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62788	User Register 40024 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62789	User Reg. 40025 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62790	User Reg. 40025 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62791	User Reg. 40025 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62792	User Register 40025 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62793	User Reg. 40026 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62794	User Reg. 40026 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62795	User Reg. 40026 Register **Destination Type**	Unsigned Integer 16 Bits

Register Address	Item	Description
	Rightmost Bits 2 – 1- 0	0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1= Negative Unipolar
	Destination Justification (Bit 3)	1 = Least Significant Bit 0 = Most Significant Bit
	Destination Scale Bit Size Bits 7 – 6- 5- 4	0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62796	User Register 40026 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62797	User Reg. 40027 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62798	User Reg. 40027 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62799	User Reg. 40027 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar
	Destination Justification (Bit 3)	1 = Least Significant Bit 0 = Most Significant Bit
	Destination Scale Bit Size Bits 7 – 6- 5- 4	0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62800	User Register 40027 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power
	Data Type (Rightmost Byte)	0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62801	User Reg. 40028 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62802	User Reg. 40028 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62803	User Reg. 40028 Register **Destination Type** Rightmost Bits 2 – 1- 0	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar

Register Address	Item	Description
	Destination Justification (Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62804	User Register 40028 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62805	User Reg. 40029 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62806	User Reg. 40029 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62807	User Reg. 40029 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62808	User Register 40029 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62809	User Reg. 40030 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62810	User Reg. 40030 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62811	User Reg. 40030 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits

Register Address	Item	Description
		0 1 0 0 =12 Bits 1 0 0 0 = 16 Bits
62812	User Register 40030 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 =Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62813	User Reg. 40031 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62814	User Reg. 40031 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62815	User Reg. 40031 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62816	User Register 40031 Source Register **Scale Type (Leftmost Byte)** **Data Type (Rightmost Byte)**	Unsigned Integer 16 Bits 0 = Normal 1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits
62817	User Reg. 40032 Scale	Unsigned Integer 16 Bits 0<=Range<=65535
62818	User Reg. 40032 Source Register Address	Unsigned Integer 16 Bits 1<=Range<=922
62819	User Reg. 40032 Register **Destination Type** Rightmost Bits 2 – 1- 0 **Destination Justification (**Bit 3) **Destination Scale Bit Size** Bits 7 – 6- 5- 4	Unsigned Integer 16 Bits 0 0 0 = Offset Bipolar 0 0 1 = Bipolar 0 1 0 = Unipolar 0 1 1 = Negative Unipolar 1 = Least Significant Bit 0 = Most Significant Bit 0 0 0 0 = 2 Bits 0 0 0 1 = 4 Bits 0 0 1 0 = 8 Bits 0 1 0 0 = 12 Bits 1 0 0 0 = 16 Bits
62820	User Register 40032 Source Register **Scale Type (Leftmost Byte)**	Unsigned Integer 16 Bits 0 = Normal

Register Address	Item	Description
	Data Type (Rightmost Byte)	1 = Remainder 2 = Phase Current 3 = Neutral Current 4 = Voltage 5 = Power 0 = Unsigned 16 Bits 1 = Unsigned 32 Bits 2 = Signed 16 Bits 3 = Signed 32 Bits

Miscellaneous Settings

The DPU2000 and DPU1500R/2000R, depending upon model numbers selected with the Front Panel Interface, has the ability to send alphanumeric messages on the front panel display. The Front Panel Interface may display up to four lines of text with 20 ASCII characters per line. (Please Refer to Appendix B for the ASCII conversion chart). A host device may send the display message to the front panel display to actuate a message which may be displayed to alert an operator of a pending message.

Since the DPU2000 does not have a Modbus Plus interface, an additional register is available for enabling or disabling password protection. Register 62949 is a Security mask duplicate of Register 62598. Table 12-23 lists the register definition for each setting.

Table 12-23. Miscellaneous Settings Map Configuration Definition

Register Address	Item	Description
62944	SPARE_1	
62945	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits
62946	Access Password	ASCII – 2 Characters Leftmost Digits
62947	Access Password	ASCII – 2 Characters Rightmost Digits
62948	SPARE_2	
62949	Security Mask For Control Block (See Section 11) Bit 0 (Rightmost Bit) Initiate Input Bit 1 Force Physical Input Bit 2 Force Physical Output Bit 3 Force Logical Output Bit 4 Set/Reset Output Bit 5 Pulse Outputs Bit 6 Reserved Bit 7 Reserved Bit 8 Reserved Bit 9 Reserved Bit 10 Reserved Bit 11 Reserved Bit 12 Reserved Bit 13 Reserved Bit 14 Reserved Bit 15 Reserved	Unsigned Integer 16 Bits 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. 1= Control Unprotected, 0 = Password Req. Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
62950	FPI Display Message Line 1 Character 1/ Character 2	ASCII - 2 Characters
62951	FPI Display Message Line 1 Character 3/ Character 4	ASCII - 2 Characters

62952	FPI Display Message Line 1 Character 5/ Character 6	ASCII - 2 Characters
62953	FPI Display Message Line 1 Character 7/ Character 8	ASCII - 2 Characters
62954	FPI Display Message Line 1 Character 9/ Character 10	ASCII - 2 Characters
62955	FPI Display Message Line 1 Character 11/ Character 12	ASCII - 2 Characters
62956	FPI Display Message Line 1 Character 13/ Character 14	ASCII - 2 Characters
62957	FPI Display Message Line 1 Character 15/ Character 16	ASCII - 2 Characters
62958	FPI Display Message Line 1 Character 17/ Character 18	ASCII - 2 Characters
62959	FPI Display Message Line 1 Character 19/ Character 20	ASCII - 2 Characters
62960	FPI Display Message Line 2 Character 1/ Character 2	ASCII - 2 Characters
62961	FPI Display Message Line 2 Character 3/ Character 4	ASCII - 2 Characters
62962	FPI Display Message Line 2 Character 5/ Character 6	ASCII - 2 Characters
62963	FPI Display Message Line 2 Character 7/ Character 8	ASCII - 2 Characters
62964	FPI Display Message Line 2 Character 9/ Character 10	ASCII - 2 Characters
62965	FPI Display Message Line 2 Character 11/ Character 12	ASCII - 2 Characters
62966	FPI Display Message Line 2 Character 13/ Character 14	ASCII - 2 Characters
62967	FPI Display Message Line 2 Character 15/ Character 16	ASCII - 2 Characters
62968	FPI Display Message Line 2 Character 17/ Character 18	ASCII - 2 Characters
62969	FPI Display Message Line 2 Character 19/ Character 20	ASCII - 2 Characters
62970	FPI Display Message Line 3 Character 1/ Character 2	ASCII - 2 Characters
62971	FPI Display Message Line 3 Character 3/ Character 4	ASCII - 2 Characters
62972	FPI Display Message Line 3 Character 5/ Character 6	ASCII - 2 Characters
62973	FPI Display Message Line 3 Character 7/ Character 8	ASCII - 2 Characters
62974	FPI Display Message Line 3 Character 9/ Character 10	ASCII - 2 Characters
62975	FPI Display Message Line 3 Character 11/ Character 12	ASCII - 2 Characters
62976	FPI Display Message Line 3 Character 13/ Character 14	ASCII - 2 Characters
62977	FPI Display Message Line 3 Character 15/ Character 16	ASCII - 2 Characters
62978	FPI Display Message Line 3 Character 17/ Character 18	ASCII - 2 Characters
62979	FPI Display Message Line 3 Character 19/ Character 20	ASCII - 2 Characters
62980	FPI Display Message Line 4 Character 1/	ASCII - 2 Characters

	Character 2	
62981	FPI Display Message Line 4 Character 3/ Character 4	ASCII - 2 Characters
62982	FPI Display Message Line 4 Character 5/ Character 6	ASCII - 2 Characters
62983	FPI Display Message Line 4 Character 7/ Character 8	ASCII - 2 Characters
62984	FPI Display Message Line 4 Character 9/ Character 10	ASCII - 2 Characters
62985	FPI Display Message Line 4 Character 11/ Character 12	ASCII - 2 Characters
62986	FPI Display Message Line 4 Character 13/ Character 14	ASCII - 2 Characters
62987	FPI Display Message Line 4 Character 15/ Character 16	ASCII - 2 Characters
62988	FPI Display Message Line 4 Character 17/ Character 18	ASCII - 2 Characters
62989	FPI Display Message Line 4 Character 19/ Character 20	ASCII - 2 Characters
	Communication Configurable Settings Area	

Oscillographic Data Storage

The DPU 2000R has two versions of Ocsillographics, Standard and Enhanced. The differentiation of the two storage methods is described below. The Standard Oscillographic option only captured 1 to 8 oscillographic records of set length and set parameters for capture. Standard Oscillographics is available on Version 1.5 DPU Firmware Version to Version 4.5 Firmware Version.

The Enhanced Oscillogrpahics captures multiple records depending upon the configuration of the IED and the amount of available memory in the device. Enhanced Oscillographics is available in Version 5.0 DPU 2000R Version 5.0 or greater Firmware Version.

The method to access the data and the construction of the waveform to the standard accepted file formats is the same for the STANDARD and ENHANCED OSCILLOGRAPHICS CAPABILITIES.

STANDARD OSCILLOGRAPHICS(Version 1.5 and Greater DPU2000R Only)

The DPU2000R has the capability of accepting an option of Oscillographics (Part Number 587 XXXXX – X1XXX [X = Don't Care]). The total storage buffer capacity for the DPU2000R is 64 cycles of waveform data, which consists of four input currents (one per phase and neutral), and three input voltages. A user may configure the DPU2000R to capture a single or multiple events of waveform capture. One may think of the waveform capture buffer as depicted in Figure 12-9.

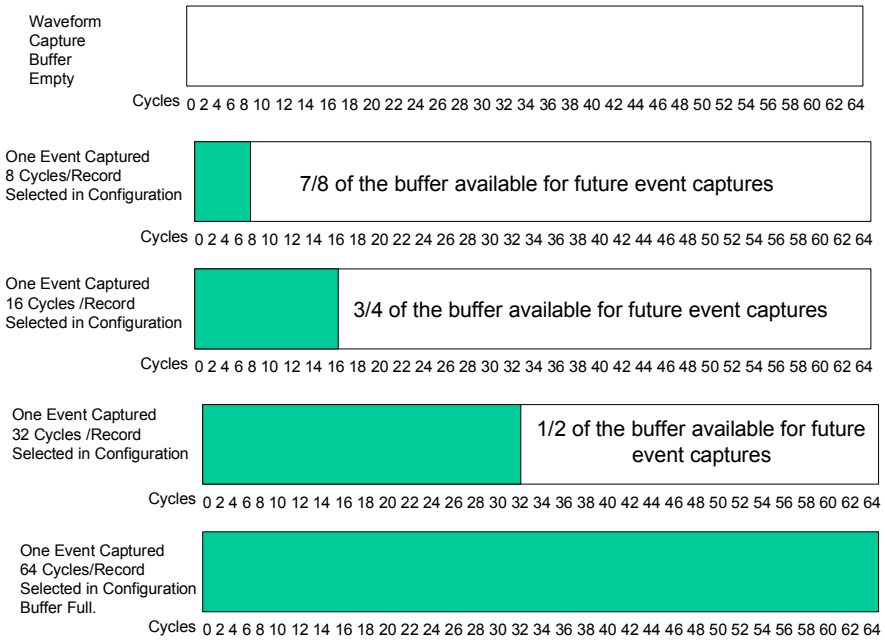


Figure 12-9. Waveform Capture Buffer Options

The DPU2000R may be configured to capture eight, four, two or one record(s) containing 8, 16, 32, or 64 cycles of data. Several data elements are stored in each waveform record. Such information as the individual quantity for each of the voltage/current phases, breaker 52a/b state, time-stamping information, and state of the protective function is retrievable via Modbus and Modbus Plus.

Oscillographic data contains two elements of particular interest to the Automation Specialist. One element is the configuration of the oscillographic component as to when to acquire the data. The other element is retrieval of the wave form functions and the understanding of how to interpret the data for display purposes.

ENHANCED OSCILLOGRAPHICS (VERSION 5.0 AND GREATER)

Enhanced OSCILLOGRAPHICS allows the operator to select the amount of pre-trigger and post Trigger cycles to be recorded. The amount of storeage is determined by the total memory unit size, which for the sake of calculations is equal to 5000.

The formula to determine the amount of memory is available to store additional waveforms is:

Waveform capture rules:

Record Size = 1 + number of channels + (number of channels * number of cycles) + number of cycles

Number of Records = Total Units / Records Size

Total Units 5000 = (340,000 / 68)

Oscillographic Configuration (12 Registers Defined)

One can configure the DPU2000R to capture pre-fault and post fault snapshots of data. The trigger to capture the data may be of the master trip element, breaker position, hard wired contact (Waveform Capture Initiate Element) or if any of the 20 defined protective elements are energized. The control and status block is defined in 6X Registers 63072 through 63199. The 6X file number for storage/retrieval of this data is in FILE 1 of the protocol.

Figure 12-10 illustrates the method to configure the oscillographics over Modbus or Modbus Plus. The host may retrieve the data via the 6X memory read command by first writing a value of "2" to the first memory location of the Oscillographic data block. The control register is defined as 63072. The registers from 63074 and 63075 should also be written with the appropriate unit password to effectuate the transfer of data from the DPU2000R to the Modbus Memory Map. The configuration data will then be transferred from the DPU2000R to the 6X Registers reflecting the state of the Oscillographic configuration.

It should be remembered that some hosts are not capable of 6X Register access. Parameterization of the Oscillographic Data Capture may be accomplished from the WinECP (Windows External Communication Program) utility.

The definition of several key parameters must be understood in order to configure the waveform capture (Oscillographic) capabilities of the relay. The relay must not be parameterized (or re-parameterized) while the relay is monitoring the waveform for capture. Register 63076 controls the start/stop capabilities of this feature.

Register 63077 controls the storage capacity within the waveform capture buffer as shown in Figure 12-9. For example, if a value of 0 is selected, Eight records of data can be captured and stored by the DPU2000R upon the trigger action as defined in Registers 63080 through 63084. If the value of 3 is selected, a single record of data is captured, filling the entire buffer. The data captured for each channel consists of 8 samples per quarter cycle per channel (each of the eight channels are Ia, Ib, Ic, In, Va, Vb, and Vc). Table 12-24 explains the resolution of the capture. The 6X Register Definition is included in Table 12-25.

Register 63078 configures the DPU2000R Trigger Mode. If Normal Mode (Value = 0) is selected, the trigger will allow waveform capture until capture is terminated by the host. If the buffer is full, the waveform will roll over and overwrite the first record in the buffer. If Single Shot (Value = 1) is selected, oscillographic capture monitoring will be terminated upon recording of the single event record.

Append Mode is a mode in which each individual bit of the Trigger Register 63080 – 63083 is evaluated. If one of the programmed trigger bits is active, the oscillographic data is stored. If during that time a second trigger bit is active, a second record shall be recorded and stored. If the Normal/Append (Value =3) Mode function is selected, the oscillographic function will continue at the end of waveform capture. If the buffer is full, then the next record will overwrite that record at the beginning of the buffer. If the Single Shot/Append Mode is selected, then the oscillographic function will terminate at the end of recording for that record.

Table 12-24. Oscillographic Resolution Capabilities STANDARD OSCILLOGRAPHICS

Register 63077 Selection	Description
0 = 8 Cycles per record – 8 Records	8 Records of Data Capture possible with 8 Cycles of Waveform Captured @ 32 Samples per cycle per channel.
1 = 16 Cycles per record – 4 Records	4 Records of Data Capture possible with 16 Cycles of Waveform Captured @ 32 Samples per cycle per channel.
2 = 32 Cycles per record – 2 Records	2 Records of Data Capture possible with 32 Cycles of Waveform Captured @ 32 Samples per cycle per channel.
3 = 64 Cycles per record – 1 Record	1 Record of Data available with 64 Cycles of Waveform Captured @ 32 Samples per cycle per channel.

Table 12-25. Oscillographic Configuration Registers STANDARD OSCILLOGRAPHICS

Register	Item	Description
63072	Execute Register	Unsigned Integer 16 Bits 0 = No Action 1 = Transfer Settings 2 = Retrieve Settings
63073	Access PASSWORD	2 Leftmost Digits ASCII
63074	Access PASSWORD	2 Rightmost Digits ASCII
63075	Reserved	Reserved
63076	Start/Stop Accumulation	Unsigned Integer 16 Bits 0 = Stop 1 = Start
63077	Acquisition Format	Unsigned Integer 16 Bits

Register	Item	Description
		0 = 8 Records Max Storage/8 Cycles/Record 1 = 4 Records Max Storage/16 Cycles/Record 2 = 2 Records Max Storage/32 Cycles/Record 3 = 1 Record Stored/64 Cycles/Record
63078	Trigger Mode	Unsigned Integer 16 Bits 0 = Normal 1 = Single Shot 2 = Normal/Append Mode 3 = Single Shot/Append Mode
63079	Trigger Position	Unsigned Integer 16 Bits Number of quarter cycles to capture pre-fault. If 63077 = 0 : 0 <=Trigger<= 32 If 63077 = 1 : 0 <=Trigger<= 64 If 63077 = 2 : 0 <=Trigger<= 128 If 63077 = 3 : 0 <=Trigger<= 256
63080	Trigger Flag Reserved	Unsigned Integer 16 Bits Set to zero
63081	Trigger Flag Reserved	Unsigned Integer 16 Bits Set to 0
63082	Trigger Flag Bit 0 = Master Trip (lsb) Bit 1 = Breaker Open Bit 2 = WCI Bit 3 = Reserved Bit 4 = Reserved Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Unsigned Integer 16 Bits Start Capture on: Master Trip State Breaker Open Waveform Capture Initiate Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
63083	Trigger Flag Bit 0 = 50N-1 (lsb) Bit 1 = 50N-2 Bit 2 = 50N-3 Bit 3 = 51N Bit 4 = 50P-1 Bit 5 = 50P-2 Bit 6 = 50P-3 Bit 7 = 51P Bit 8 = 67P Bit 9 = 67N Bit 10 = 46 Bit 11 = 27 Bit 12 = 59 Bit 13 = 79V Bit 14 = 81S-1 Bit 15 = 81R –1 (msb)	Unsigned Integer 16 Bits Start Capture on: Neutral. Instantaneous Overcurrent Trip Neutral. Instantaneous Overcurrent Trip Neutral. Instantaneous Overcurrent Trip Neutral Time Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Time Overcurrent Trip Direct Overcurrent Trip Positive Sequence Direct Overcurrent Trip Negative Sequence Negative Sequence Overcurrent Trip Undervoltage Trip Overcurrent Trip Recloser Lockout Frequency Shed (1st Stage) Frequency Restore (1st Stage)
63084	Reserved	Reserved
63085- 63199	Reserved	Reserved

Oscillographic Configuration Registers STANDARD OSCILLOGRAPHICS

Register	Item	Description
63072	RESERVED	RESERVED
63073	Execute Register	Unsigned Integer 16 Bits 0 = No Action 1 = Transfer Settings 2 = Retrieve Settings
63074	Access PASSWORD	2 Leftmost Digits ASCII
63075	Access PASSWORD	2 Rightmost Digits ASCII
63076	Reserved	Reserved
63077	Start/Stop Accumulation	Unsigned Integer 16 Bits 0 = Stop 1 = Start
63078	Setup new Acquisition	Unsigned Integer 16 Bits 0 = Present Records will not be overwritten 1 = Present Records Will Be Overwritten
63079	Trigger Mode	Unsigned Integer 16 Bits 0 = Normal 1 = Single Shot
63080	Trigger Flag - RESERVED	Unsigned Integer 16 Bits
63081	Trigger Flag Bit 0 = Master Trip (lsb) Bit 1 = 52A Bit 2 = Breaker Fail Alarm Bit 3 = Pick UP Alarm Bit 4 = Digital Fault Rec Init. Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved (msb)	Unsigned Integer 16 Bits Start Capture on: Master Trip Breaker Contact STatus Breaker Fail Alarm Pick UP Alarm Digital Fault Recorder Initialte Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
63082	Trigger Flag Bit 0 = 50N-1 (lsb) Bit 1 = 50N-2 Bit 2 = 50N-3 Bit 3 = 50P-1 Bit 4 = 50P-2 Bit 5 = 50P-3 Bit 6 = 51N Bit 7 = 51P Bit 8 = 67P Bit 9 = 67N Bit 10 = 46 Bit 11 = 46A Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved (msb)	Unsigned Integer 16 Bits Start Capture on: Neutral. Instantaneous Overcurrent Trip Neutral. Instantaneous Overcurrent Trip Neutral. Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Neutral Time Overcurrent Trip Phase Time Overcurrent Trip Direct Overcurrent Trip Positive Sequence Direct Overcurrent Trip Negative Sequence Negative Sequence Overcurrent Trip Negative Sequence Overcurrent Trip Reserved Reserved Reserved Reserved
63083	Trigger Flag Bit 0 = 27 (lsb)	Unsigned Integer 16 Bits Start Capture on:

Register	Item	Description
	Bit 1 = 59 Bit 2 = 79V Bit 3 = 81S Bit 4 = 81R Bit 5 = Reserved Bit 6 = Reserved Bit 7 = 21-P1 Bit 8 = 21-P2 Bit 9 = 21-P3 Bit 10 = 21-P4 Bit 11 = 59G Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved	Single Phase Overvoltage Reclose Undervoltage Block Frequency Load Shed Trip Frequency Restore Reserved Reserved Phase Distance Element Zone 1 Phase Distance Element Zone 2 Phase Distance Element Zone 3 Phase Distance Element Zone 4 Ground Overvoltage Reserved Reserved Reserved Reserved
63084	Analog Channel Selected Bit 0 = Load A Current (lsb) Bit 1 = Load B Current Bit 2 = Load C Current Bit 3 = Load N Current Bit 4 = Voltage Phase A Bit 5 = Voltage Phase B Bit 6 = Voltage Phase C Bit 7 = Iload Bit 8 = V0 Bit 9 = Bus Voltage Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved(msb)	Unsigned Integer 16 Bits:
63085	Number of Pre Trigger Cycles to Be Recorded	Unsigned Integer 16 Bits:
63086	Number of Post Trigger Cycles to be Recoreded	Unsigned Integer 16 Bits:
63087-63199	Reserved	Reserved

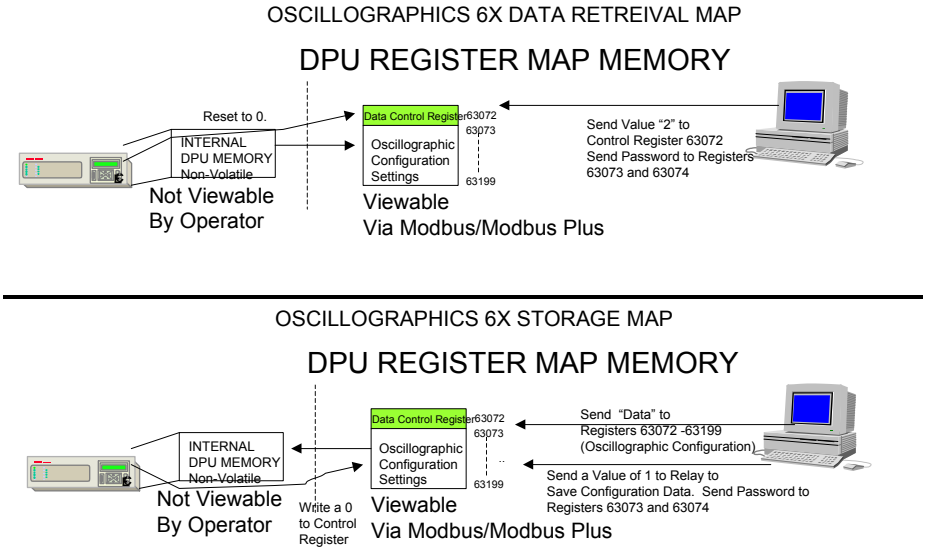


Figure 12-10. Oscillographics Retrieval/Storage Parameterization Philosophy

Whenever the relay is in the capture mode, the capture mode must be stopped to change setting information. Therefore, the following must be performed before changing settings:

1. Register 63072 should be written with a value of "2" to fill registers with the present configuration data within the DPU2000R. Registers 63073 and 63074 should contain the correct password to effectuate the "REFRESH REGISTER" command.
2. The oscillographic accumulation must be stopped to effectuate re-parameterization of the unit. A value of 0 must be written to Register 63076 to pause oscillographic monitoring.
3. The oscillographic data in the configuration block can be modified. To change the parameters, one would write the changed parameters to the appropriate registers as defined in Table 12-23.
4. The host would then write a value of "1" (Start Oscillographic Accumulation) to Register 63076.
5. The host would then write a value of "1" (Transfer Settings) to Register 63072 along with the appropriate password (Registers 63073 and 63074). The data would then be transferred from the Modbus volatile register memory to the DPU2000R's non-volatile configuration memory. This procedure is shown in Figure 12-9 above.

Oscillographic Data Retrieval

The DPU2000R has two steps which must be accomplished for Oscillographic Data Retrieval. Step 1 is that the Channel Data Parameters must be read from the DPU2000R. These parameters display the number of records in the Oscillographics buffer, Trigger Information, sample time stamps and point scaling information. The data is stored in a format in which the information is easily translated to a COMTRADE format.

The second step is the actual retrieval of the data point information used to construct the waveform. The data retrieved is in a Block of 56 Data Points. Register definition for this feature is given in Table 12-25.

Data Retrieval Theory of Operation

There are two sets of write registers required to obtain the captured waveforms, 41666 and 41793/41794.

Register 41666 controls the data constant retrieval for interpreting the point information of the individual points along the waveform curve. The registers in this define the parameters for the selected record. The method for access is described in Figure 12-11.

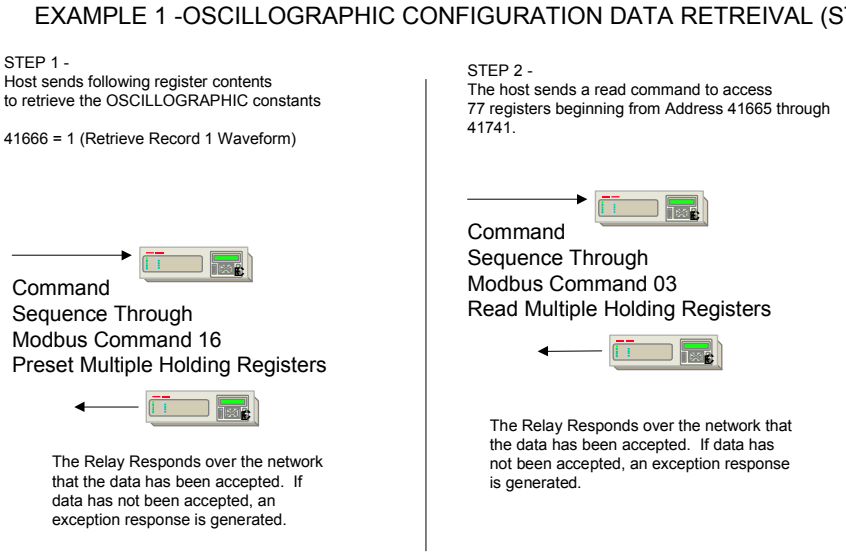


Figure 12-11. Configuration Data Retrieval Example

Register 41793 and 41794 control the method to obtain the individual points to construct the curve.

Each waveform consists of 32 points. The DPU2000R stores the waveform and transfers the data to the host in quarter cycle blocks. Thus, if 8 cycles are stored for a waveform Record, 32 blocks of data must be retrieved by the host to display the selected waveform record. Waveform data is to be read eight points per channel with eight channels per block.

The steps required to read the data are as such:

- Write the record number and quarter cycle block to access (Register 41794 = 1 for read first Quarter Cycle Block of Data). The DPU2000R shall reset the control register to 0.
- Read the block of point data.
- Write the Record Number and quarter cycle block to access (Register 41794 = 2 for read next Quarter Cycle Block of Data). The DPU2000R shall reset the control register to 0.
- Read the Block of point data.
- If Register 41796 is not equal to 0, repeat the previous two steps.

The process is illustrated pictorially in Figure 12-12.

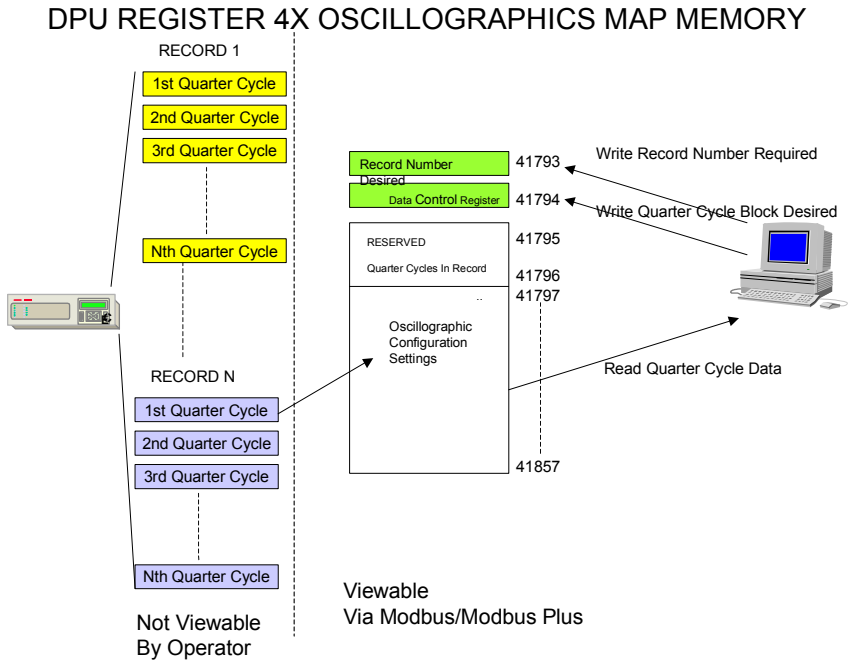


Figure 12-12. Memory Map Philosophy for Oscillographics Waveform Retrieval

Table 12-26. Oscillographic Data Format Retrieval Block

Register Address	Item	Description
CHANNEL DATA		
41665	READ DATA – Number of Records Stored	Unsigned Integer (16 Bits) Amount of Data Records in Buffer (Value = 0 - 8)
41666	WRITE DATA- Record Desired to Retrieve	Unsigned Integer (16 Bits) (Value = 0 to 8)
41667	READ DATA –Trigger Flag Word 1 Reserved	Unsigned Integer (16 Bits) Reserved
41668	READ DATA – Trigger Flag Word 2 Reserved	Unsigned Integer (16 Bits) Reserved
41669	READ DATA – Trigger Flag Word 3 Bit 0 = Master Trip (lsb) Bit 1 = Breaker Open Bit 2 = WCI Bit 3 = Reserved Bit 4 = Reserved Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved (msb)	Unsigned Integer (16 Bits) Start Capture on Master Trip State Start Capture on Breaker Open Start Capture on Waveform Capture Initiate Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
41670	READ DATA – Trigger Flag Word 4 Bit 0 = 50N-1 (lsb) Bit 1 = 50N-2	Unsigned Integer (16 Bits) Neutral Instantaneous Overcurrent Trip Neutral Instantaneous Overcurrent Trip

Register Address	Item	Description
	Bit 2 = 50N-3	Neutral Instantaneous Overcurrent Trip
	Bit 3 = 51N	Neutral Time Overcurrent Trip
	Bit 4 = 50P-1	Phase Instantaneous Overcurrent Trip
	Bit 5 = 50P-2	Phase Instantaneous Overcurrent Trip
	Bit 6 = 50P-3	Phase Instantaneous Overcurrent Trip
	Bit 7 = 51P	Phase Time Overcurrent Trip
	Bit 8 = 67P	Direct Overcurrent Trip Positive Sequence
	Bit 9 = 67N	Direct Overcurrent Trip Negative Sequence
	Bit 10 = 46	Negative Sequence Overcurrent Trip
	Bit 11 = 27	Undervoltage Trip
	Bit 12 = 59	Overcurrent Trip
	Bit 13 = 79V	Recloser Lockout
	Bit 14 = 81S-1	Frequency Shed (1st Stage)
	Bit 15 = 81R-1 (msb)	Frequency Restore (1st Stage)
DATE/TIMESTAMPS OF TRIGGER POINT		
41671	Year	Unsigned Integer 16 Bits 0-99
41672	Month	Unsigned Integer 16 Bits 1- 12
41673	Day	Unsigned Integer 16 bits 1-31
41674	Hour	Unsigned Integer 16 Bits 0-23
41675	Minute	Unsigned Integer 16 Bits 0-59
41676	Second	Unsigned Integer 16 Bits 0-59
41677	Hundredths of Seconds	Unsigned Integer 16 Bits 0 – 99
41678	Quarter Cycle Trigger Point	Unsigned Integer 16 Bits Number of 1/4 Cycle of Trigger Point 0-255 (Dependent on 6X Register Config)
41679	Total Number of Channels	Unsigned Integer 16 Bits Default as 7
41680	Total Analog Data Channels	Unsigned Integer 16 Bits Fixed at 7
41681	Total Digital Data Channels	Unsigned Integer 16 Bits 0 <=Range <= 64
LINE FREQUENCY OF WAVEFORM		
41682	Line Frequency	Unsigned Integer 16 Bits 50 or 60 Hz
SAMPLE RATE INFORMATION		
41683	Reserved	Reserved
41684	Reserved	Reserved
41685	Reserved	Reserved
CHANNEL NAMES, UNITS, AND CONVERSIONS		
41686	Channel 1 – Channel Number	Unsigned Integer 16 Bits See Note 1
41687	Channel 1 – Channel Name	2 Digits ASCII
41688	Channel 1 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41689	Channel 1 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41690	Channel 1 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)

Register Address	Item	Description
41691	Channel 1 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41692	Channel 1 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41693	Channel 1 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41694	Channel 2 – Channel Number	Unsigned Integer 16 Bits See Note 1
41695	Channel 2 – Channel Name	2 Digits ASCII
41696	Channel 2 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41697	Channel 2 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41698	Channel 2 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41699	Channel 2 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41700	Channel 2 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41701	Channel 2 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41702	Channel 3 – Channel Number	Unsigned Integer 16 Bits See Note 1
41703	Channel 3 – Channel Name	2 Digits ASCII
41704	Channel 3 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41705	Channel 3 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41706	Channel 3 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41707	Channel 3 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41708	Channel 3 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41709	Channel 3 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41710	Channel 4 – Channel Number	Unsigned Integer 16 Bits See Note 1
41711	Channel 4 – Channel Name	2 Digits ASCII
41712	Channel 4 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41713	Channel 4 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41714	Channel 4 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41715	Channel 4 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41716	Channel 4 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41717	Channel 4 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41718	Channel 5 – Channel Number	Unsigned Integer 16 Bits See Note 1
41719	Channel 5 – Channel Name	2 Digits ASCII
41720	Channel 5 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41721	Channel 5 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41722	Channel 5 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41723	Channel 5 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41724	Channel 5 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41725	Channel 5 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41726	Channel 6 – Channel Number	Unsigned Integer 16 Bits See Note 1
41727	Channel 6– Channel Name	2 Digits ASCII

Register Address	Item	Description
41728	Channel 6 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41729	Channel 6 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41730	Channel 6 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41731	Channel 6 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41732	Channel 6 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41733	Channel 6 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41734	Channel 7 – Channel Number	Unsigned Integer 16 Bits See Note 1
41735	Channel 7 – Channel Name	2 Digits ASCII
41736	Channel 7 – Channel Phase Identification	Unsigned Integer 16 Bits See Note 1
41737	Channel 7 – Channel Units	Unsigned Integer 16 Bits 1 = Amps 2 = Volts
41738	Channel 7 – Scale Factor Numerator	Unsigned 32 Bit High Order Word (MSW)
41739	Channel 7 – Scale Factor Numerator	Unsigned 32 Bit Low Order Word (LSW)
41740	Channel 7 – Scale Factor Denominator	Unsigned 32 Bit High Order Word (MSW)
41741	Channel 7 – Scale Factor Denominator	Unsigned 32 Bit Low Order Word (MSW)
41742 through 41792 Reserved for future use.		
NOTE 1:The code for channel numbers/channel phase ID are as follows - 1 = Ia 2 = Ib 3 = Ic 4 = In 5 = Va 6 = Vb 7 = Vc		
OSCILLOGRAPHIC QUARTER CYCLE DATA POINTS		
41793	WRITE DATA Record Number Desired	Unsigned Integer 16 Bits 0<=Range <= 8 depending sample size
41794	WRITE DATA Control Register	Unsigned Integer 16 Bits 1 = First Quarter Cycle of Data 2 = Next Quarter Cycle of Data 3 = Previous Quarter Cycle of Data
41795	Reserved	Reserved
41796	Quarter Cycle Blocks Remaining to be read	Unsigned Integer 16 Bits 0 = None <= Range<= 255
41797	Quarter Cycle Fault Type Word 1 Reserved	Unsigned Integer 16 Bits Reserved
41798	Quarter Cycle Fault Type Word 2 Bit 0 = 50N-1 (lsb) Bit 1 = 50N-2 Bit 2 = 50N-3 Bit 3 = 51N Bit 4 = 50P-1 Bit 5 = 50P-2 Bit 6 = 50P-3 Bit 7 = 51P Bit 8 = 67P Bit 9 = 67N Bit 10 = 46 Bit 11 = 27	Unsigned Integer 16 Bits Neutral Instantaneous Overcurrent Trip Neutral Instantaneous Overcurrent Trip Neutral Instantaneous Overcurrent Trip Neutral Time Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Time Overcurrent Trip Direct Overcurrent Trip Positive Sequence Direct Overcurrent Trip Negative Sequence Negative Sequence Overcurrent Trip Undervoltage Trip

Register Address	Item	Description
	Bit 12 = 59 Bit 13 = 79V Bit 14 = 81S-1 Bit 15 = 81R-1 (msb)	Overcurrent Trip Recloser Lockout Frequency Shed (1st Stage) Frequency Restore (1st Stage)
41799	Quarter Cycle Pickup Type Word 1 Reserved	Unsigned Integer 16 Bit Reserved
41800	Quarter Cycle Pickup Type Word 2 Bit 0 = 50N-1 (lsb) Bit 1 = 50N-2 Bit 2 = 50N-3 Bit 3 = 51N Bit 4 = 50P-1 Bit 5 = 50P-2 Bit 6 = 50P-3 Bit 7 = 51P Bit 8 = 67P Bit 9 = 67N Bit 10 = 46 Bit 11 = 27 Bit 12 = 59 Bit 13 = 79V Bit 14 = 81S-1 Bit 15 = 81R-1 (msb)	Unsigned Integer 16 Bits Neutral Instantaneous Overcurrent Trip Neutral Instantaneous Overcurrent Trip Neutral Instantaneous Overcurrent Trip Neutral Time Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Instantaneous Overcurrent Trip Phase Time Overcurrent Trip Direct Overcurrent Trip Positive Sequence Direct Overcurrent Trip Negative Sequence Negative Sequence Overcurrent Trip Undervoltage Trip Overcurrent Trip Recloser Lockout Frequency Shed (1st Stage) Frequency Restore (1st Stage)
41801	Quarter Cycle Miscellaneous Data Word 1 Reserved	Unsigned Integer 16 Bits Reserved
41802	Quarter Cycle Miscellaneous Data Word 2 Bit 0 = Master Trip (lsb) Bit 1 = 52aa Bit 2 = BFA Bit 3 = Reserved Bit 4 = Reserved Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved Bit 8 = Reserved Bit 9 = Reserved Bit 10 = Reserved Bit 11 = Reserved Bit 12 = Reserved Bit 13 = Reserved Bit 14 = Reserved Bit 15 = Reserved (msb)	Unsigned Integer 16 Bits Master Trip Status Breaker Status (1 = Open, 0 = Closed) Breaker Fail Alarm Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved
OSCILLOGRAPHIC DATA POINTS		
41803	Channel 1 Point 1	Signed Integer 16 Bits
41804	Channel 2 Point 1	Signed Integer 16 Bits
41805	Channel 3 Point 1	Signed Integer 16 Bits
41806	Channel 4 Point 1	Signed Integer 16 Bits
41807	Channel 5 Point 1	Signed Integer 16 Bits
41808	Channel 6 Point 1	Signed Integer 16 Bits
41809	Channel 7 Point 1	Signed Integer 16 Bits
41810	Channel 1 Point 2	Signed Integer 16 Bits
41811	Channel 2 Point 2	Signed Integer 16 Bits
41812	Channel 3 Point 2	Signed Integer 16 Bits
41813	Channel 4 Point 2	Signed Integer 16 Bits
41814	Channel 5 Point 2	Signed Integer 16 Bits
41815	Channel 6 Point 2	Signed Integer 16 Bits

Register Address	Item	Description
41816	Channel 7 Point 2	Signed Integer 16 Bits
41817	Channel 1 Point 3	Signed Integer 16 Bits
41818	Channel 2 Point 3	Signed Integer 16 Bits
41819	Channel 3 Point 3	Signed Integer 16 Bits
41820	Channel 4 Point 3	Signed Integer 16 Bits
41821	Channel 5 Point 3	Signed Integer 16 Bits
41822	Channel 6 Point 3	Signed Integer 16 Bits
41823	Channel 7 Point 3	Signed Integer 16 Bits
41824	Channel 1 Point 4	Signed Integer 16 Bits
41825	Channel 2 Point 4	Signed Integer 16 Bits
41826	Channel 3 Point 4	Signed Integer 16 Bits
41827	Channel 4 Point 4	Signed Integer 16 Bits
41828	Channel 5 Point 4	Signed Integer 16 Bits
41829	Channel 6 Point 4	Signed Integer 16 Bits
41830	Channel 7 Point 4	Signed Integer 16 Bits
41830	Channel 1 Point 5	Signed Integer 16 Bits
41831	Channel 2 Point 5	Signed Integer 16 Bits
41832	Channel 3 Point 5	Signed Integer 16 Bits
41833	Channel 4 Point 5	Signed Integer 16 Bits
41834	Channel 5 Point 5	Signed Integer 16 Bits
41835	Channel 6 Point 5	Signed Integer 16 Bits
41836	Channel 7 Point 5	Signed Integer 16 Bits
41837	Channel 1 Point 6	Signed Integer 16 Bits
41838	Channel 2 Point 6	Signed Integer 16 Bits
41839	Channel 3 Point 6	Signed Integer 16 Bits
41840	Channel 4 Point 6	Signed Integer 16 Bits
41841	Channel 5 Point 6	Signed Integer 16 Bits
41842	Channel 6 Point 6	Signed Integer 16 Bits
41843	Channel 7 Point 6	Signed Integer 16 Bits
41844	Channel 1 Point 7	Signed Integer 16 Bits
41845	Channel 2 Point 7	Signed Integer 16 Bits
41846	Channel 3 Point 7	Signed Integer 16 Bits
41847	Channel 4 Point 7	Signed Integer 16 Bits
41848	Channel 5 Point 7	Signed Integer 16 Bits
41849	Channel 6 Point 7	Signed Integer 16 Bits
41850	Channel 7 Point 7	Signed Integer 16 Bits
41851	Channel 1 Point 8	Signed Integer 16 Bits
41852	Channel 2 Point 8	Signed Integer 16 Bits
41853	Channel 3 Point 8	Signed Integer 16 Bits
41854	Channel 4 Point 8	Signed Integer 16 Bits
41855	Channel 5 Point 8	Signed Integer 16 Bits
41856	Channel 6 Point 8	Signed Integer 16 Bits
41857	Channel 7 Point 8	Signed Integer 16 Bits
41858 – 41919 Reserved for future use.		

Oscillographic Data Interpretation

Once the point and configuration data is obtained from the relay, constructing the waveform curve is fairly straightforward as illustrated in Figure 12-13. The mathematics required for obtaining point data follows:

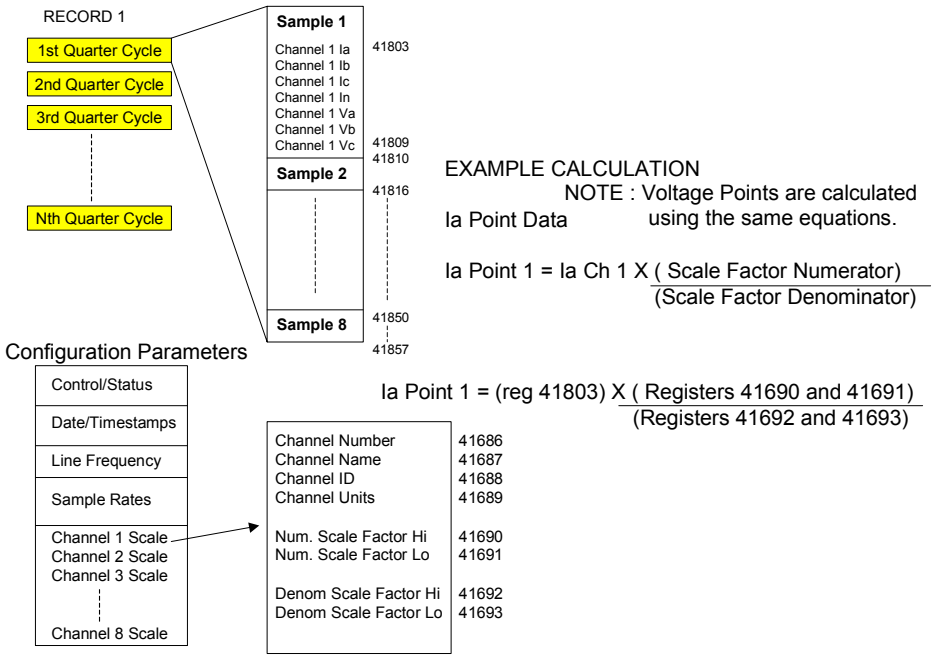


Figure 12-13 Data Interpretation

UCA PARAMETERIZATION

If the DPU 2000R has a UCA card installed within it, then the parameters may be obtained from the 6X registers since the UCA card has both Modbus and UCA parameters imbedded within. The following Table 12-27 contains the registers containing the parameterization of the UCA /Modbus Card (Type E, 6). The access of the parameters follow the same philosophy as previous blocks of data.

ADDRESS	ELEMENT	DESCRIPTION
63200	Reserved	Reserved
63201	Execute Register 0 = No Action 1 = Update Registers 2 = Refresh Registers	Unsigned 16 Bits Range 0-2
63202	Access Password	ASCII – 2 Characters Leftmost Digits
63203	Access Password	ASCII – 2 Characters Rightmost Digits
63204	SPARE_2	
63205	AP Title	ASCII (Leftmost 2 Characters)
63206	AP Title	ASCII – 2 Characters
63207	AP Title	ASCII – 2 Characters
63208	AP Title	ASCII – 2 Characters
63209	AP Title	ASCII – 2 Characters
63210	AP Title	ASCII – 2 Characters
63211	AP Title	ASCII – 2 Characters
63212	AP Title	ASCII – 2 Characters
63213	AP Title	ASCII – 2 Characters
63214	AP Title	ASCII – 2 Characters
63215	AP Title	ASCII – 2 Characters
63216	AP Title	ASCII – 2 Characters
63217	AP Title	ASCII – 2 Characters
63218	AP Title	ASCII – 2 Characters
63219	AP Title	ASCII – 2 Characters
63220	AP Title	ASCII – 2 Characters
63221	AP Title	ASCII – 2 Characters
63222	AP Title	ASCII – 2 Characters
63223	AP Title	ASCII – 2 Characters
63224	AP Title	ASCII – 2 Characters
63225	AP Title	ASCII – 2 Characters
63226	AP Title	ASCII (Leftmost 2 Characters)

63227	AE Qualifier	Unsigned Long (Hi Word)
63228	AE Qualifier	Unsigned Long (Lo Word)
63229	Mechanism Name	Unsigned Long (Hi Word)
63230	Mechanism Name	Unsigned Long (Lo Word)
63231	Authentication	ASCII (Leftmost 2 Characters)
63232	Authentication	ASCII – 2 Characters
63233	Authentication	ASCII – 2 Characters
63234	Authentication	ASCII – 2 Characters
63235	Authentication	ASCII – 2 Characters
63236	Authentication	ASCII – 2 Characters
63237	Authentication	ASCII – 2 Characters
63238	Authentication	ASCII – 2 Characters
63239	Authentication	ASCII – 2 Characters
63240	Authentication	ASCII – (Rightmost) 2 Characters
63241	Local P Selector	ASCII (Leftmost 2 Characters)
63242	Local P Selector	ASCII – 2 Characters
63243	Local P Selector	ASCII – 2 Characters
63244	Local P Selector	ASCII – 2 Characters
63245	Local P Selector	ASCII – 2 Characters
63246	Local P Selector	ASCII – 2 Characters
63247	Local P Selector	ASCII – 2 Characters
63248	Local P Selector	ASCII – 2 Characters
63249	Local P Selector	ASCII – 2 Characters
63250	Local P Selector	ASCII – 2 Characters
63251	Local P Selector	ASCII – 2 Characters
63252	Local P Selector	ASCII – (Rightmost) 2 Characters
63253	Local S Selector	ASCII (Leftmost 2 Characters)
63254	Local S Selector	ASCII – 2 Characters
63255	Local S Selector	ASCII – 2 Characters
63256	Local S Selector	ASCII – 2 Characters
63257	Local S Selector	ASCII – 2 Characters
63258	Local S Selector	ASCII – 2 Characters

63259	Local S Selector	ASCII – 2 Characters
63260	Local S Selector	ASCII – 2 Characters
63261	Local S Selector	ASCII – 2 Characters
63262	Local S Selector	ASCII – 2 Characters
63263	Local S Selector	ASCII – 2 Characters
63264	Local S Selector	ASCII – (Rightmost) 2 Characters
63265	Local TSAP	ASCII (Leftmost 2 Characters)
63266	Local TSAP	ASCII – 2 Characters
63267	Local TSAP	ASCII – 2 Characters
63268	Local TSAP	ASCII – 2 Characters
63269	Local TSAP	ASCII – 2 Characters
63270	Local TSAP	ASCII – 2 Characters
63271	Local TSAP	ASCII – 2 Characters
63272	Local TSAP	ASCII – 2 Characters
63273	Local TSAP	ASCII – 2 Characters
63274	Local TSAP	ASCII – 2 Characters
63275	Local TSAP	ASCII – 2 Characters
63276	Local TSAP	ASCII – (Rightmost) 2 Characters
63277	Local NSAP	ASCII (Leftmost 2 Characters)
63278	Local NSAP	ASCII – 2 Characters
63279	Local NSAP	ASCII – 2 Characters
63280	Local NSAP	ASCII – 2 Characters
63281	Local NSAP	ASCII – 2 Characters
63282	Local NSAP	ASCII – 2 Characters
63283	Local NSAP	ASCII – 2 Characters
63284	Local NSAP	ASCII – 2 Characters
63285	Local NSAP	ASCII – 2 Characters
63286	Local NSAP	ASCII – 2 Characters
63287	Local NSAP	ASCII – 2 Characters
63288	Local NSAP	ASCII – (Rightmost) 2 Characters
63289	Local Mac Address (Read-Only)	Unsigned Integer
63290	Local Mac Address (Read-Only)	Unsigned Integer

63291	Local Mac Address (Read-Only)	Unsigned Integer
63292	Local Mac Address (Read-Only)	Unsigned Integer
63293	ESH Interval	Unsigned Integer
63294	ESH Interval	Unsigned Integer
63295	TP Ack Time	Unsigned Integer
63296	TP Ack Time	Unsigned Integer
63297	CLNP Lifetime	Unsigned Integer
63298	CLNP Lifetime	Unsigned Integer
63299	TP Inactivity Time	Unsigned Integer
63300	TP Inactivity Time	Unsigned Integer
63301	TP Transit Delay	Unsigned Integer
63302	TP Transit Delay	Unsigned Integer
63303	TP Max Retransmit	Unsigned Integer
63304	TP Max Retransmit	Unsigned Integer
63305	TP Max PDU Size	Unsigned Integer
63306	TP Max PDU Size	Unsigned Integer
63307	TP Max SDU Size	Unsigned Integer
63308	TP Max SDU Size	Unsigned Integer
63309	TP Max Credits	Unsigned Integer
63310	TP Max Credits	Unsigned Integer
63311	TP Max Input Que Size	Unsigned Integer
63312	TP Max Input Que Size	Unsigned Integer
63313	TP Max Output Que Size	Unsigned Integer
63314	TP Max Output Que Size	Unsigned Integer
63315	TP Max Connections	Unsigned Integer
63316	TP Max Connections	Unsigned Integer
63317	Buffer Pool Size	Unsigned Integer
63318	Buffer Pool Size	Unsigned Integer
63319	IP Address	Unsigned Integer
63320	IP Address	Unsigned Integer
63321	Reserved	Reserved

63322	Reserved	Reserved
63323	Reserved	Reserved
63324	Reserved	Reserved
63325	GOOSE IN Address	Unsigned Integer
63326	GOOSE IN Address	Unsigned Integer
63327	GOOSE IN Address	Unsigned Integer
63328	GOOSE IN Address	Unsigned Integer
63329	GOOSE OUT Address	Unsigned Integer
63330	GOOSE OUT Address	Unsigned Integer
63331	GOOSE OUT Address	Unsigned Integer
63332	GOOSE OUT Address	Unsigned Integer
63333	Reserved	Reserved
63334	Reserved	Reserved
63335	Reserved	Reserved
63336	Reserved	Reserved
63337	Reserved	Reserved
63338	Reserved	Reserved
63339	Reserved	Reserved
63340	Reserved	Reserved
63341	Reserved	Reserved
63342	Reserved	Reserved
63343	Reserved	Reserved
63344	Reserved	Reserved
63345	Reserved	Reserved
63346	Reserved	Reserved
63347	Reserved	Reserved
63348	Reserved	Reserved
63349	Reserved	Reserved
63350	Reserved	Reserved
63351	Reserved	Reserved
63352	Reserved	Reserved
63353	SNTP IP Address	
63354	SNTP IP Address	

63355	Reserved	Reserved
63356	Reserved	Reserved
63357	Reserved	Reserved
63358	Reserved	Reserved
63359	Reserved	Reserved
63360	SNTP Enable	Unsigned Integer 0 = Disable 1 = Enable
63361	SNTP Period	Unsigned Integer Word Lo
63362	SNTP Period	Unsigned Integer Word Hi
63363	Reserved	Reserved
63364	SNTP Timeout ()	Unsigned Integer 50 <=x<= 1000 milli-sec
63365	SNTP Offset from UTC	Signed Integer - -780 <=x<= +720 minutes

Section 13 - Modbus ASCII Communication Test Example

The easiest method to initiate communications in the Modbus protocol is to read known discrete and register data. As per the DPU2000/DPU1500/DPU2000R Modbus Register documentation, the unit catalog number is resident at Register 40133. A list of the register definitions of the DPU2000/DPU1500R/DPU2000R is presented and explained in the next section. A Read Holding Register Modbus Command is explained. Documentation is available from Groupe Schneider further describing the Modbus ASCII emulation characteristics. The explanation contained within this document is intended to be a quick start guide to communication initiation.

The length of the catalog number is 12 characters or 6 registers. The following command string format, when sent will retrieve the catalog number from the unit.

: 01 03 00 83 00 06 73 lf cr

The above string in Modbus ASCII format should be sent:

3A 30 31 30 33 30 30 38 33 30 30 30 36 37 33 0D 0A

The string is translated as such:

Colon (in HEX), unit address = 01 (in HEX), Read Holding Registers (Code 3 in HEX), data memory desired address –1 = 132 decimal (0084 in HEX), number of registers read = 6 (0006 in HEX), message calculated LRC code 72 (37 32), and line feed (0D) and (0A).

A typical response shall include the following:

: Address number (01), Read Holding Registers Command (Code 3 in HEX), Byte Count Returned in decimal (0C in HEX 12 bytes in decimal) , Data Register 40133 = 3538 hex – 58 ASCII, Data Register 40134= 3743 Hex , 7C ASCII , Data Register 40135 = 3034, 04 ASCII Data Register 40136 = 3132 hex, 32 ASCII Data Register 40137 = 3631 HEX, 61 ASCII Data Register 40138 = 3131 HEX, 11 ASCII, and calculated LRC =79 (HEX) and line feed with carriage return (0D 0A).

The aforementioned response would be returned as such:

3A 30 31 30 33 30 43 35 38 37 43 30 34 31 32 36 31 31 31 37 39 0A 0D.

Calculation of the LRC (Longitudinal Redundancy Code)

Modbus ASCII protocol uses a Longitudinal Redundancy Code to verify correct reception of the command. This error check is used in addition to the parity option (used by the UART in the PC) and other data such as the byte count which verifies data returned. The process for calculation of the checksum is described as such:

1. Add all bytes in the message except for the colon, line feed, and carriage return. Exclude the LRC checksum which in included in the message structure.
2. Invert all bits in the word after the addition.
3. Add 1 to the inverted result. This is the checksum.

An example is as follows:
Command sent:

3A 30 31 30 33 30 30 38 33 30 30 30 36 37 33 0D 0A

Decode of the data from ASCII to HEX yields.

: 01 03 00 83 00 06 73 lf cr

The decoded LRC checksum is 73. The calculation of the checksum is as such:

1. Neglect the colon (3A) and the lf (Line Feed 0A) and cr (Carriage Return OD). This decreases the string to
2. The LRC checksum 73 (37 33 in ASCII) should also be saved for comparison to the original data string. The string for LRC calculation is 01 03 00 83 00 06.
3. The byte data should be added thus 01 + 03 + 00 +83 + 00 + 06 = 8D in HEX. Notice that the bytes have been decoded from ASCII before performing the addition.
4. A Two's compliment must be performed on the number to determine the LRC Checksum. Inversion of the number 8D hex yields 72 hex.
5. To complete the Two's compliment addition for accurate compilation of the checksum 1 hex must be added to the inverted bits to yield 72 + 1 = 73 HEX. Thus the two calculated values agree.

Please reference the Modicon Modbus Documentation for additional command configuration on each data type (0X, 1X, 4X and 6X read write capabilities).

Modbus CRC-16 Calculation

The CRC–16 error check is much more robust than that of the LRC error check. It is however, a more complex algorithm to compute. It's computation is started by setting a word of 16 bits to a value of FFFF hex. A byte of the message is logically OR'ed with the register word and then shifted in a predictable method. What follows is a reprint from the protocol manufacturer's manual MODICON MODBUS PROTOCOL REFERENCE GUIDE – PI-MBUS-300 Revision J Dated June 1996 published by Modicon Inc. Industrial Automation Systems, One High Street, North Andover, MA 01845.

"The Cyclical Redundancy Check (CRC) field is two bytes, containing a 16 –bit binary value. The CRC value is calculated by the transmitting device which appends the CRC to the message. The receiving device, recalculates a CRC during the receipt of the message, and compares the calculated value to the value it received in the CRC field. If the two values are not equal, an error results"

The CRC is started by first preloading a 16 bit register register to all 1's. Then a process begins of applying successive 8 – bit bytes of the message to the current contents of the register. Only the eight bits of data in each character are used for generating the CRC. Start and stop bits and the parity bit do not apply to the CRC.

During the generation of the CRC, each 8-bit character is exclusive Ored with the register contents. Then the reslult is shifted in the direction of the least significant bit (LSB), with a zero filled into the most significant bit (MSB) position. The LSB is extracted and examined. If the LSB was a 1, the register is then exclusive Ored with a preset, fixed value. If the LSB was a0, no exclusive OR takes place.

The process is repeated until eight shifts have been performed. After the last eighth shift, the next 8-bit character is exclusive OR'ed with the register's current value and the process repeats for eight more shifts as described above. The final contents of the register,after all the characters of the message have been applied, is the CRC value.

A procedure for generating a CRC is

1. Load a 16 Bit Register with FFFF hex (all 1's) Call this the CRC register.

2. Exclusive OR the first 8-bit byte of the message with the lwo-order byte of the 16-bit CRC register, putting the result in the CRC register.

3. Shift the CRC register one bit to the right (Toward the LSB), zero-filling the MSB. Extract and examine the LSB.

4. (If the LSB was 0): Repeat Step 3 (Another Shift)

(If the LSB was 1): Exclusive OR the CRC register with the polynomial value A001 hex (1010 0000 0000 0001)

5. Repeat Steps 3 and 4 until 8 shifts have been performed. When this is done, a complete 8-bit byte will have been processed
6. Repeat Steps 2 through 5 for the next 8 bit byte of the message. Continue doing this until all bytes have been processed.
7. The final contents of this CRC register is the CRC value.
8. When the CRC is placed into the message, its upper and lower bytes must be swapped as described below."

The CRC-16 message generation capability is best done by a hardware chip or using a software algorithm. Within the aforementioned manual, the protocol's inventor supplies a C language program to calculate the CRC-16 code. It is advised that the text be referenced for those wishing to calculate such a code.

DPU2000/DPU2000R/DPU1500R Modbus Exception Response Analysis

If the DPU2000/DPU2000R/DPU1500R does not understand the command sent to the device or if the command is sent in the wrong format, the DPU2000/DPU2000R/DPU1500R shall generate an exception response. A Modbus exception response is in the format of that shown in Figure 13-1. As illustrated, the function code is "ANDed" with 80 HEX. Following the modified function code, an exception code byte will follow. The customary LRC and terminator of a Carriage Return and Line feed will terminate the communication string.

Table 13-1 shall list the standard Modbus Exception Codes and Table 13-2 lists the exception codes as the DPU2000/DPU2000R reports them. Notice that the DPU2000/DPU2000R does not report its exception codes as per the Modbus standard defined codes.

Table 13-1. Modbus Standard Exception Codes

Code	Name
01	Illegal Function
02	Illegal Data Address
03	Illegal Data Value
05	Acknowledge
06	Slave Device Busy
07	Negative Acknowledge
08	Memory Parity Error

Table 13-2. DPU2000/DPU2000R Defined Exception Codes

Code	Description
01	Invalid Password
04	Invalid Register Address
05	Invalid Range Accessed
06	Invalid Data
34	Invalid Function Code
36	Supervisory Control Disabled

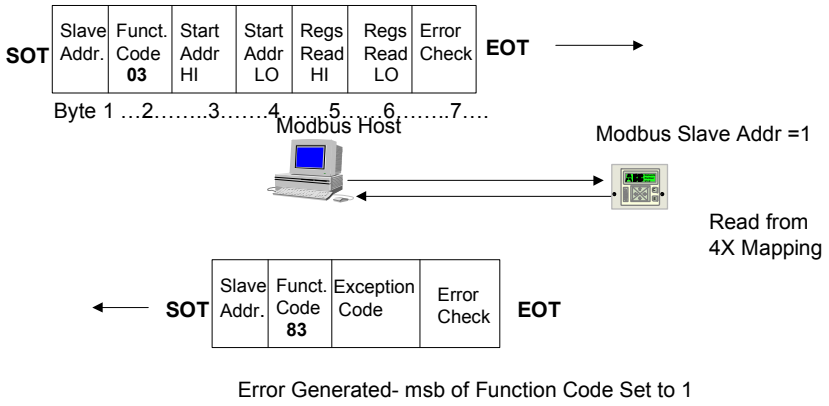


Figure 13-1. Exception Code Example for Holding Register Read

Modbus Troubleshooting Tips

The Modbus Protocol contains a set of commands intended to assist with network troubleshooting. Those commands are:

08 – Diagnostic Functions
0B – Fetch Communication Event Counter
0C – Fetch Communication Log

The DPU2000 and DPU2000R do support one sub function code of the Diagnostic Function 08. Modbus Commands 0B and 0C are not supported.

Figure 13-2 lists the 08 Diagnostic Function Format.

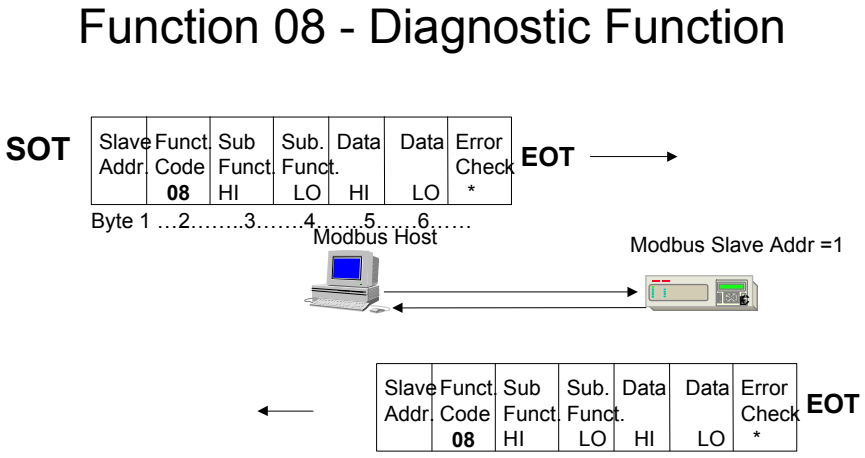


Figure 13-2. Diagnostic Function Code

Only Sub function 00 is supported. Sub function 00 is the loop-back function. If the sub function hi and lo bytes are 00 hex, whatever is placed in the data field by the host will be received by the DPU2000 or DPU2000R and returned or looped back to the host.

Another method to troubleshoot the DPU2000/DPU2000R is to use the 03 (Read Holding Register) command and access the communication status registers. The communication status registers reside at 40712 through 40179. Section 11 of this document list the method to access and use these registers.

Finally, it is always advantageous to use a datascope or a communication analyzer when troubleshooting a Modbus Network. Such devices allow the implementers to view the data strings between the host and IED. Modicon's parent company Schneider Electric has designed many utilities and products to assist the network professional with troubleshooting. Such tools are inexpensive when compared to the person-hours spent guessing as to what is sent between a host and IED. Such tools available are at a modest cost, such as Modlink, or at no cost MTS. Many of these tools are available on the website www.modicon.com.

DPU2000/DPU2000R Modbus ASCII Communication Timing Analysis

Perhaps the most common error in implementing a Modbus ASCII network is timing setup for communication. Modbus ASCII protocol operates according to the following timing rules:

- If the DPU2000/DPU2000R **receives** a command without a communication error (LRC, PARITY, FRAMING, OVERRUN … errors), a normal response occurs.
- If the DPU2000/DPU2000R **does not receive** a command without a communication error (LRC, PARITY, FRAMING, OVERRUN…, errors),no response is returned. The host (master) device will sense a timeout according to its timeout parameter. The host could then send a new command or retry sending the original command.
- Modbus ASCII allows for internals up to 1 second between characters are acceptable gaps. The DPU2000/DPU2000R will not timeout. Character send gaps in excess of 1 second will result in DPU2000/DPU2000R Modbus port timeouts.

DPU2000/DPU2000R Modbus network implementers will usually notice communication errors in the form of excessive communication retries, errors, or non-responses. Understanding communication timing is a subject rarely covered in protocol manuals, but an important topic in network implementation.

Network timing is predicated upon the following factors:

Host Latency (How long does it take a host device to generate a command, receive the response and interpret the data).
Intermediate Device Latency (If a Modem, data concentrator or other device is between the end device required for data retrieval, how long does it take for each device to receive the command and process it downline to the next device).
DPU2000/DPU2000R Device Latency (How long does it take for a DPU2000/DPU2000R to receive a command, and return a response to the network).
Baud Rate (How fast is each data bit propagated on the medium.)
Protocol Efficiency [Network Bandwidth Utilization] (Does the protocol utilized allow for the issuance of another command before a response is received from an outstanding communication request).

The common question to a network system engineer is usually " How fast can I get my relay alarm data to appear on the screen?" An analysis of the amount of data and the above 5 areas is required.

Host latency varies widely by manufacturer or the PC or host computer. Software speed and port access varies widely. Most manufacturers of these hardware and software platforms have general benchmarks to supply to the users for processing time once the device acquires the data from the communication port.

Intermediate Device Latency also varies from the type of device used. Some modems have a device turnaround of 5 mS per transactions whereas, a radio modem may require hundreds of mS to obtain an open frequency from which to transmit.

This section shall illustrate and explain a simple network transaction based upon a simple point to point communication from a single DPU2000/DPU2000R to a host device as illustrated in Figure 13-3 of this document. **This example shall exclude SCADA Master host latency**.

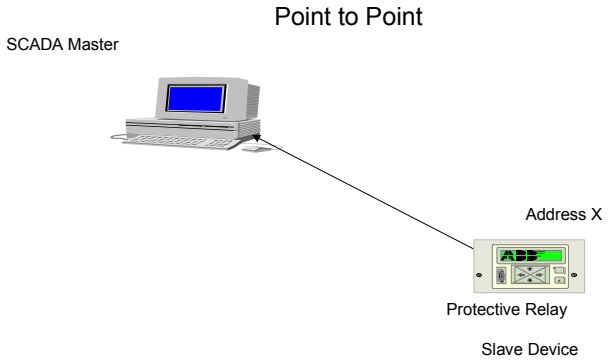


Figure 13-3. Example Communication Timing Topology

Modbus Baud Rate Analysis

In Section 4 **Modbus ASCII Protocol** is re-examined, the Modbus frame is illustrated in Figure 4-9. The frame is a standard 10 bit frame. One character (7 data bits) is transmitted as 10 bits per frame.

The rate of the data transfer is determined by the selected baud rate, the faster the baud rate, the faster the communication. The DPU2000/DPU2000R supports baud rates of 1200, 2400, 4800, 9600 and 19200. The effect of transfer time is shown in Table 13-3. Each bit has specific transfer time which correlates to a specific character transfer time.

Table 13-3. Character Transfer Time vs Baud Rate

Baud Rate	Transfer Time Per Bit	Transfer Time Per Character
300	3.33 mS	3.33 mS
1200	0.833 mS	8.333 mS
2400	0.4167 mS	4.167 mS
4800	0.2083 mS	2.083 mS
9600	0.1041 mS	1.041 mS
19200	0.0521 mS	0.521 mS

These are fixed times determined by the laws of physics, and are standard for asynchronous bit stream transfers ASCII.

Each Modbus transfer varies in the amount of bytes transmitted and requested. Table 13-3 lists the amount of fixed data per some of the common Modbus Commands. For example, each data transmission contains the following characters as per Figure 8:

- Colon (:)[3A Hex]
- Slave Address (Two Characters)
- Function (Two Characters)
- Error Check (Two Characters)
- Line Feed (One Character)
- Carriage Return (One Character)

Each base transmitted and received command has at least 9 characters for transmission. The transmission time, depending upon baud rate can range from 74.97 mS (at 1200 baud) to 4.689 mS (at 19200 baud). For example Figure 10 illustrates the Function 01 Read Coil Status format. Figure 11 illustrates the transaction request for four coils. Analysis of the data transmitted and received yields the following:

Transmission Request:

Common characters 9 + 4 address characters + 4 data request characters
Total characters for transmission request = 17 characters.

Returned Response

Common characters 9 + 2 data byte characters + 4 data returned characters.
Total characters returned by DPU2000/DPU2000R = 15 characters.

Depending upon the baud rate the total time for the communication characters to propagate along the network could range from:

Transmission Request:

17 characters at 141.61. mS (1200 Baud) to 8.857 mS (19200 Baud)

Returned Response

15 characters at 124.95 mS (1200 Baud) to 7.815 (19200 Baud)

Total network transfer time via the physical medium can range from 265.56 mS at 1200 baud to 16.672 at 19,200 baud.

Baud rate is a major influence at 1200 baud and a lesser influence at 19200 baud. It must be realized that this is only one of three components analyzed for a complete throughput analysis. In this case the Host time to generate the command.

DPU2000/DPU2000R Throughput Analysis

Communication implementation within a protective relay is a demanding task. In other devices, communications may take first priority. Within an ABB protective relay **PROTECTION IS THE FIRST PRIORITY.** Communication shall not compromise protection capabilities. Thus communication throughput may vary depending upon the demands of the protection. Table 13-4 illustrates the DPU2000/DPU2000R average benchmark times for recognition of a Modbus command at the physical port and the time it takes to generate a reply to the respective port. The times listed in the table are average times and do not include the calculated values generated in Section 4.

Table 13-4. DPU2000/DPU2000R Modbus Command Throughput (average time in mS)

			Reading from DPU2000/DPU2000R		Write to DPU2000/DPU2000R	
Modbus Command	**Register Start**	**Num. Refs.**	**Min (ms)**	**Max (ms)**	**Min (ms)**	**Max (ms)**
Real Logical Outs	00001	14	5.023	14.417		
Read Physical Outs	00129	4	1.497	10.688		
Read Physical Inputs	10129	2	1.381	13.726		
Load Metering	40513	27	21.270	30.184		
Configuration & Status	40129	22	18.848	26.324		
Event Records	41281	12	9.927	23.237		
Config Settings	60001	21	18.657	23.477	39.224	289.634
Primary Settings	60257	39	27.557	37.834	67.129	497.97
Master Trip Settings	61665	10	9.728	17.660	22.935	110.169
Test Setup:						
DPU2000/DPU2000R COMM Port Settings: 9600, E, 7, 2, through the front RS232 port						
Modlink Setup: 500 ms Poll though COM1 on a 486DX100 Notebook Serial Port						
DPU2000/DPU2000R is "idle", No Current/Voltage applied.						
Write Min - Writing to update the Write Link side in ModLink						
Write Max - Time to Write 3 Sets of parameters to EEPROM and Return Response						
Write Max times ARE proportional to the size of the block being written, the larger the block,						
the longer the write time.						

For the example, the DPU2000/DPU2000R generation time for the sample example can range from 1.497 mS to 10.688 mS

Final Throughput Calculation and Analysis

A final calculation of our example throughput is warranted. For this example, the host update time shall now be assumed to be 250 mS. This 250 mS shall be an example estimation or time to generate a command, interpret the received command and update the screen. This is just for this example and varies according to:

- Speed of the host processor (hardware bus structure, # of processors, video card update, RAM memory, microprocessor speed…)
- Operating system selected (LINUX, UNIX, OS2, WIN NT, WIN 3.1, WIN 98, WIN 95,…)
- MMI Port Driver Efficiency (PRICOM, Power RICH, USDATA)

Two results will be calculated, operation at 1200 and 19200 baud. The example is described as per Figure 11 within this document. The formula used to produce the typical response is:

System Throughput = Host Processing Time + String Transmit Time + DPU2000/DPU2000R Processing Time + String Reception Time

At 1200 Baud:

527.248 mS = 250 mS + 141.61 mS + 10.688mS (using worst case) + 124.95 mS

At 19200 Baud:

277.36 = 250 mS + 8.857 mS + 10.688 (using worst case) mS + 7.815 mS

Figures 13-4 and 13-5 illustrate the individual contributions from each of the components as a percentage of total transaction time.

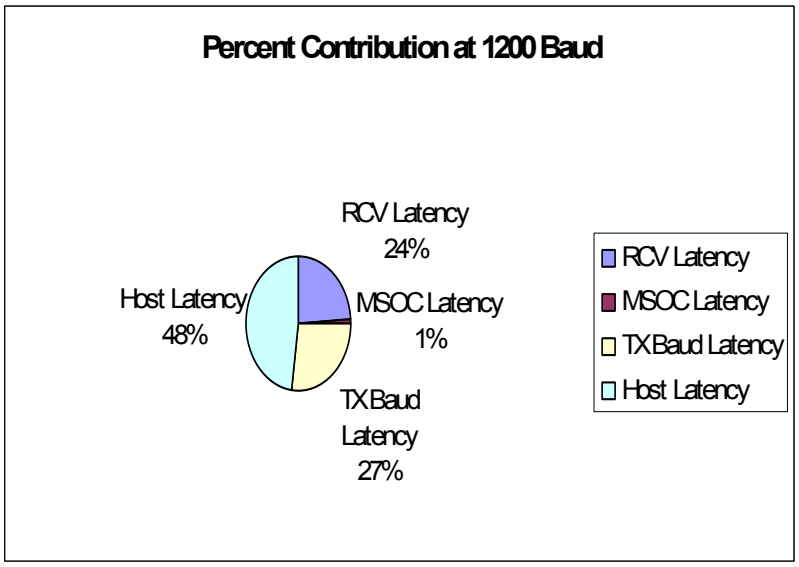


Figure 13-4. Network Throughput Analysis at 1200 Baud

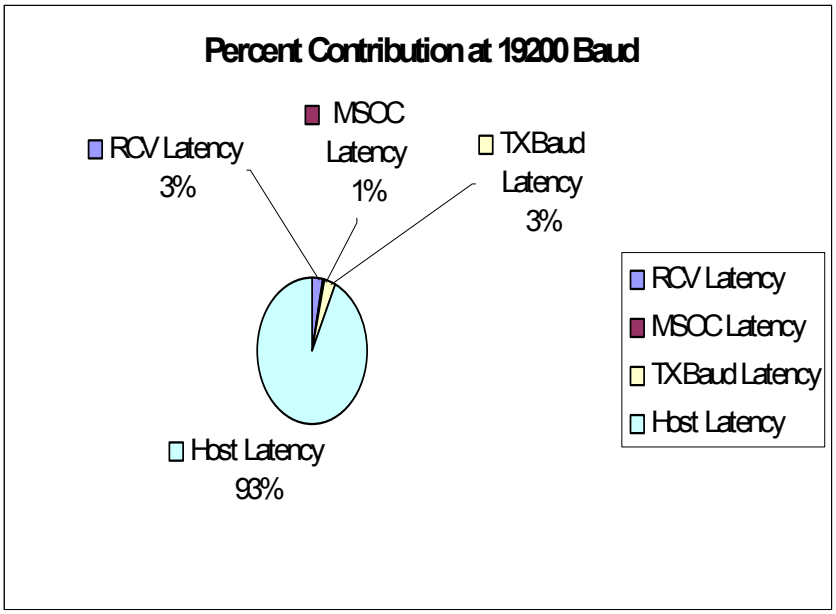


Figure 13-5. Network Throughput Analysis at 19200 Baud

Analysis of the simple example yields a few points to be considered when analyzing system throughput. Each element involved in communication timing contributes significantly to overall throughput. If the host executed and updated faster, overall throughput could be improved. If intermediate devices were inserted within the network, transaction time would increase proportionately. Baud rate is only one of many contributing factors in calculating system throughput. If one network access was required for retrieval of system data, overall network efficiency would be improved. If in a networked system, the protocol utilized would allow for additional data request commands while the slave device is processing a response, Network throughput time would be improved.

Virtual treatises have been written on improving system throughput and data updates. This simple example illustrates and allows the user to calculate system throughput times. This is especially critical so that the system user will not be surprised with overall system response.

ABB has implemented features within the protective relay to maintain system data integrity. Latched bit status, momentary change detect are a few features implemented within the various implementations of the Modbus protocol.

Modbus Plus Troubleshooting

Schneider Electric has designed Modbus Plus to be a very robust communication network. The publication 890 USE 100 00 Version 2.0 titled Modicon Modbus Plus Network Planning and Installation Guide Copyright 1995, AEG Schneider Automation, Inc. details the method for troubleshooting a Modbus Plus network.

There is no communication analyzer for Modbus Plus to view the communication commands occurring over the network. The SA 85 or PCMCIA Modbus Plus adapters have a software utility called MBP STAT which allows a personal computer to attach to the network allowing a network professional to troubleshoot a Modbus Plus anomaly. Please reference the MBP STAT documentation for use of this valuable troubleshooting tool.

Issues common to Modbus Plus communication errors arise from the following

1. Improper Device Termination. The manufacturer's in-line and termination connectors must be used. Termination connectors must be used at the end of the lines for a string. The end of the string could be a repeater, bridge, repeater, or end device node.

2. Improper cable used. The manufacturer's cable should be used in that it is the correct impedance, capacitance and physical wire dimensions to physically mate with the connector.

3. Improper addressing is assumed. The DPU2000/2000R 's address is in HEX. The Modbus Plus host and MBP STAT uses decimal addressing. Additionally, it must be remembered that an additional byte must be appended to the end of the address signifying the path the host wishes to communicate.

4. Improper routing of the cable. The cable should be routed clear of high current devices and wires. Although, Modbus Plus is an industrial network, it is not recommended to route or wrap the cable around devices (such as bus bar) which emit EMI/RFI or high current spike devices. The network is a serial network, branches, or splits are not allowed in the cabling. If such configurations are necessary, please use fiber optics.

5. Improper grounding of the cable.

If proper care is not taken in the planning and installation of the network, the time saved on planning and installation is usually spent and exceeded in troubleshooting of the network. Since Modbus Plus is a serial network, any loose connection, impedance mismatch, or anomaly is usually difficult to find. Cable planning and installation errors are usually seen as communication errors or retries seen using the MBP STAT utility. The cable must be checked for continuity (in case of damage) and usually the cable must be disconnected and the cable sections checked.

A copy of the device troubleshooting section from the aforementioned Modbus Plus text is included for the benefit of the reader. The section covers cable continuity.

- Before checking continuity, disconnect all network cable connectors from the node devices-leave the drop cable ground lugs (ed. Note – if any since the tap and drop connectors have ground lugs whereas the dark and light grey connectors do not).to their site panel grounds.
- At any node device connector, measure the resistance between pins 2 and 3 (the signal pins), in the range of 60.80 Ω, which include the cable wire resistance.
- At each node device connector, check for an open circuit between pin 2 (a signal pin) and pin 1 (the shield pin); then check between pin 3 (a signal pin) and pin 1 – an open circuit should exist for both checks.
- At each connector, check the continuity between pin 1 and the plant ground point on the local site panel or frame – direct continuity should be present.

If the above continuity checks are not consistent, break the network at various points, and it is recommended that a termination connector be selected at the break. Perform the above tests using MBP STAT and the continuity tests outlined above until the error rate is at a negligible level.

Also as with the Modbus test procedures, Modbus Plus has access to the communication status registers. Another method to troubleshoot the DPU2000/DPU2000R is to use Read 4X Holding Register command via a DDE editor or a PLC's MSTR instruction. The communication status registers may then be accessed. The communication status registers reside at 40712 through 40179. Section 11 of this document lists the method to access and use these registers.

Modbus Plus Throughput

The Manual Titled Modicon Modbus Plus Network Planning and Installation Guide Copyright 1995, AEG Schneider Automation, Inc., lists the methods to calculate Modbus Plus network throughput . It is recommended that the aforementioned text be consulted to perform a specific network throughput analysis.

The same principles for any protocol analysis apply to Modbus Plus Protocol analysis. Modbus Plus is a very efficient protocol since it's bandwidth is effectively utilized by using the hybrid features of an HDLC protocol with token passing. The ability of the network to carry out 32 individual conversations and 2 Global Data broadcast conversations is a very useful capability of the network. Combined with a high baud rate of over 1 megabaud, fast throughput is assured.

A typical Modbus Plus network is depicted in Figure 13-6. A Programmable Logic Controller is connected to a DPU 2000R protective relay accessing data along one of its 8 data slave paths. A Personal Computer Host is not used as a device in this example since it is difficult to predict the latency of the host device. As seen from the example calculated with Modbus, host latency (in this case the PLC), network latency, and IED latency (DPU

2000R) all must be evaluated in their contributions to overall network throughput. The PLC is using a Master instruction to access data on the network. The amount of logic in the PLC is 1K of ladder instructions operating with a combined scan rate of 4 mS per K of logic. A PLC physical input is assumed to be using in triggering the data for this example. The latency of the I/O module is assumed to be 1 mS (125 VDC Input Module).

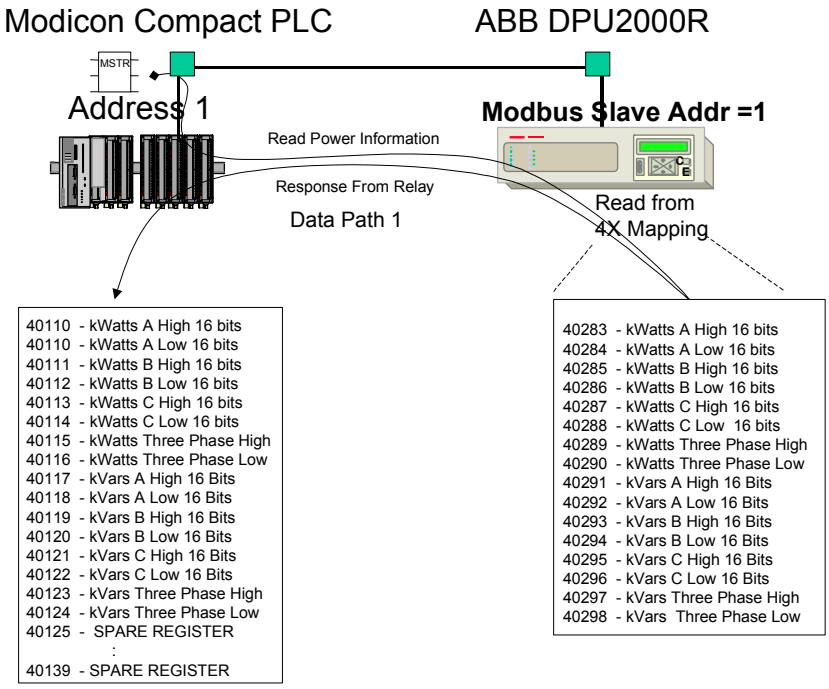


Figure 13-6. Modbus Plus Network Throughput Example

For a network with two nodes on a network as illustrated in Figure 13-6, the first step is to calculate the token rotation time using a master instruction.

Using the Token Rotation Time on Page 74 of the aformentioned Modbus Plus Manual, 890 USE 100 00 Version 2.0 where

TR = Token Rotation
DMW = Average number of words per Data Master Path used in the network (maximum = 100)
DMP = the number of Data Master Paths used continuously in the network
GDW = the average number of global data words per message used in the network (maximum = 32)
N = the number of nodes on the network.

Thus the token rotation is calculated according to the formula:
TR = (2.08 + 0.016 * DMW) * DMP + (0.19 + 0.016 * GDW) * GDN + 0.53 * N

In this example the PLC is continuously requesting 16 words of data. Only 1 path in this example (Path 1 is being utilized). For the sake of simplicity, no Global Data is being used on the network. The calculation for the token rotation time for the network in Figure 13-6 is:

TR = (2.08 + 0.016 * 16) * 1 + (0.19 + 0.016 * 0) * 0 + (0.53 * 2)

TR = 2.336 + 0 + 1.06

TR = 3.239 mS

As per the suggestions in the manual, the worst case token rotation time is:
TR wk = 1* TR = 3.239 mS

As per the suggestions in the manual,the best case token rotation time is:

TR bk = 0.5 * TR = 1.620 mS

Let us assume that a single read is triggered by a physical input on the PLC transitioning from a level 0 to a level 1 on the PLC processor.

A PLC throughput analysis of the host yields the following:

PLC Input Delay = 1mS
PLC Scan = 4 mS per K: 2 scans of the PLC = 8 mS = 2 * 4 mS
PLC Scan and Delay = 5 mS best case and 9 mS worst Case

It is interesting to note that 32 words of Global Data (if used in this calculation) were requested. An additional token rotation time of (32* 0.016) * 1 = 0.512 mS would be added to a token rotation worst case (0.256 average contribution to the network otherwise). Thus with Global data, the average contribution for a single transaction would be 1.024 mS worst case for each network transaction.

Appendix A – Standard 10-Byte Protocol Document for DPU2000/2000R/1500R

Revision 13.0

1 Document Revision History

Rev	Date	Author	Notes
4.00	05/29/96	DAH	ER No. 960045
5.00	04/14/99	DAH	Revised document's format to reflect current ABB documentation format. Changed document name to reflect addition of 1500R to the DPU Series of relays. Modified commands for the DPU1500R Protocol Command Set.
6.00	11/99	CWH	Revised document and added 59G, 67N, and 3V0 enhancements for the DPU2000R 4.10 release .
7.00	04/10/01	KEB	Add 47, 47*, 3ph_59, and 3ph_59* to logical outputs in 3 0 7 Command
8.0	04/29/01	Vab	Added 21P-1/2/3/4 and 21P-1*/2*/3*/4*. Added appendix A for protocol change details for V5.0 DPU2000R.
9.0	07/12/01	Vs	Added C1 – C6 and 9 Targets Alarms for Logical Outputs in Block 6, offset 52 for cmd 3 1 1
10.0	10/12/01	KEB	Add Support for C1-C6 and DPU200R rel Ver 5.10.
11.0	03/11/02	Vab	Added Table of Figures & Table of Contents. Consolidated multiple definitions into tables for logical inputs, input bit assignments, and output bit assignments. Added 3-0-9 command for Clear Records, reserved for future use.
11.1	04/01/03	Vab	Added SEFT to bit 8, offset 50, for 3-1-1 command.
12.0	04/01/03	Vab	Updated for V5.20 DPU2000R logical i/o & operation record additions. Company name was 'ABB Automation Inc.'.
13.0	04/01/03	Vab	Added REMOTE-D for V5.30 DPU2000R.
14.0	04/04/03	JSC	Added new operations records for capturing information on 065 error. Also Added 3 – 1 – 4, 3 – 1 – 5, and 3 – 1 – 6 commands
15.0	07/24/03	Vab	Changes for V5.40 DPU. Added logical inputs: SWSET, SHIFTA, & SHIFTB. Added logical outputs: PRI-ON, ALT1-ON, ALT2-ON, SHIFTA-1, SHIFTA-2, SHIFTA-3, SHIFTA-4, SHIFTB-1, SHIFTB-2, SHIFTB-3, SHIFTB-4.
16.0	07/28/03	VS	In 8.2.1.1.7 BLK 6: PHYSICAL and LOGICAL INPUT/OUTPUT BLOCK : Offset 50 was changed to 52 and offset 52 changed to 56 on p 30
17.0	01/19/2004	VAB	Added note ('DFR commands found in extended Modbus register set') to 3 14 n commands (waveform capture) section.

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9.3 DPU2000R version 5.20, protocol document revision 12.0 ..... **Error! Bookmark not defined.**
9.4 DPU2000R version 5.30, protocol document revision 13.0 ..... **Error! Bookmark not defined.**
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5 Introduction

5.1 Purpose

The purpose of this protocol document is to define the valid commands for the DPU Series of relays. The words transmit and receive in each command description, are with respect to the relay.

This DPU Series Protocol Command Set document is intended for ABB personnel and customers.

5.2 Scope

This DPU Series Protocol Command Set document will depict the manner in which a three-byte INCOM protocol is translated to a 10-byte RS-232 protocol. This document defines the communication commands required for the following product models: DPU2000, DPU2000R and DPU1500R. The first three characters of the DPU's catalog number identifies the model. For a DPU2000 they are 484 or 487. For a DPU2000R they are 587 or 687. For a DPU1500R they are 577. Features that are specific to only one unit model or variation of that model will be noted throughout this document.

Starting with V5.0 DPU2000R, appendix A lists the protocol changes between box versions.

6 Protocol Translation

The commands are spelt out in a 10-byte RS-232 protocol or a 3-byte INCOM protocol. It will be easy to understand the commands in a 33-bit INCOM context and then translate the protocol to a 10-byte RS-232 protocol. The protocol messages are of two types - command and data.

Command Message (33 bit INCOM)

	S	S	C/D	Inst	Cmd	Subcmd	Address	BCH	S
Bit	1	2	3	4 to 7	8 to 11	12 to 15	16 to 27	28 to 32	33

Figure 5 - Command Message (33-bit INCOM)

Data Message (33 bit INCOM)

	S	S	C/D	Data 1	Data 2	Data 3	BCH	S
Bit	1	2	3	4 to 11	12 to 19	20 to 27	28 to 32	33

Figure 6 - Data Message (33-bit INCOM)

6.1 Command Message

An INCOM command message can be represented in a 10 byte RS-232 protocol as shown in Figure 7 below.

Command Message (10 byte RS-232)

	STX	C/D	Inst	Cmd	SCmd	Addr Lo	Addr Mid	Addr Hi	CS Lo	CS Hi
Byte	1	2	3	4	5	6	7	8	9	10

Figure 7 - Command Message (10 byte RS 232)

The address bytes, Addr Lo, Addr Mid, and Addr Hi, are a 3 digit hex address. The checksum is 256 minus the sum of the ASCII characters in bytes 1 to 8. CS Lo is the low byte and CS Hi is the high byte of the checksum.

Example (3 4 1 command with a unit address of 001)

STX	=	hex 02	=	use 2 -->	Start of transmission
C/D	=	hex 31	=	ASCII 1 -->	Command type of message
Inst	=	hex 33	=	ASCII 3 -->	Instruction byte
Cmd	=	hex 34	=	ASCII 4 -->	Command byte
SCmd	=	hex 31	=	ASCII 1 -->	Subcommand byte
Addr Lo	=	hex 31	=	ASCII 1 -->	Unit address low byte
Addr Mid	=	hex 30	=	ASCII 0 -->	Unit address mid byte
Addr Hi	=	hex 30	=	ASCII 0 -->	Unit address high byte
CS Lo	=	hex 34	=	ASCII 4 -->	Checksum low byte
CS Hi	=	hex 46	=	ASCII F -->	Checksum high byte

Checksum = 256 - (STX + C/D + Inst + Cmd + SCmd + Addr Lo + Addr Mid + Addr Hi)

256 - (2 + 1 + 3 + 4 + 1 + 1 + 0 + 0) = F4

6.2 Data Message

An INCOM data message can be represented in a 10 byte RS-232 protocol as follows:

Data Message (10 byte RS-232)

	STX	C/D	D1 Lo	D1 Hi	D2 Lo	D2 Hi	D3 Lo	D3 Hi	CS Lo	CS Hi
Byte	1	2	3	4	5	6	7	8	9	10

Figure 8 - Data Message (10 byte RS-232)

Where D1 Lo is the low nibble of the first data byte and D1 Hi is the high nibble of the first data byte, D2 Lo is the low nibble of the second data byte and D2 Hi is the high nibble of the second data byte, and D3 Lo is the low nibble of the third data byte and D3 Hi is the high nibble of the third data byte.

The checksum is 256 minus the sum of the ASCII characters in bytes 1 to 8. CS Lo is the low byte and CS Hi is the high byte of the checksum.

Example (3 data bytes, ASCII characters 4, 8, and 7)

STX	=	hex 2 -->	Start of transmission
C/D	=	hex 0 -->	Data type of message
D1 Lo	=	hex 4 -->	Data 1 low byte
D1 Hi	=	hex 3 -->	Data 1 high byte
D2 Lo	=	hex 8 -->	Data 2 low byte
D2 Hi	=	hex 3 -->	Data 2 high byte
D3 Lo	=	hex 7 -->	Data 3 low byte
D3 Hi	=	hex 3 -->	Data 3 high byte
CS Lo	=	hex 2 -->	Checksum low byte
CS Hi	=	hex E -->	Checksum high byte

The three data bytes translate to:
Data 1 = 34 --> ASCII 4
Data 2 = 38 --> ASCII 8
Data 3 = 37 --> ASCII 7

Checksum = 256 - (STX + C/D + D1L + D1H + D2L + D2H + D3L + D3H)
256 - (2 + 0 + 4 + 3 + 8 + 3 + 7 + 3) = E2

7 Transmission and Reception Convention

To acknowledge successful receipt of a message, an ACK is transmitted. The three byte message packet is 0x000013. For an unsuccessful reception, ie. a checksum error or an error in command processing, a NACK is transmitted. The three byte message packet is 0x100013.

The commands for the relay can be categorized into three basic types according to the response that is expected by the master. When a command or data is received, the relay must acknowledge if the reception was successful.

7.1 Simple Commands

A simple command directs the relay to perform specific actions. After the successful completion of these actions, the relay transmits an ACK as seen below.

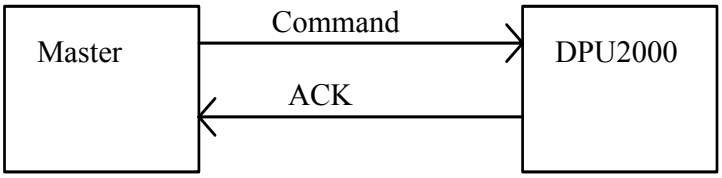

Figure 9 - Simple Command Communication Flow

7.2 Upload Data

This type of command requests the relay to transmit specific data. The proper transmission of this data is the relay acknowledgement of this type of command as seen in Figure 10 below.

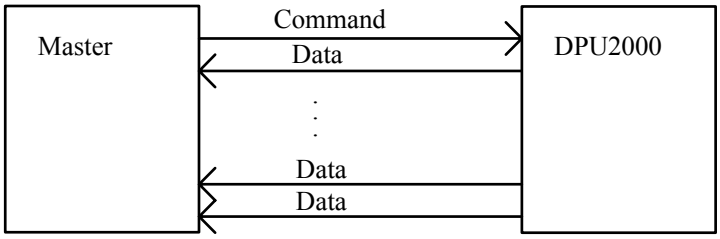

Figure 10 - Upload Data Communication Flow

7.3 Download Data

These commands edit the relay data. The relay responds with an ACK after the successful receipt of each data message packet. This can be seen in Figure 11 below.

Message Packet Checksum: This checksum is different than the checksum associated with every INCOM message packet. The value of the checksum is contained in a two byte integer and is the summation of all

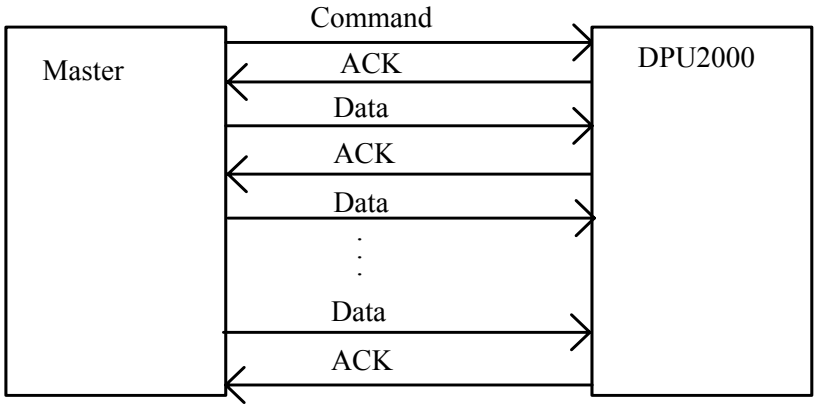

Figure 11 - Download Data Communication Flow

message bytes (1/1 + 1/2 + 1/3 + 2/1 + 2/2 + ...) for the command. The only exception is that the checksum message bytes are not included in the summation.

Example (3 3 1 command): (values are hex equivalent of the ASCII)

1/1 = hex 05	3/1 = hex 44
1/2 = hex 31	3/2 = hex 00
1/3 = hex 04	3/3 = hex 00
2/1 = hex 00	4/1 = hex 00
2/2 = hex 01	4/2 = hex 00 <-- checksum high byte
2/3 = hex 44	4/3 = hex C3 <-- checksum low byte

8 Command Set Summary

Inst	Cmd	Subcmd	Definition
3	0	n	Status Commands
3	1	n	Register Data Acquisition Command
3	2	n	
3	3	n	Transmit Settings Commands
3	4	n	Transmit Settings Commands
3	5	n	Transmit Meter/Record Commands
3	6	n	Load Profile Commands
3	7	n	
3	8	n	
3	9	n	Relay Commands
3	10	n	Receive Edit Buffer Commands
3	11	n	Receive Edit Buffer Commands
3	12	n	
3	13	n	Programmable Curve Commands
3	14	n	Waveform Capture Commands
3	15	n	Reserved for Factory

8.1 Transmit Status "N" Commands (3 0 n)

N	Definition
0	Transmit Fast Status
1	Reserved
2	Unit Information
3	Reserved for RCVDALL
4	Unreported Record Status
5	Reset Alarms/Target LEDs
6	Reset Max/Min Demand Currents
7	Logical Input/Output Status
8	Reset Relay Status Flag

8.1.1 Transmit Fast Status (3 0 0)

This command will cause the relay to respond with one data message with the format shown below:

```
byte 3                      |byte 2                      |byte 1
ST2 ST1 L T4 T3 T2 T1 T0|P5 P4 P3 P2 P1 P0 A3 A2 | A1 A0 D5 D4 D3 D2 D1 D0
```

D5 D4 D3 D2 D1 D0 => Division Code. RTD division code is 5 (000101)
A3 A2 A1 A0 => A0 - If this bit is set, one or more Unreported Operations have occurred.
A1 => Reserved
A2, A3 => Reserved
P5 P4 P3 P2 P1 P0 => Product ID. (DPU2000 series = 001110)
T2 T1 T0 => Reserved
T4 T3 => Reserved
L => Local Operator interface action. (Future implementation)
ST2 ST1 => Corporate standard status bits. (Future implementation)

8.1.2 Unit Information (3 0 2)

This command will cause the relay to transmit data messages containing catalog number and the software version.

1/1-5/3	Catalog Number (15 characters)
6/1	CPU Software Version high byte (*100)
6/2	CPU Software Version low byte (bit 0-14 version number *100, bit 15 1=non released software version)
6/3	DSP Software Version (*10)

7/1	Front Panel Software Version (*10)
7/2	Rear Communication Software version (*10)
7/3	Serial Number most significant high byte
8/1	Serial Number most significant low byte
8/2	Serial Number least significant high byte
8/3	Serial Number least significant low byte

8.1.3 RCVDALL (3 0 3)

- Reserved -

8.1.4 Unreported Record Status (3 0 4)

This command will respond with the number of unacknowledged operation and fault records.

To mark the record as being reported, a 3 6 8 command will retrieve the oldest unreported fault record and decrement the unreported fault record counter by one.

Likewise, a 3 6 9 command will retrieve the oldest unreported operations record and decrement the unreported fault record counter by one.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x04
1/3	Total Number of Messages = 4
2/1	Unreported Fault Record Count byte
2/2	Unreported Operation Record Count byte
2/3	Spare
3/1	Spare
3/2	Spare
3/3	Spare
4/1	Spare
4/2	Spare
4/3	Spare

8.1.5 Reset Alarms/Target LEDs (3 0 5)

The targets, alarms and relay status flag (see command 3 4 1 msg 2/1) will be reset on the relay. After the relay receives this command it will transmit an ACK/NACK based on the completion of the command.

8.1.6 Reset Max/Min Demand Currents (3 0 6)

This command will reset the Max/Min demand current values along with their time tags. After the relay receives this command it will transmit an ACK/NACK based on the completion of the command.

8.1.7 Show logical Input/Ouput Status (3 0 7)

This command displays the binary value of the logical input and output table for the present state of the unit.

Bit = 0, Input Disabled/Output Not Energized.
Bit = 1, Input Enabled/Output Energized.
Outputs denoted with '*' are sealed in until cleared.

8.1.7.1 DPU2000 Logical I/O

DPU2000 Logical Inputs Include: "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", “ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "UDI".

DPU2000 Logical Outputs Include: "TRIP", "CLOSE", "ALARM", “BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "67P", "67N", "81S-1", "81R-1", "81O-1", "27-1P", "59", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA",

"50-1D", "LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "59*", "67P*", "67N*", "81S-1*", "81R-1*", "81O-1*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "ULO1", "ULO2", "ULO3", "ULO4", "ULO5", "ULO6", "ULO7", "ULO8", "ULO9", "81O-2", "81S-2", "81R-2", "81O-2*", "81S-2*", "81R-2*", "CLTA", "PWatt1", "PWatt2", "79CA1*", "79CA2*", "BFA*".

8.1.7.2 DPU2000R Logical I/O

DPU2000R Logical Inputs Include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "EXTBF", "BFI", "UDI", "25"(*Synch Check Model*), "25By"(*Synch Check Model*). The following logical inputs are available in CPU versions greater than 1.92: "LOCAL", "TGT", "SIA". The following logical inputs are available in CPU version greater than 4.02 (2.01 for PTH): “LIS1”, “LIS2 “,“LIS3”, “LIS4 “, “LIS5”, “LIS6 “, “LIS7”, “LIS8“, “LIR1”, “LIR2”, “LIR3”, “LIR4 “, “LIR5”, “LIR6 “, “LIR7”, “LIR8”, “TR_SET”, “TR_RST”.

DPU2000R Logical Outputs Include: "TRIP", "CLOSE", "ALARM", “BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "67P", "67N", "81S-1", "81R-1", "81O-1", "27-1P", "59", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA", "50-1D", "LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "32PA", "32NA", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "59*", "67P*", "67N*", "81S-1*", "81R-1*", "81O-1*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "ULO1", "ULO2", "ULO3", "ULO4", "ULO5", "ULO6", "ULO7", "ULO8", "ULO9", "81O-2", "81S-2", "81R-2", "81O-2*", "81S-2*", "81R-2*", "CLTA", /* V1.40 */ "PWatt1", "PWatt2", "79CA1*", "79CA2*".

The following were added to CPU V1.60: "SEF*"(*Sensitive Earth Model*), "SEF"(*Sensitive Earth Model*), "BZA", "BFT", "ReTrp", "BFT*", "ReTrp*".

The following were added to CPU V1.80: "32P-2", "32N-2", "32P-2*", "32N-2*", "BFA*".

The following were added to CPU V1.93: “25*"(*Synch Check Model*), "25"(*Synch Check Model*), "SBA".

The following were added to CPU V3.20: “79V"and "RClin". The following were added to CPU V4.10 (2.10 for PTH): “59G”,”59G*”, “LO1”, “LO2”,”LO3”,”LO4”,”LO5”,”LO6”,”LO7”,”LO8”, “TR_ON”,”TR_OFF”,”TR_TAG”.

The following were added to CPU V5.0: ”59-3p”, ”59-3p*”, ”47”,”47*”,”21P-1”,”21P-1*”,”21P-2”,”21P-2*”,”21P-3”,”21P-3*”,”21P-4”,”21P-4*”.

The following were added to CPU V5.1: “C1”, “C2”, “C3”, “C4”, “C5”, “C6”,”TRIPT”, “NTA”, “TIMET”, “INSTT”, “NEGSEQT”, “FREQT”, “DIRT”, “VOLTT”, “DISTT”, “SEFT”, “50-3D”.

8.1.7.3 DPU1500R Logical I/O

DPU1500R Logical Inputs Include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "UDI", "LOCAL", "TGT", "SIA".

DPU1500R Logical Outputs Include: "TRIP", "CLOSE", "ALARM", “BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "27-1P", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA", "50-1D","LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "CLTA", "PWatt1", "PWatt2", "79CA1*", "79CA2*", "SEF*"(*Sensitive Earth Model*), "SEF"(*Sensitive Earth Model*), "BZA", "BFA*", "SBA", “79V" and "RClin".

8.1.7.4 Logical I/O Bit Definitions

Byte-Bit	Output	Input	Byte-Bit	Output	Input
1-7	TRIP	52a	2-7	50N2	TCM
1-6	CLOSE	52b	2-6	50P3	50-1
1-5	ALARM	43a	2-5	50N3	50-2
1-4	27	PH3	2-4	51P	50-3

1-3	46	GRD	2-3	51N	ALT1
1-2	50P1	SCC	2-2	59	ALT2
1-1	50N1	79S	2-1	67P	ECI1
1-0	50P2	79M	2-0	67N	ECI2

Byte-Bit	Output	Input	Byte-Bit	Output	Input
3-7	81S-1	WCI	4-7	PUA	ULI2
3-6	81R-1	ZSC	4-6	79LOA	ULI3
3-5	PATA	OPEN	4-5	BFA	ULI4
3-4	PBTA	CLOSE	4-4	PPDA	ULI5
3-3	PCTA	46	4-3	NPDA	ULI6
3-2	TCFA	67P	4-2	BFUA	ULI7
3-1	TCC	67N	4-1	KSI	ULI8
3-0	79DA	ULI1	4-0	79CA-1	ULI9

Byte-Bit	Output	Input	Byte-Bit	Output	Input
5-7	HPFA	CRI	6-7	GRD-D	25By
5-6	LPFA	ARCI	6-6	32PA	LOCAL
5-5	OCTC	TARC	6-5	32NA	TGT
5-4	50-1D	SEF	6-4	27-3P	SIA
5-3	50-2D	EXTBFI	6-3	VarDA	LIS1
5-2	STC	BFI	6-2	79CA-2	LIS2
5-1	ZSC	UDI	6-1	TRIPA	LIS3
5-0	PH3-D	25	6-0	TRIPB	LIS4

Byte-Bit	Output	Input	Byte-Bit	Output	Input
7-7	TRIPC	LIS5	8-7	50N3*	LIR5
7-6	27*	LIS6	8-6	51P*	LIR6
7-5	46*	LIS7	8-5	51N*	LIR7
7-4	50P1*	LIS8	8-4	59*	LIR8
7-3	50N1*	LIR1	8-3	67P*	TR_SET
7-2	50P2*	LIR2	8-2	67N*	TR_RST
7-1	50N2*	LIR3	8-1	81S-1*	ULI10
7-0	50P3*	LIR4	8-0	81R-1*	ULI11

Byte-Bit	Output	Input	Byte-Bit	Output	Input
9-7	81O-1*	ULI12	10-7	ULO4	
9-6	27-3P*	ULI13	10-6	ULO5	
9-5	TRIPA*	ULI14	10-5	ULO6	
9-4	TRIPB*	ULI15	10-4	ULO7	
9-3	TRIPC*	ULI16	10-3	ULO8	
9-2	ULO1	46A TC	10-2	ULO9	
9-1	ULO2		10-1	PVArA	
9-0	ULO3		10-0	NVArA	

Byte-Bit	Output	Input	Byte-Bit	Output	Input
11-7	LOADA		12-7	CLTA	
11-6	81O-1		12-6	PWatt1	
11-5	81O-2		12-5	PWatt2	
11-4	81S-2		12-4	79CA1*	
11-3	81R-2		12-3	79CA2*	
11-2	81O-2*		12-2	SEF*	
11-1	81S-2*		12-1	SEF	
11-0	81R-2*		12-0	BZA	

Byte-Bit	Output	Input	Byte-Bit	Output	Input
13-7	BFT		14-7	BFA*	
13-6	RETRIP		14-6	25*	
13-5	BFT*		14-5	25	

13-4	RETRIP*		14-4	SBA	
13-3	32P-2		14-3	79V	
13-2	32N-2		14-2	RClin	
13-1	32P-2*		14-1	59G	
13-0	32N-2*		14-0	59G*	

Byte-Bit	Output	Input	Byte-Bit	Output	Input
15-7	LO1		16-7	TR_ON	
15-6	LO2		16-6	TR_OFF	
15-5	LO3		16-5	TR_TAG	
15-4	LO4		16-4	59-3ph	
15-3	LO5		16-3	59-3ph*	
15-2	LO6		16-2	47	
15-1	LO7		16-1	47*	
15-0	LO8		16-0	50-3D	

Byte-Bit	Output	Input	Byte-Bit	Output[note1]	Input
17-7	21P-1	not	18-7	not	not
17-6	21P-1*	applicable,	18-6	applicable,	applicable,
17-5	21P-2	no more	18-5	no more	no more
17-4	21P-2*	logical input	18-4	logical input	logical input
17-3	21P-3	bytes are	18-3	bytes are	bytes are
17-2	21P-3*	available.[note 1]	18-2	available[note 1]	available.[note 1]
17-1	21P-4		18-1		
17-0	21P-4*		18-0		

NOTE: SEF and SEF* are available in DPU2000R and DPU1500R Sensitive Earth models only.

Note 1: Do NOT use this command for future expansion of logical outputs or logical inputs. Use the appropriate 3-1-1 command in place of 3-0-7. 3-0-7 will eventually be replaced by command 3-1-1.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x07
1/3	Total Number of Messages = 13
2/1	Logical Output byte1
2/2	Logical Output byte2
2/3	Logical Output byte3
3/1	Logical Output byte4
3/2	Logical Output byte5
3/3	Logical Output byte6
4/1	Logical Output byte7
4/2	Logical Output byte8
4/3	Logical Output byte9
5/1	Logical Output byte10
5/2	Logical Output byte11
5/3	Logical Output byte12
6/1	Logical Output byte13
6/2	Logical Output byte14
6/3	Logical Output byte15
7/1	Logical Output byte16
7/2	Logical Input byte1
7/3	Logical Input byte2
8/1	Logical Input byte3
8/2	Logical Input byte4
8/3	Logical Input byte5
9/1	Logical Input byte6
9/2	Logical Input byte7
9/3	Logical Input byte8

10/1	Logical Input byte9
10/2	Logical Input byte10
10/3	Logical Input byte11
11/1	Logical Input byte12
11/2	Logical Input byte13
11/3	Logical Input byte14
12/1	Logical Input byte15
12/2	Logical Input byte16
12/3	Logical Output byte 17
13/1	Logical Output byte 18
13/2	Checksum High Byte
13/3	Checksum Low Byte

8.1.8 Reset Relay Status (3 0 8)

The relay status flag (see command 3 4 1 msg 2/1) will be reset on the relay. After the relay receives this command it will transmit an ACK/NACK based on the completion of the command.

8.1.9 Clear Records (3 0 9)

- This is reserved for future use for Clear Records -

8.2 Register Data "N" Command (3 1 n)

N	Definition
0	Reserved for repeat 3 1 n
1	Register Based Communication Command
2	Transmit Modbus™ Extended Register Set Command
3	Receive Modbus™ Extended Register Set Command
4	Not Used
5	Not Used
6	Process Modbus™ command

8.2.1 Transmit Register Based Data Set (3 1 1)

NOTE: **The register based command, 3-1-1, is available in DPU2000R and DPU1500R, all block and offset register data refers to DPU2000R and DPU1500R models**.

Data Byte	Definition	
1/1	Block Number	(0-255)
1/2	Offset Number	(0-255)
1/3	Number of Bytes to Retrieve (Num Bytes)	(1-132)

Msg Byte	Definition
1/1	Relay Status Byte Bit 7: Control Power Cycled Bit 6: New Fault Recorded Bit 5: Alternate 2 Settings Active Bit 4: Alternate 1 Settings Active Bit 3: Remote Edit Disable Bit 2: Local Settings Changed Bit 1: Contact Input Chnaged Bit 0: Selftest Status
1/2	Command + Subcommand = 11
1/3	Total Number of Messages (TotalMsg = 1+(Num Bytes/3))
2/1	Data Byte Block Number, Offset Number
2/2	Data Byte Block Number, Offset Number + 1
2/3	Data Byte Block Number, Offset Number + 2
.	.
.	.
.	.
TotalMsg/1	Data Byte Block Number, Offset Number + NumBytes - 3
TotalMsg/2	Data Byte Block Number, Offset Number + NumBytes - 2
TotalMsg/3	Data Byte Block Number, Offset Number + NumBytes - 1

Data Type Definitions	Value Ranges
Unsigned Byte	(0 to 255)
Signed Byte	(-128 to 127)
Unsigned Short	(0 to 65,535)
Signed Short	(-32,768 to 32,767)
Unsigned Long	(0 to 4,294,967,295)
Signed Long	(-2,147,483,648 to 2,147,483,647)

Note: Data Byte Order follows the Low Addres-High Byte, High Address -Low Byte Convention.

8.2.1.1 Register Based Communication Definitions

8.2.1.1.1 BLK 0: SYSTEM STATUS/CONFIGURATION BLOCK

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Word		Relay Status Bit 15-11: Spare Bit 10: New Minimum DemandValue Bit 9: New Peak Demand Value Bit 8: New Operation Recorded Bit 7: Control Power Cycled Bit 6: New Fault Recorded Bit 5: Alternate 2 Settings Active Bit 4: Alternate 1 Settings Active Bit 3: Remote Edit Disable Bit 2: Local Settings Changed Bit 1: Contact Input Changed Bit 0: Selftest Status
Offset 2:	Unsigned Long		Diagnostic Status Flag Bit 31-16: Spare Bit 15: DSP COP FAILURE Bit 14: DSP +5V FAILURE Bit 13: DSP +/-15V FAILURE Bit 12: DSP +/-5V FAILURE Bit 11: DSP ADC FAILURE Bit 10: DSP EXT RAM FAILURE Bit 9: DSP INT RAM FAILURE Bit 8: DSP ROM FAILURE Bit 7: Spare Bit 6: Spare Bit 5: Spare Bit 4: Spare Bit 3: CPU EEPROM FAILURE Bit 2: CPU NVRAM FAILURE Bit 1: CPU EPROM FAILURE Bit 0: CPU RAM FAILURE
Offset 6:	Unsigned Word		Relay Configuration Bit 15-2: Spare Bit 2: 0=V(line-neutral), 1=V(line-line) Bit 1: 0=kWhr/kVarhr, 1=MWhr/MVarhr Bit 0: 0= Wye PT, 1=Delta PT
Offset 8:20	Char String		Catalog Number
Offset 28:	Unsigned Short	100	CPU Software Version Number
Offset 30:	Unsigned Short	10	Analog/DSP Software Version Number
Offset 32:	Unsigned Short	10	Front Panel Controller Software Version Number
Offset 34:	Unsigned Short	10	Auxillary Communication Software Version Number
Offset 36:	Unsigned Long	1	Serial Number
Offset 40:	18 Char String		Unit Name

8.2.1.1.2 BLK 1: RMS LOAD CURRENT/ANGULAR VALUES BLOCK

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Word	1	Load Current-A
Offset 2:	Unsigned Word	1	Load Current-A Angle
Offset 4:	Unsigned Word	1	Load Current-B
Offset 6:	Unsigned Word	1	Load Current-B Angle
Offset 8:	Unsigned Word	1	Load Current-C
Offset 10:	Unsigned Word	1	Load Current-C Angle
Offset 12:	Unsigned Word	1	Load Current-N
Offset 14:	Unsigned Word	1	Load Current-N Angle
Offset 16:	Unsigned Long	1	Voltage VAN
Offset 20:	Unsigned Word	1	Voltage VAN Angle

Offset 22:	Unsigned Long	1	Voltage VBN
Offset 26:	Unsigned Word	1	Voltage VBN Angle
Offset 28:	Unsigned Long	1	Voltage VCN
Offset 32:	Unsigned Word	1	Voltage VCN Angle
Offset 34:	Unsigned Long	1	Voltage VAB
Offset 38:	Unsigned Word	1	Voltage VAB Angle
Offset 40:	Unsigned Long	1	Voltage VBC
Offset 44:	Unsigned Word	1	Voltage VBC Angle
Offset 46:	Unsigned Long	1	Voltage VCA
Offset 50:	Unsigned Word	1	Voltage VCA Angle
Offset 52:	Signed Long	1	kWatts A
Offset 56:	Signed Long	1	kWatts B
Offset 60:	Signed Long	1	kWatts C
Offset 64	Signed Long	1	3 Phase kWatts
Offset 68:	Signed Long	1	kVars A
Offset 72:	Signed Long	1	kVars B
Offset 76:	Signed Long	1	kVars C
Offset 80	Signed Long	1	3 Phase kVars
Offset 84:	Signed Long	1	kWatt Hours A
Offset 88:	Signed Long	1	kWatt Hours B
Offset 92:	Signed Long	1	kWatt Hours C
Offset 96	Signed Long	1	kWatt Hours 3 Phase
Offset 100:	Signed Long	1	kVar Hours A
Offset 104:	Signed Long	1	kVar Hours B
Offset 108:	Signed Long	1	kVar Hours C
Offset 112	Signed Long	1	kVar Hours 3 Phase
Offset 116:	Unsigned Word	1	Load Current Zero Sequence
Offset 118:	Unsigned Word	1	Load Current Zero Sequence Angle
Offset 120:	Unsigned Word	1	Load Current Positive Sequence
Offset 122:	Unsigned Word	1	Load Current Positive Sequence Angle 1
Offset 124:	Unsigned Word	1	Load Current Negative Sequence
Offset 126:	Unsigned Word	1	Load Current Negative Sequence Angle
Offset 128:	Unsigned Long	1	Voltage 1 Magnitude
Offset 132:	Unsigned Word	1	Voltage 1 Angle
Offset 134:	Unsigned Long	1	Voltage 2 Magnitude
Offset 138:	Unsigned Word	1	Voltage 2 Angle
Offset 140:	Unsigned Word	100	System Frequency
Offset 142	Unsigned Word		Power Factor Bit 15-9: Not used Bit 8: 0=Positive, 1=Negative Bit 7: 0=Leading, 1=Lagging Bit 6-0: Power Factor Value (x100)
Offset 144:	Unsigned Long	1	Current Sens Earth Mag
Offset 148:	Unsigned Word	1	Current Sens Earth Angle
Offset 150:	Unsigned Long	1	3V0/Vbus Mag
Offset 154:	Unsigned Word	1	3V0/Vbus Ang
Offset 156:	Signed Word	100	Power Factor
Offset 158:	Unsigned Word		Power Factor Status Bits 15-1: Not used Bit 0: 0=Leading, 1=Lagging
Offset 159:	Unsigned Word	1	Reserved
Offset 160:	Unsigned Word	1	Reserved
Offset 161:	Unsigned Word	1	3V0 Mag (calculated)
Offset 162:	Unsigned Word	1	3V0 Ang (calculated)

8.2.1.1.3 BLK 2: RMS DEMAND CURRENT/REAL and REACTIVE POWER VALUES BLOCK

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Short	1	Demand Current-A
Offset 2:	Unsigned Short	1	Demand Current-B
Offset 4:	Unsigned Short	1	Demand Current-C
Offset 6:	Unsigned Short	1	Demand Current-N
Offset 8:	Signed Long	1	Demand kWatts-A
Offset 12:	Signed Long	1	Demand kWatts-B
Offset 16:	Signed Long	1	Demand kWatts-C
Offset 20:	Signed Long	1	3 Phase Demand Watts
Offset 24:	Signed Long	1	Demand kVars-A
Offset 28:	Signed Long	1	Demand kVars-B
Offset 32:	Signed Long	1	Demand kVars-C
Offset 36:	Signed Long	1	3 Phase Demand Vars

8.2.1.1.4 BLK 3: RMS PEAK DEMAND CURRENT/REAL and REACTIVE POWER VALUES and TIME STAMPS BLOCK

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Word	1	Peak Demand Current-A
Offset 2:	Unsigned Byte		Peak Demand Current-A Year
Offset 3:	Unsigned Byte		Peak Demand Current-A Month
Offset 4:	Unsigned Byte		Peak Demand Current-A Day
Offset 5:	Unsigned Byte		Peak Demand Current-A Hour
Offset 6:	Unsigned Byte		Peak Demand Current-A Minute
Offset 7:	Unsigned Byte		Spare
Offset 8:	Unsigned Word	1	Peak Demand Current-B
Offset 10:	Unsigned Byte		Peak Demand Current-B Year
Offset 11:	Unsigned Byte		Peak Demand Current-B Month
Offset 12:	Unsigned Byte		Peak Demand Current-B Day
Offset 13:	Unsigned Byte		Peak Demand Current-B Hour
Offset 14:	Unsigned Byte		Peak Demand Current-B Minute
Offset 15:	Unsigned Byte		Spare
Offset 16:	Unsigned Word	1	Peak Demand Current-C
Offset 18:	Unsigned Byte		Peak Demand Current-C Year
Offset 19:	Unsigned Byte		Peak Demand Current-C Month
Offset 20:	Unsigned Byte		Peak Demand Current-C Day
Offset 21:	Unsigned Byte		Peak Demand Current-C Hour
Offset 22:	Unsigned Byte		Peak Demand Current-C Minute
Offset 23:	Unsigned Byte		Spare
Offset 24:	Unsigned Word	1	Peak Demand Current-N
Offset 26:	Unsigned Byte		Peak Demand Current-N Year
Offset 27:	Unsigned Byte		Peak Demand Current-N Month
Offset 28:	Unsigned Byte		Peak Demand Current-N Day
Offset 29:	Unsigned Byte		Peak Demand Current-N Hour
Offset 30:	Unsigned Byte		Peak Demand Current-N Minute
Offset 31:	Unsigned Byte		Spare
Offset 32:	Signed Long	1	Peak Demand KWatts-A
Offset 36:	Unsigned Byte		Peak Demand KWatts-A Year
Offset 37:	Unsigned Byte		Peak Demand KWatts-A Month
Offset 38:	Unsigned Byte		Peak Demand KWatts-A Day
Offset 39:	Unsigned Byte		Peak Demand KWatts-A Hour
Offset 40:	Unsigned Byte		Peak Demand KWatts-A Minute
Offset 41:	Unsigned Byte		Spare
Offset 42:	Signed Long	1	Peak Demand KWatts-B
Offset 46:	Unsigned Byte		Peak Demand KWatts-B Year
Offset 47:	Unsigned Byte		Peak Demand KWatts-B Month
Offset 48:	Unsigned Byte		Peak Demand KWatts-B Day
Offset 49:	Unsigned Byte		Peak Demand KWatts-B Hour

Offset 50:	Unsigned Byte		Peak Demand KWatts-B Minute
Offset 51:	Unsigned Byte		Spare
Offset 52:	Signed Long	1	Peak Demand KWatts-C
Offset 56:	Unsigned Byte		Peak Demand KWatts-C Year
Offset 57:	Unsigned Byte		Peak Demand KWatts-C Month
Offset 58:	Unsigned Byte		Peak Demand KWatts-C Day
Offset 59:	Unsigned Byte		Peak Demand KWatts-C Hour
Offset 60:	Unsigned Byte		Peak Demand KWatts-C Minute
Offset 61:	Unsigned Byte		Spare
Offset 62:	Signed Long	1	3 Phase Peak Demand KWatts
Offset 66:	Unsigned Byte		3 Phase Peak Demand KWatts Year
Offset 67:	Unsigned Byte		3 Phase Peak Demand KWatts Month
Offset 68:	Unsigned Byte		3 Phase Peak Demand KWatts Day
Offset 69:	Unsigned Byte		3 Phase Peak Demand KWatts Hour
Offset 70:	Unsigned Byte		3 Phase Peak Demand KWatts Minute
Offset 71:	Unsigned Byte		Spare
Offset 72:	Signed Long	1	Peak Demand KVars-A
Offset 76:	Unsigned Byte		Peak Demand KVars-A Year
Offset 77:	Unsigned Byte		Peak Demand KVars-A Month
Offset 78:	Unsigned Byte		Peak Demand KVars-A Day
Offset 79:	Unsigned Byte		Peak Demand KVars-A Hour
Offset 80:	Unsigned Byte		Peak Demand KVars-A Minute
Offset 81:	Unsigned Byte		Spare
Offset 82:	Signed Long	1	Peak Demand KVars-B
Offset 86:	Unsigned Byte		Peak Demand KVars-B Year
Offset 87:	Unsigned Byte		Peak Demand KVars-B Month
Offset 88:	Unsigned Byte		Peak Demand KVars-B Day
Offset 89:	Unsigned Byte		Peak Demand KVars-B Hour
Offset 90:	Unsigned Byte		Peak Demand KVars-B Minute
Offset 91:	Unsigned Byte		Spare
Offset 92:	Signed Long	1	Peak Demand KVars-C
Offset 96:	Unsigned Byte		Peak Demand KVars-C Year
Offset 97:	Unsigned Byte		Peak Demand KVars-C Month
Offset 98:	Unsigned Byte		Peak Demand KVars-C Day
Offset 99:	Unsigned Byte		Peak Demand KVars-C Hour
Offset 100:	Unsigned Byte		Peak Demand KVars-C Minute
Offset 101:	Unsigned Byte		Spare
Offset 102:	Signed Long	1	3 Phase Peak Demand KVars
Offset 106:	Unsigned Byte		3 Phase Peak Demand KVars Year
Offset 107:	Unsigned Byte		3 Phase Peak Demand KVars Month
Offset 108:	Unsigned Byte		3 Phase Peak Demand KVars Day
Offset 109:	Unsigned Byte		3 Phase Peak Demand KVars Hour
Offset 110	Unsigned Byte		3 Phase Peak Demand KVars Minute
Offset 111:	Unsigned Byte		Spare

8.2.1.1.5 BLK 4: RMS MINIMUM DEMAND CURRENT/REAL and REACTIVE POWER VALUES and TIME STAMPS BLOCK

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Word	1	Minimum Demand Current-A
Offset 2:	Unsigned Byte		Minimum Demand Current-A Year
Offset 3:	Unsigned Byte		Minimum Demand Current-A Month
Offset 4:	Unsigned Byte		Minimum Demand Current-A Day
Offset 5:	Unsigned Byte		Minimum Demand Current-A Hour
Offset 6:	Unsigned Byte		Minimum Demand Current-A Minute
Offset 7:	Unsigned Byte		Spare
Offset 8:	Unsigned Word	1	Minimum Demand Current-B
Offset 10:	Unsigned Byte		Minimum Demand Current-B Year
Offset 11:	Unsigned Byte		Minimum Demand Current-B Month
Offset 12:	Unsigned Byte		Minimum Demand Current-B Day

Offset 13:	Unsigned Byte		Minimum Demand Current-B Hour
Offset 14:	Unsigned Byte		Minimum Demand Current-B Minute
Offset 15:	Unsigned Byte		Spare
Offset 16:	Unsigned Word	1	Minimum Demand Current-C
Offset 18:	Unsigned Byte		Minimum Demand Current-C Year
Offset 19:	Unsigned Byte		Minimum Demand Current-C Month
Offset 20:	Unsigned Byte		Minimum Demand Current-C Day
Offset 21:	Unsigned Byte		Minimum Demand Current-C Hour
Offset 22:	Unsigned Byte		Minimum Demand Current-C Minute
Offset 23:	Unsigned Byte		Spare
Offset 24:	Unsigned Word	1	Minimum Demand Current-N
Offset 26:	Unsigned Byte		Minimum Demand Current-N Year
Offset 27:	Unsigned Byte		Minimum Demand Current-N Month
Offset 28:	Unsigned Byte		Minimum Demand Current-N Day
Offset 29:	Unsigned Byte		Minimum Demand Current-N Hour
Offset 30:	Unsigned Byte		Minimum Demand Current-N Minute
Offset 31:	Unsigned Byte		Spare
Offset 32:	Signed Long	1	Minimum Demand KWatts-A
Offset 36:	Unsigned Byte		Minimum Demand KWatts-A Year
Offset 37:	Unsigned Byte		Minimum Demand KWatts-A Month
Offset 38:	Unsigned Byte		Minimum Demand KWatts-A Day
Offset 39:	Unsigned Byte		Minimum Demand KWatts-A Hour
Offset 40:	Unsigned Byte		Minimum Demand KWatts-A Minute
Offset 41:	Unsigned Byte		Spare
Offset 42	Signed Long	1	Minimum Demand KWatts-B
Offset 46:	Unsigned Byte		Minimum Demand KWatts-B Year
Offset 47:	Unsigned Byte		Minimum Demand KWatts-B Month
Offset 48:	Unsigned Byte		Minimum Demand KWatts-B Day
Offset 49:	Unsigned Byte		Minimum Demand KWatts-B Hour
Offset 50:	Unsigned Byte		Minimum Demand KWatts-B Minute
Offset 51:	Unsigned Byte		Spare
Offset 52:	Signed Long	1	Minimum Demand KWatts-C
Offset 56:	Unsigned Byte		Minimum Demand KWatts-C Year
Offset 57:	Unsigned Byte		Minimum Demand KWatts-C Month
Offset 58:	Unsigned Byte		Minimum Demand KWatts-C Day
Offset 59:	Unsigned Byte		Minimum Demand KWatts-C Hour
Offset 60:	Unsigned Byte		Minimum Demand KWatts-C Minute
Offset 61:	Unsigned Byte		Spare
Offset 62:	Signed Long	1	3 Phase Minimum Demand KWatts
Offset 66:	Unsigned Byte		3 Phase Minimum Demand KWatts Year
Offset 67:	Unsigned Byte		3 Phase Minimum Demand KWatts Month
Offset 68:	Unsigned Byte		3 Phase Minimum Demand KWatts Day
Offset 69:	Unsigned Byte		3 Phase Minimum Demand KWatts Hour
Offset 70:	Unsigned Byte		3 Phase Minimum Demand KWatts Minute
Offset 71:	Unsigned Byte		Spare
Offset 72:	Signed Long	1	Minimum Demand KVars-A
Offset 76:	Unsigned Byte		Minimum Demand KVars-A Year
Offset 77:	Unsigned Byte		Minimum Demand KVars-A Month
Offset 78:	Unsigned Byte		Minimum Demand KVars-A Day
Offset 79:	Unsigned Byte		Minimum Demand KVars-A Hour
Offset 80:	Unsigned Byte		Minimum Demand KVars-A Minute
Offset 81:	Unsigned Byte		Spare
Offset 82:	Signed Long	1	Minimum Demand KVars-B
Offset 86:	Unsigned Byte		Minimum Demand KVars-B Year
Offset 87:	Unsigned Byte		Minimum Demand KVars-B Month
Offset 88:	Unsigned Byte		Minimum Demand KVars-B Day
Offset 89:	Unsigned Byte		Minimum Demand KVars-B Hour
Offset 90:	Unsigned Byte		Minimum Demand KVars-B Minute
Offset 91:	Unsigned Byte		Spare

Offset 92:	Signed Long	1	Minimum Demand KVars-C
Offset 96:	Unsigned Byte		Minimum Demand KVars-C Year
Offset 97:	Unsigned Byte		Minimum Demand KVars-C Month
Offset 98:	Unsigned Byte		Minimum Demand KVars-C Day
Offset 99:	Unsigned Byte		Minimum Demand KVars-C Hour
Offset 100:	Unsigned Byte		Minimum Demand KVars-C Minute
Offset 101:	Unsigned Byte		Spare
Offset 102:	Signed Long	1	3 Phase Minimum Demand KVars
Offset 106:	Unsigned Byte		3 Phase Minimum Demand KVars Year
Offset 107:	Unsigned Byte		3 Phase Minimum Demand KVars Month
Offset 108:	Unsigned Byte		3 Phase Minimum Demand KVars Day
Offset 109:	Unsigned Byte		3 Phase Minimum Demand KVars Hour
Offset 110:	Unsigned Byte		3 Phase Minimum Demand KVars Minute
Offset 111:	Unsigned Byte		Spare

8.2.1.1.6 BLK 5: COUNTERS BLOCK

Overcurrent Trip Counters A, B, C, and N are available in DPU2000R with Recloser Curve Software option, catalog numbers XXXXXXXX-XXX2X or XXXXXXXX-XXX3X.

Block Offset	Data Size	Scale	Description
Offset 0:	Unsigned Short	1	Operations Counter
Offset 2:	Unsigned Short	1	Fault Counter
Offset 4:	Unsigned Short	1	Sum of Fault Currents, A
Offset 6:	Unsigned Short	1	Sum of Fault Currents, B
Offset 8:	Unsigned Short	1	Sum of Fault Currents, C
Offset 10:	Unsigned Short	1	Overcurrent Trip Counter
Offset 12:	Unsigned Short	1	Breaker Operations Counter
Offset 14:	Unsigned Short	1	Recloser Counter 1
Offset 16:	Unsigned Short	1	Stage 1 Reclose Counter
Offset 18:	Unsigned Short	1	Stage 2 Reclose Counter
Offset 20:	Unsigned Short	1	Stage 3 Reclose Counter
Offset 22:	Unsigned Short	1	Stage 4 Reclose Counter
Offset 24:	Unsigned Short	1	Recloser Counter 2
Offset 26:	Unsigned Short	1	Overcurrent Trip Counter A
Offset 28:	Unsigned Short	1	Overcurrent Trip Counter B
Offset 30:	Unsigned Short	1	Overcurrent Trip Counter C
Offset 32:	Unsigned Short	1	Overcurrent Trip Counter D

8.2.1.1.7 BLK 6: PHYSICAL and LOGICAL INPUT/OUTPUT BLOCK

Block Offset	Data Size	Description				
Offset 0:	Unsigned Long	Logical Output 0-31				
			Bit 31:	TRIP	Bit 15:	81S (2000R)
			Bit 30:	CLOSE	Bit 14:	81R (2000R)
			Bit 29:	ALARM	Bit 13:	PATA
			Bit 28:	27-1P	Bit 12:	PBTA
			Bit 27:	46	Bit 11:	PCTA
			Bit 26:	50P-1	Bit 10:	TCFA
			Bit 25:	50N-1	Bit 9:	TCC
			Bit 24:	50P-2	Bit 8:	79DA
			Bit 23:	50N-2	Bit 7:	PUA
			Bit 22:	50P-3	Bit 6:	79LOA
			Bit 21:	50N-3	Bit 5:	BFA
			Bit 20:	51P	Bit 4:	PPDA
			Bit 19:	51N	Bit 3:	NPDA
			Bit 18:	59 (2000R)	Bit 2:	BFUA
			Bit 17:	67P (2000R)	Bit 1:	KSI
			Bit 16:	67N (2000R)	Bit 0:	79CA
Offset 4:	Unsigned Long	Logical Output 32-63				
			Bit 31:	HPFA	Bit 15:	TRIPC
			Bit 30:	LPFA	Bit 14:	27-1P*
			Bit 29:	OCTC	Bit 13:	46*

			Bit 28:	50-1D	Bit 12:	50P-1*
			Bit 27:	50-2D	Bit 11:	50N-1*
			Bit 26:	STC	Bit 10:	50P-2*
			Bit 25:	ZSC	Bit 9:	50N-2*
			Bit 24:	PH3-D	Bit 8:	50P-3*
			Bit 23:	GRD-D	Bit 7:	50N-3*
			Bit 22:	32PA (2000R)	Bit 6:	51P*
			Bit 21:	32NA (2000R)	Bit 5:	51N*
			Bit 20:	27-3P	Bit 4:	59* (2000R)
			Bit 19:	VarDA	Bit 3:	67P* (2000R)
			Bit 18:	79CA-2	Bit 2:	67N* (2000R)
			Bit 17:	TRIPA	Bit 1:	81S1* (2000R)
			Bit 16:	TRIPB	Bit 0:	81R1* (2000R)
Offset 8:	Unsigned Long	Logical Output 64-95				
			Bit 31:	81O1* (2000R)	Bit 15:	LOADA
			Bit 30:	27-3P*	Bit 14:	81O1 (2000R)
			Bit 29:	TRIPA*	Bit 13:	81O2 (2000R)
			Bit 28:	TRIPB*	Bit 12:	81S2 (2000R)
			Bit 27:	TRIPC*	Bit 11:	81R2 (2000R)
			Bit 26:	ULO1 (2000R)	Bit 10:	81O2 (2000R)
			Bit 25:	ULO2 (2000R)	Bit 9:	81S2 (2000R)
			Bit 24:	ULO3 (2000R)	Bit 8:	81R2 (2000R)
			Bit 23:	ULO4 (2000R)	Bit 7:	CLTA
			Bit 22:	ULO5 (2000R)	Bit 6:	Watt1
			Bit 21:	ULO6 (2000R)	Bit 5:	Watt2
			Bit 20:	ULO7 (2000R)	Bit 4:	79CA*
			Bit 19:	ULO8 (2000R)	Bit 3:	79CA-2*
			Bit 18:	ULO9 (2000R)	Bit 2:	SEF*
			Bit 17:	PVArA	Bit 1:	SEF
		Bit 16:	NVArA		Bit 0:	BZA w/out SEF
Offset 12:	Unsigned Long	Logical Output 96-127				
			Bit 31:	BFT (2000R)	Bit 15:	LO1
			Bit 30:	ReTrip (2000R)	Bit 14:	LO2
			Bit 29:	BFT* (2000R)	Bit 13:	LO3
			Bit 28:	ReTrip* (2000R)	Bit 12:	LO4
			Bit 27:	32P-2 (2000R)	Bit 11:	LO5
			Bit 26:	32N-2 (2000R)	Bit 10:	LO6
			Bit 25:	32P-2* (2000R)	Bit 9:	LO7
			Bit 24:	32N-2* (2000R)	Bit 8:	LO8
			Bit 23:	BFA*	Bit 7:	TR_ON
			Bit 22:	25* (2000R)	Bit 6:	TR_OFF
			Bit 21:	25 (2000R)	Bit 5:	TR_TAG
			Bit 20:	SBA	Bit 4:	59-3p (DPU2000R)
			Bit 19:	79V	Bit 3:	59-3p* (DPU2000R)
			Bit 18:	RClin	Bit 2:	47 (DPU2000R)
			Bit 17:	59G	Bit 1:	47* (DPU2000R)
			Bit 16:	59G*	Bit 0:	50-3D
Offset 16:	Unsigned Long	Logical Input 0-31				
			Bit 31:	52a	Bit 15:	WCI
			Bit 30:	52b	Bit 14:	ZSC
			Bit 29:	43a	Bit 13:	OPEN
			Bit 28:	PH3	Bit 12:	CLOSE
			Bit 27:	GRD	Bit 11:	46
			Bit 26:	SCC	Bit 10:	67P (2000R)
			Bit 25:	79s	Bit 9:	67N (2000R)
			Bit 24:	79m	Bit 8:	ULI1 (2000R)
			Bit 23:	TCM	Bit 7:	ULI2 (2000R)
			Bit 22:	50-1	Bit 6:	ULI3 (2000R)
			Bit 21:	50-2	Bit 5:	ULI4 (2000R)

			Bit 20:	50-3	Bit 4:	ULI5 (2000R)
			Bit 19:	ALT1	Bit 3:	ULI6 (2000R)
			Bit 18:	ALT2	Bit 2:	ULI7 (2000R)
			Bit 17:	ECI1	Bit 1:	ULI8 (2000R)
			Bit 16:	ECI2	Bit 0:	ULI9 (2000R)
Offset 20:	Unsigned Long	Logical Input 32-63				
			Bit 31:	CRI	Bit 15:	LIS5(2000R)
			Bit 30:	ARCI	Bit 14:	LIS6(2000R)
			Bit 29:	TARC	Bit 13:	LIS7(2000R)
			Bit 28:	SEF TC	Bit 12:	LIS8(2000R)
			Bit 27:	EXTBFI (2000R)	Bit 11:	LIR1(2000R)
			Bit 26:	BFI (2000R)	Bit 10:	LIR2(2000R)
			Bit 25:	UDI	Bit 9:	LIR3(2000R)
			Bit 24:	25 (2000R)	Bit 8:	LIR4(2000R)
			Bit 23:	25By (2000R)	Bit 7:	LIR5(2000R)
			Bit 22:	LOCAL	Bit 6:	LIR6(2000R)
			Bit 21:	TGT	Bit 5:	LIR7(2000R)
			Bit 20:	SIA	Bit 4:	LIR8(2000R)
			Bit 19:	LIS1(2000R)	Bit 3:	TR_SET(2000R)
			Bit 18:	LIS2(2000R)	Bit 2:	TR_RST(2000R)
			Bit 17:	LIS3(2000R)	Bit 1:	
			Bit 16:	LIS4(2000R)	Bit 0:	
Offset 24:	Unsigned Long	Logical Input 64-95 (Reserved)				
Offset 28:	Unsigned Long	Logical Input 96-127 (Reserved)				
Offset 32:	Unsigned Short	Physical Output				
			Bit 15:	Reserved	Bit 7:	OUT6
			Bit 14:	Reserved	Bit 6:	OUT5
			Bit 13:	Reserved	Bit 5:	OUT4
			Bit 12:	Reserved	Bit 4:	OUT3
			Bit 11:	Reserved	Bit 3:	OUT2
			Bit 10:	Reserved	Bit 2:	OUT1
			Bit 9:	Reserved	Bit 1:	CLOSE (Reserved)
			Bit 8:	Reserved	Bit 0:	TRIP
Offset 34:	Unsigned Short	Physical Input				
			Bit 15:	Reserved	Bit 7:	IN5
			Bit 14:	Reserved	Bit 6:	IN4
			Bit 13:	Reserved	Bit 5:	IN3
			Bit 12:	Reserved	Bit 4:	IN2
			Bit 11:	Reserved	Bit 3:	IN1
			Bit 10:	IN8 (2000R) IN6 (1500R)	Bit 2:	Reserved
			Bit 9:	IN7 (2000R)	Bit 1:	Reserved
			Bit 8:	IN6 (2000R)	Bit 0:	Reserved
Offset 36:	Unsigned Short	Forced Physical Inputs Normal State Mask 0=Normal state, 1=Normal state override or return to Normal state				
			Bit 15:	Reserved	Bit 7:	IN5
			Bit 14:	Reserved	Bit 6:	IN4
			Bit 13:	Reserved	Bit 5:	IN3
			Bit 12:	Reserved	Bit 4:	IN2
			Bit 11:	Reserved	Bit 3:	IN1
			Bit 10:	IN8 (2000R) IN6 (1500R)	Bit 2:	Reserved
			Bit 9:	IN7 (2000R)	Bit 1:	Reserved
			Bit 8:	IN6 (2000R)	Bit 0:	Reserved
Offset 38:	Unsigned Short	Forced Physical Inputs Forcing State Mask If Forced Physical Inputs Normal State Mask bit is set then 0=Forcing Reset state or Open, 1=Forcing Set state or Close				
			Bit 15:	Reserved	Bit 7:	IN5
			Bit 14:	Reserved	Bit 6:	IN4

	Bit 13:	Reserved	Bit 5:	IN3
	Bit 12:	Reserved	Bit 4:	IN2
	Bit 11:	Reserved	Bit 3:	IN1
	Bit 10:	IN8 (2000R) IN6 (1500R)	Bit 2:	Reserved
	Bit 9:	IN7 (2000R)	Bit 1:	Reserved
Bit 8:	IN6 (2000R)	Bit 0:	Reserved	

Offsets 36 and 38, two 16 bit words, Forced Physical Inputs Normal State mask and Forced Physical Inputs Forcing State mask, indicate which inputs to force and the state to which they are being forced. If the bit specific to an input is reset in the Normal State mask then all input operations for that input will proceed according to normal logical conditions. If the Normal State mask bit specific to an input is set then all input operations for that input will be ignored and the Forcing State mask will be utilized to force the input condition indicated by the Forcing State mask.

Offset 40: Unsigned Short Forced Physical Outputs Normal State Mask
0=Normal state, 1=Normal state override or return to Normal state

Bit 15:	Spare	Bit 7:	OUT6
Bit 14:	Spare	Bit 6:	OUT5
Bit 13:	Spare	Bit 5:	OUT4
Bit 12:	Spare	Bit 4:	OUT3
Bit 11:	Spare	Bit 3:	OUT2
Bit 10:	Spare	Bit 2:	OUT1
Bit 9:	Reserved	Bit 1:	CLOSE (Reserved)
Bit 8:	Reserved	Bit 0:	TRIP

Offset 42: Unsigned Short Forced Physical Outputs Forcing State Mask
If Forced Physical Outputs Normal State Mask bit is set then
0=Forcing Reset state or De-Assert, 1=Forcing Set state or Assert

Bit 15:	Spare	Bit 7:	OUT6
Bit 14:	Spare	Bit 6:	OUT5
Bit 13:	Spare	Bit 5:	OUT4
Bit 12:	Spare	Bit 4:	OUT3
Bit 11:	Spare	Bit 3:	OUT2
Bit 10:	Spare	Bit 2:	OUT1
Bit 9:	Reserved	Bit 1:	CLOSE (Reserved)
Bit 8:	Reserved	Bit 0:	TRIP

Offsets 40 and 42, two 16 bit words, Forced Physical Outputs Normal State mask and Forced Physical Outputs Forcing State mask, indicate which outputs to force and the state to which they are being forced. If the bit specific to an output is reset in the Normal State mask then all output operations for that output will proceed according to normal logical conditions. If the Normal State mask bit specific to an output is set then all output operations for that output will be ignored and the Forcing State mask will be utilized to force the output condition indicated by the Forcing State mask.

Offset 44: Unsigned Long Forced Logical Inputs Normal State Mask
0=Normal state, 1=Normal state override or return to Normal state

Bit 31:	FLI31	Bit 15:	FLI15
Bit 30:	FLI30	Bit 14:	FLI14
Bit 29:	FLI29	Bit 13:	FLI13
Bit 28:	FLI28	Bit 12:	FLI12
Bit 27:	FLI27	Bit 11:	FLI11
Bit 26:	FLI26	Bit 10:	FLI10
Bit 25:	FLI25	Bit 9:	FLI09
Bit 24:	FLI24	Bit 8:	FLI08
Bit 23:	FLI23	Bit 7:	FLI07
Bit 22:	FLI22	Bit 6:	FLI06
Bit 21:	FLI21	Bit 5:	FLI05
Bit 20:	FLI20	Bit 4:	FLI04
Bit 19:	FLI19	Bit 3:	FLI03
Bit 18:	FLI18	Bit 2:	FLI02
Bit 17:	FLI17	Bit 1:	FLI01
Bit 16:	FLI16	Bit 0:	FLI00

Offset 48:	Unsigned Long	Forced Logical Inputs Forcing State Mask			
		If Forced Logical Inputs Normal State Mask bit is set then			
		0=Forcing Reset state or Open, 1=Forcing Set state or Close			
		Bit 31:	FLI31	Bit 15:	FLI15
		Bit 30:	FLI30	Bit 14:	FLI14
		Bit 29:	FLI29	Bit 13:	FLI13
		Bit 28:	FLI28	Bit 12:	FLI12
		Bit 27:	FLI27	Bit 11:	FLI11
		Bit 26:	FLI26	Bit 10:	FLI10
		Bit 25:	FLI25	Bit 9:	FLI09
		Bit 24:	FLI24	Bit 8:	FLI08
		Bit 23:	FLI23	Bit 7:	FLI07
		Bit 22:	FLI22	Bit 6:	FLI06
		Bit 21:	FLI21	Bit 5:	FLI05
		Bit 20:	FLI20	Bit 4:	FLI04
		Bit 19:	FLI19	Bit 3:	FLI03
		Bit 18:	FLI18	Bit 2:	FLI02
		Bit 17:	FLI17	Bit 1:	FLI01
		Bit 16:	FLI16	Bit 0:	FLI00

Offsets 44 and 48, four 32 bit words, the Forced Logical Inputs Normal State mask and Forced Logical Inputs Forcing State mask, indicate which inputs to force and the state to which they are being forced. If the bit specific to an input is reset in the Normal State masks then all input operations for that input will proceed according to normal logical conditions. If the Normal State mask bit specific to an input is set in the Normal State masks then all input operations for that input will be ignored and the Forcing State mask will be utilized to force the input condition indicated by the Forcing State mask.

Offset 52:	Unsigned Long	Logical Output 128 – 159 (DPU2000R only, out_stat_4)			
		Bit 31:	21P-1	Bit 15:	TimeT
		Bit 30:	21P-1*	Bit 14:	InstT
		Bit 29:	21P-2	Bit 13:	NegSeqT
		Bit 28:	21P-2*	Bit 12:	FreqT
		Bit 27:	21P-3	Bit 11:	DirT
		Bit 26:	21P-3*	Bit 10:	VoltT
		Bit 25:	21P-4	Bit 9:	DistT
		Bit 24:	21P-4*	Bit 8:	SEFT
		Bit 23:	C1	Bit 7:	ULO 10
		Bit 22:	C2	Bit 6:	ULO 11
		Bit 21:	C3	Bit 5:	ULO 12
		Bit 20:	C4	Bit 4:	ULO 13
		Bit 19:	C5	Bit 3:	ULO 14
		Bit 18:	C6	Bit 2:	ULO 15
		Bit 17:	TripT	Bit 1:	ULO 16
		Bit 16:	NTA	Bit 0:	HBHL
Offset 56:	Unsigned Long	Logical Output 160 – 191 (DPU2000R only, out_stat_5)			
		Bit 31:	HBDL	Bit 15:	
		Bit 30:	DBHL	Bit 14:	
		Bit 29:	DBDL	Bit 13:	
		Bit 28:	46A	Bit 12:	
		Bit 27:	46A*	Bit 11:	
		Bit 26:	REMOTE_D	Bit 10:	
		Bit 25:		Bit 9:	
		Bit 24:		Bit 8:	
		Bit 23:		Bit 7:	
		Bit 22:		Bit 6:	
		Bit 21:		Bit 5:	
		Bit 20:		Bit 4:	
		Bit 19:		Bit 3:	
		Bit 18:		Bit 2:	
		Bit 17:		Bit 1:	

Bit 16: Bit 0:

8.2.2 Transmit Modbus ™ Extended Register Set Command (3 1 2)

NOTE: The Modbus™ register based command, 3-1-2, is available in DPU2000R series, CPU V1.80 and above and DPU1500R. See Modbus/Modbus Plus Protocol Document for 6X Register Definitions.

Data Byte	Definition
1/1	Address High Byte (Use 6XXXX-60000)
1/2	Address Low Byte
1/3	Number of **WORDS** (2 byte quantities) to Retrieve (1-65)

Msg Byte	Definition
1/1	Relay Status Byte Bit 7: Control Power Cycled Bit 6: New Fault Recorded Bit 5: Alternate 2 Settings Active Bit 4: Alternate 1 Settings Active Bit 3: Remote Edit Disable Bit 2: Local Settings Changed Bit 1: Contact Input Chnaged Bit 0: Selftest Status
1/2	Command + Subcommand = 12
1/3	Total Number of Messages
2/1	Data Word 0 High Byte
2/2	Data Word 0 Low Byte
2/3	Data Word 1 High Byte
3/1	Data Word 1 Low Byte
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.	.
.	.
TotalMsg/1	Data Word n Low Byte (or could be spare used to fill out last message)
TotalMsg/2	Checksum High Byte
TotalMsg/3	Checksum Low Byte

8.2.3 Receive Modbus ™ Extended Register Set Command (3 1 3)

NOTE: The Modbus™ register based command, 3-1-2, is available in DPU2000R series, CPU V1.80 and above and DPU1500R. See Modbus/Modbus Plus Protocol Document for 6X Register Definitions.

Data Byte	Definition
1/1	Address High Byte (Use 6XXXX-60000)
1/2	Address Low Byte
1/3	Number of **WORDS** (2 byte quantities) to Write (1-65)
2/1	Data Word 0 High Byte
2/2	Data Word 0 Low Byte
2/3	Data Word 1 High Byte
3/1	Data Word 1 Low Byte
.	.
.	.
.	.
TotalMsg/1	Data Word n Low Byte (or could be spare used to fill out last message)
TotalMsg/2	Checksum High Byte
TotalMsg/3	Checksum Low Byte

8.2.4 Receive Modbus ™ Extended Register Set Command (3 1 6)

NOTE: The Modbus™ register based command, 3-1-2, is available in DPU2000R series, CPU V1.80 and above and DPU1500R. See Modbus/Modbus Plus Protocol Document for 6X Register Definitions.

Data Byte	Definition
1/1	Number of messages, starting from message 2 on.
1/2	0
1/3	0
2/1	Modbus RTU Query 1st byte
2/2	Modbus RTU Query 2nd byte
2/3	Modbus RTU Query 3rd byte
3/1	Modbus RTU Query ….
.	.
.	.
.	.
TotalMsg/1	Modbus RTU Query Last byte – CRC Hi
TotalMsg/2	Checksum High Byte
TotalMsg/3	Checksum Low Byte

Note: the total Number of bytes sent must be a multiple of 3. If the 'Checksum Low Byte' does not fall into TotalMsg/3 then fill in with 0 until you get to TotalMsg/3. Ex if 'Checksum Low Byte' falls into TotalMsg/1 then TotalMsg/2 and TotalMsg/3 would each be set to 0. Any Modbus™ query that is supported in the Modbus™ protocol document for the DPU2000R can be sent using this INCOM command.

8.3 Transmit Buffer "33N" Commands (3 3 n)

N	Definition
0	Reserved for repeat 3 3 n
1	Communications Settings
2	Counter Settings
3	Master Trip Output Assignment
4	Breaker Fail Settings

8.3.1 Transmit Communications Settings (3 3 1)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Port configuration byte
- bit 0-3 = port baud rate
  - where 0 = 300, 1 = 1200, 2 = 2400, 3 = 4800, 4 = 9600, 5 = 19200, 6 = 38400
- bit 4-5 = parity (0=None, 1=Odd, 2=Even)
- bit 6 = number of data bits (0=seven,1=eight)

bit 7 = number of stop bits (0=one,1=two)

Valid Frame Combinations: EVEN 7 1, ODD 7 1, NONE 8 1, EVEN 8 1, ODD 8 1, NONE 8 2, NONE 7 2

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x31
1/3	Total Number of Messages = 9
2/1	Unit Address high byte
2/2	Unit Address low byte
2/3	Front Panel RS232 configuration byte
3/1	Rear Panel RS232 or INCOM configuration byte
3/2	Rear Panel RS485 configuration byte
3/3	Rear Panel IRIG byte 0=Disable; 1=Enable-cc, time stamp HH:MM:SS.cc; 2=Enable-mmm, time stamp HH:MM:SS.mmm
4/1	Spare
4/2	Spare

4/3	Aux Port Parameter 1 byte (0-255)
5/1	Aux Port Parameter 2 byte (0-255)
5/2	Aux Port Parameter 3 byte (0-255)
5/3	Aux Port Parameter 4 byte (0-255)
6/1	Aux Port Parameter 5 byte (0-255)
6/2	Aux Port Parameter 6 byte (0-255)
6/3	Aux Port Parameter 7 byte (0-255)
7/1	Aux Port Parameter 8 byte (0-255)
7/2	Aux Port Parameter 9 byte (0-255)
7/3	Aux Port Parameter 10 byte (0-255)
8/1	Aux Port Parameter Mode byte (0-255)
	Bit 0: Par Mode 1 (0=Disable, 1=Enable)
	Bit 1: Par Mode 2 (0=Disable, 1=Enable)
	Bit 2: Par Mode 3 (0=Disable, 1=Enable)
	Bit 3: Par Mode 4 (0=Disable, 1=Enable)
	Bit 4: Par Mode 5 (0=Disable, 1=Enable)
	Bit 5: Par Mode 6 (0=Disable, 1=Enable)
	Bit 6: Par Mode 7 (0=Disable, 1=Enable)
	Bit 7: Par Mode 8 (0=Disable, 1=Enable)
8/2	Spare
8/3	Spare
9/1	Spare
9/2	Checksum high byte
9/3	Checksum low byte

8.3.2 Transmit Counter Settings (3 3 2)

NOTE: Overcurrent Trip Counters A, B, C, and N are available with Recloser Curve Software option, catalog numbers XXXXXXXX-XXX2X or XXXXXXXX-XXX3X. In DPU2000 series, CPU V1.41 or higher is required for the Recloser Curve Software option.

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x32
1/3	Total Number of Messages = 15
2/1	KSI Sum A Counter high byte (0-9999)
2/2	KSI Sum A Counter low byte
2/3	KSI Sum B Counter high byte (0-9999)
3/1	KSI Sum B Counter low byte
3/2	KSI Sum C Counter high byte (0-9999)
3/3	KSI Sum C Counter low byte
4/1	Over Current Trip Counter high byte (0-9999)
4/2	Over Current Trip Counter low byte
4/3	Breaker Operations Counter high byte (0-9999)
5/1	Breaker Operations Counter low byte
5/2	Reclose Counter 1 high byte (0-9999)
5/3	Reclose Counter 1 low byte
6/1	1st Reclose Counter high byte (0-9999)
6/2	1st Reclose Counter low byte
6/3	2nd Reclose Counter high byte (0-9999)
7/1	2nd Reclose Counter low byte
7/2	3rd Reclose Counter high byte (0-9999)
7/3	3rd Reclose Counter low byte
8/1	4th Reclose Counter high byte (0-9999)
8/2	4th Reclose Counter low byte
8/3	Reclose Counter 2 high byte (0-9999)
9/1	Reclose Counter 2 low byte

9/2	Overcurrent Trip A Counter high byte (0-9999), (DPU2000/R)
9/3	Overcurrent Trip A Counter low byte
10/1	Overcurrent Trip B Counter high byte (0-9999) , (DPU2000/R)
10/2	Overcurrent Trip B Counter low byte
10/3	Overcurrent Trip C Counter high byte (0-9999) , (DPU2000/R)
11/1	Overcurrent Trip C Counter low byte
11/2	Overcurrent Trip N Counter high byte (0-9999) , (DPU2000/R)
11/3	Overcurrent Trip N Counter low byte
12/1	SPARE
12/2	SPARE
12/3	SPARE
13/1	SPARE
13/2	SPARE
13/3	SPARE
14/1	SPARE
14/2	SPARE
14/3	SPARE
15/1	SPARE
15/2	Checksum high byte
15/3	Checksum low byte

8.3.3 Transmit Master Trip Output Assignment (3 3 3)

NOTE: In DPU2000 series, CPU V1.70 or higher is required.

Msg/Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x33
1/3	Total Number of Messages = 5
2/1	Master Trip Assignment, Byte 1
	Bit 0: SPARE
	Bit 1: SPARE
	Bit 2: SPARE
	Bit 3: SPARE
	Bit 4: SPARE
	Bit 5: SPARE
	Bit 6: SPARE
	Bit 7: SPARE
2/2	Master Trip Assignment, Byte 2
	Bit 0: SPARE
	Bit 1: SPARE
	Bit 2: SPARE
	Bit 3: SPARE
	Bit 4: SPARE
	Bit 5: SPARE
	Bit 6: SPARE
	Bit 7: SPARE
2/3	Master Trip Assignment, Byte 3
	Bit 0: 67P (DPU2000 and DPU2000R)
	Bit 1: 67N (DPU2000 and DPU2000R)
	Bit 2: 46
	Bit 3: SPARE
	Bit 4: SPARE
	Bit 5: SPARE
	Bit 6: SPARE
	Bit 7: SPARE
3/1	Master Trip Assignment, Byte 4
	Bit 0: 50N-1
	Bit 1: 50N-2
	Bit 2: 50N-3

Bit 3: 51N
Bit 4: 50P-1
Bit 5: 50P-2
Bit 6: 50P-3
Bit 7: 51P

3/2	Spare
3/3	Spare
4/1	Spare
4/2	Spare
4/3	Spare
5/1	Spare
5/2	Checksum, high byte
5/3	Checksum, low byte

8.3.4 Transmit Breaker Fail Settings (3 3 4)

NOTE: In DPU2000 series, CPU V1.70 or higher is required. This command is NOT available in the DPU1500R series.

Msg/Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x34
1/3	Total Number of Messages = 7
2/1	Enable (1=ON, 0=OFF)
2/2	BFT Pickup Time Delay (high byte) (0.00 to 10.00 sec. In 0.01 sec. Steps)
2/3	BFT Pickup Time Delay (low byte)
3/1	BFT Drop Time Delay (0.0 to 10.0 cycles in 0.25 steps)
3/2	BFT Starters Bit 0: External input Bit 1: Phase Level Detector Bit 2: Neutral Level Detector
3/3	ReTrip Pickup Time Delay (high byte) (0.00 to 10.00 sec. In 0.01 sec. Steps)
4/1	ReTrip Pickup Time Delay (low byte)
4/2	ReTrip Drop Time Delay (0.0 to 10.0 cycles in 0.25 steps)
4/3	ReTrip Starters Bit 0: External input Bit 1: Phase Level Detector Bit 2: Neutral Level Detector
5/1	Phase Level Detector Pickup (5 to 100% of 51P in 5% steps)
5/2	Neutral Level Detector Pickup (5 to 100% of 51N in 5% steps)
5/3	Spare
6/1	Spare
6/2	Spare
6/3	Spare
7/1	Spare
7/2	Checksum, high byte
7/3	Checksum, low byte

8.4 Transmit Buffer "3-4-N" Commands (3 4 n)

N	Definition
0	Reserved for repeat 3 4 n
1	Input Select and Index Tables
2	Programmable Input Negated AND Table
3	Programmable Input AND/OR Table
4	Programmable Input User Defined Input Names
5	Programmable Output Select Table
6	Programmable Output AND/OR Table
7	Programmable Output User Defined Output Strings
8	Primary Relay Settings
9	Alternate 1 Relay Settings
10	Alternate 2 Relay Settings
11	Configuration Settings
12	Counter Settings
13	Alarm Settings
14	Real Time Clock
15	Programmable Output Delays

8.4.1 Transmit Programmable Input Select and Index (3 4 1)

Bit Position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	C6	C5	C4	C3	C2	C1
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit Position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPU2000:	IN12	IN13	IN5	IN6	IN7	IN8	IN11	IN1	52A	52B	43A	IN10	IN2	IN9	IN4	IN3
DPU2000R:	FB8	FB7	IN5	IN6	IN7	IN8	FB6	IN1	FB5	FB4	FB3	FB2	IN2	FB1	IN4	IN3
DPU1500R:	N/A	N/A	IN5	N/A	N/A	IN6	N/A	IN1	N/A	N/A	N/A	N/A	IN2	N/A	IN4	IN3

Figure 12 – Physical Input Mapping

Programmable Input Definitions

Physical Input: The opto-isolated binary input that allows external control by physically wiring the input terminals of the relay. Physical inputs are labeled (IN1, IN2, IN3, …, 43A, 52A, 52B).

Logical Input: An input equated by the boolean combination of the physical inputs. These inputs are used by the relay's state machine and control subroutines. Logical Inputs are labeled (PH3, GRD, TCM, …). See protocol document paragraph 4.1 for additional labels.

Active Open: This defines the type of connection from the physical input or inputs and means the physical state of the opto-isolator's logic is inverted. Example: if the voltage across IN1's terminals equals zero, then the boolean equation will evaluate this term as a logical one. Likewise, when a volatge is applied to IN1, the boolean equation will evaluate this term as a logical zero.

Active Closed: This defines the type of connection from the physical input or inputs and means that the physical state of the opto-isolator's logic is the non-inverted. Example: if a voltage is applied across IN1's terminals, then the boolean equation will evaluate this term as a logical one. Likewise, when a volatge is applied to IN1, the boolean equation will evaluate this term as a logical zero.

Example of a boolean input equation:

```
          Logical       Ored Physical
50-1   =      IN1 + IN2 + IN3

          Logical       ANDed Physical
GRD    =      IN1 * IN2 * IN3
```

Input Select:
The physical inputs are associated with a bit mask to determine which inputs are used when resolving the logical input's boolean equation. If the appropriate bit is set, the term will be included as part of the equation. Likewise, a cleared bit indicates that the physical input term will be ignored.

The bit assignment mask for the physical inputs are as follows:

0 = IN3, 1 = IN4, 2 = IN9, 3 = IN2, 4 = IN10, 5 = 43A, 6 = 52B, 7 = 52A, 8 = IN1, 9 = IN11, 10 = IN8, 11 = IN7, 12 = IN6, 13 = IN5, 14 = IN13, 15 = IN12.

Negated AND Input:
This is a bit mask that indicates if a selected input is inverted based on the active open or closed state. The bit mask uses the same associated physical inputs pattern as in the Input Select data.

AND/OR Select:
The combination of the physical inputs' state used to resolve the boolean equation allows for the algebraic ANDing or Oring of all of the selected physical inputs.

User Definable Names:
Physical inputs, IN1 – IN13, have memory allocated for an eight character (NULL is implied in character 9) user definable strings.

Four protocol commands are required to view or change the relay's programmable input setting tables. The command order for viewing these tables can be retrieved in any sequence, but when the settings are sent to the relay, the commands must be sent in the following sequence:

3 11 1: Recieve Programmable Input Select and Index data.
3 11 2: Recieve Programmable Negated AND Input data.
3 11 3: Recieve Programmable Input AND/OR Select data.
3 11 4: Recieve Programmable Input User Defined Name data.

Up to 29 logical inputs may selected at any one time. The protocol document refers to these generic logical inputs as INPUT1 – INPUT29.

Example:
We want the PH3 logical input to be the combination of the physical inputs IN4 AND NOT IN3 AND ALT1 logical input to be the combination of the physical inputs IN1 OR IN3 OR NOT IN5.

PH3 = IN4 * !IN3
ALT1 = IN1 + IN3 + !IN5

First, generic inputs must be selected to setup the logic equation and for this case INPUT3 is used for PH3 and INPUT8 is used for ALT1. Note, any inputs 1-29 could be valid selections. The data values required for these selections use the the INDEX table defined in the protocol document in section 4.1 and 11.1.

Command	Msg/byte	HexData	Comment
3 11 1	5/1	0xFF	No physicals selected for INPUT3 Input Select high byte
3 11 1	5/2	0xFA	Selects IN3 and IN4 bits for INPUT3 Input Select low byte
3 11 1	5/3	0x03	Assigning PH3 offset to INPUT3 for Input Index
3 11 1	10/1	0xB7	Selects IN1 and IN5 bits for INPUT8 Input Select high byte
3 11 1	10/2	0xF7	Selects IN3 bit for INPUT8 Input Select low byte
3 11 1	10/3	0x03	Assigning ALT1 offset to INPUT8 for Input Index
3 11 2	4/1	0xFF	No physical's logic inverted for INPUT3 Negated AND Input high byte
3 11 2	4/2	0xF7	Inverts IN3's logical state for INPUT3 Negated AND Input low byte
3 11 2	7/3	0xBF	Inverts IN5's logical state for INPUT8 Negated AND Input high byte
3 11 2	8/1	0xFF	No physical's logic inverted for INPUT8 Negated AND Input low byte

3 11 3	3/1	0x00	Boolean combination of INPUT3 selected
3 11 3	3/2	0x00	physical logic are ANDed, all other
3 11 3	3/3	0x00	INPUT1,2,4-29 are Ored together
3 11 3	4/1	0x04	

Bit = 0, Physical Input is selected.
Bit = 1, Physical Input is not selected.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.
Index byte is the offset into the DPU's logical input structure.

Logical Input List for DPU2000 – Requires matrix (29 x 16) to allow user to map 29 Logical Inputs to 13 Physical Inputs plus "43A", "52A", and "52B". Logical Inputs include: "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "UDI".

Logical Input List for DPU2000R – Requires matrix (29 x 16) to allow user to map 29 Logical Inputs to 8 Physical Inputs plus 8 Feedback Inputs. Logical Inputs include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "EXTBF", "BFI", "UDI", "25"(*Synch Check Model*), "25By"(*Synch Check Model*). The following logical inputs are available in CPU versions greater than 1.92: "LOCAL", "TGT", "SIA". The following logical inputs are available in CPU version greater than 4.02 (2.01 for PTH): LIS1, LIS2, LIS3, LIS4, LIS5, LIS6, LIS7, LIS8, LIR1, LIR2, LIR3, LIR4, LIR5, LIR6, LIR7, LIR8, TR_SET, TR_RST.

Logical Input List for DPU1500R – Requires matrix (29 x 6) to allow user to map 29 Logical Inputs to 6 Physical Inputs. Logical Inputs include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "UDI", "LOCAL", "TGT", "SIA".

Table 3 below has the complete listing of Logical Input Offsets and their respective definitions.

Table 3-Logical Input Definitions

Index	Logical Input	Definition
00	52A	Breaker Position – Closed or Open per breaker
01	52B	Breaker Position – Open or Closed opposite of breaker
02	43A	Reclose Function – Enabled or Disabled
03	PH3	Phase Torque Control
04	GRD	Ground Torque Control
05	SCC	Spring Charging Contact
06	79S	Single Shot Reclosing
07	79M	Multi Shot Reclosing
08	TCM	Trip Coil Monitoring
09	50-1	Enables instantaneous over-currents: 50P-1, 50N-1
10	50-2	Enables instantaneous over-currents: 50P-2, 50N-2
11	50-3	Enables instantaneous overcurrents: 50P-3, 50N-3
12	ALT1	Enables ALT1 settings
13	ALT2	Enables ALT2 settings
14	ECI1	Event Capture Initiate - data recorded in fault record
15	ECI2	Event Capture Initiate – data recorded in fault record
16	WCI	Waveform Capture Initiate
17	ZSC	Zone Sequence Co-ordination
18	Open	Initiate a circuit breaker Trip
19	Close	Initiate a circuit breaker Close
20	46	Enables 46 protective function
21	67P	Enables 67P protective function (DPU2000/R)
22	67N	Enables 67N protective function (DPU2000/R)
23	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
24	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
25	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
26	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
27	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
28	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
29	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
30	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
31	ULI1	User Logical Input – asserts ULO1 (DPU2000/R)
32	CRI	Counter Reset Input – resets all over-current and recloser counters
33	ARCI	Timed reclose block
34	TARC	Initiate Trip and Automatic Reclose
35	SEF	Enables Sensitive Earth Fault
36	EXTBFI	External Starter Input (DPU2000/R)
37	BFI	Breaker Fail Initiate (DPU2000/R)
38	UDI	User-defined Display Input
39	25	Enables Synchronism Check function (DPU2000/R)
40	25 BYP	Synchronism Check Bypass
41	LOCAL	Local enable
42	TGT	Resets target alarms and target LEDs
43	SIA	Resets seal-in alarms
44	LIS1	Set #1 Latching Logical I/O
45	LIS2	Set #2 Latching Logical I/O
46	LIS3	Set #3 Latching Logical I/O
47	LIS4	Set #4 Latching Logical I/O
48	LIS5	Set #5 Latching Logical I/O
49	LIS6	Set #6 Latching Logical I/O
50	LIS7	Set #7 Latching Logical I/O
51	LIS8	Set #8 Latching Logical I/O
52	LIR1	Reset #1 Latching Logical I/O
53	LIR2	Reset #2 Latching Logical I/O
54	LIR3	Reset #3 Latching Logical I/O

Index	Logical Input	Definition
55	LIR4	Reset #4 Latching Logical I/O
56	LIR5	Reset #5 Latching Logical I/O
57	LIR6	Reset #6 Latching Logical I/O
58	LIR7	Reset #7 Latching Logical I/O
59	LIR8	Reset #8 Latching Logical I/O
60	TR_SET	Set Hot-Line-Tag function
61	TR_RST	Reset Hot-Line-Tag function
62	ULI 10	User Logical Input 10
63	ULI 11	User Logical Input 11
64	ULI 12	User Logical Input 12
65	ULI 13	User Logical Input 13
66	ULI 14	User Logical Input 14
67	ULI 15	User Logical Input 15
68	ULI 16	User Logical Input 16
69	46A TC	46A Torque Control Input
70	SWSET	Logical Input that on rising edge will switch enabled settings groups
71	SHIFTA	Rising Edge Trigger for Barrel Shifter A
72	SHIFTB	Rising Edge Trigger for Barrel Shifter B

Example : if message 2/1 = hex 24
2/2 = hex 11
2/3 = hex 4

Then I/O word is 00100100 00010001 hex 2411. All of these outputs are mapped onto GND (04 offset). Note the Physical Inputs are translated using the physical input table below.

In the example IN3, IN10, IN8 and IN5 are selected for GND. The AND/OR selection and enable disable mapping is selected with commands 3 11 3 and 3 11 2.

Msg byte	Definition
1/1	Relay Status (Note: the relay status is cleared by the 3 0 8 command) Bits that are set to 1 is an indication the condition exists. Bit 0 : SelfTest Status Bit 1 : Contact Input Status changed Bit 2 : Local Settings Change Bit 3 : Remote Edit Disabled. Bit 4 : Alternate Settings Group 1 Active. Bit 5 : Alternate Setting Group 2 Active. Bit 6 : Fault Record Logged. Bit 7 : Power was Cycled
1/2	Command + Subcommand = 0x41
1/3	Total Number of Messages = 31
2/1	INPUT1 high byte (per bits 0-7 in Figure 12, on page 310)
2/2	INPUT1 low byte (per bits 8-15 in Figure 12, on page 310)
2/3	INPUT1 index byte (per Table 3, on page 313)
3/1	INPUT2 high byte
3/2	INPUT2 low byte
3/3	INPUT2 index byte
4/1	INPUT3 high byte
4/2	INPUT3 low byte
4/3	INPUT3 index byte
5/1	INPUT4 high byte
5/2	INPUT4 low byte
5/3	INPUT4 index byte
6/1	INPUT5 high byte
6/2	INPUT5 low byte

6/3	INPUT5 index byte
7/1	INPUT6 high byte
7/2	INPUT6 low byte
7/3	INPUT6 index byte
8/1	INPUT7 high byte
8/2	INPUT7 low byte
8/3	INPUT7 index byte
9/1	INPUT8 high byte
9/2	INPUT8 low byte
9/3	INPUT8 index byte
10/1	INPUT9 high byte
10/2	INPUT9 low byte
10/3	INPUT9 index byte
11/1	INPUT10 high byte
11/2	INPUT10 low byte
11/3	INPUT10 index byte
12/1	INPUT11 high byte
12/2	INPUT11 low byte
12/3	INPUT11 index byte
13/1	INPUT12 high byte
13/2	INPUT12 low byte
13/3	INPUT12 index byte
14/1	INPUT13 high byte
14/2	INPUT13 low byte
14/3	INPUT13 index byte
15/1	INPUT14 high byte
15/2	INPUT14 low byte
15/3	INPUT14 index byte
16/1	INPUT15 high byte
16/2	INPUT15 low byte
16/3	INPUT15 index byte
17/1	INPUT16 high byte
17/2	INPUT16 low byte
17/3	INPUT16 index byte
18/1	INPUT17 high byte
18/2	INPUT17 low byte
18/3	INPUT17 index byte
19/1	INPUT18 high byte
19/2	INPUT18 low byte
19/3	INPUT18 index byte
20/1	INPUT19 high byte
20/2	INPUT19 low byte
20/3	INPUT19 index byte
21/1	INPUT20 high byte
21/2	INPUT20 low byte
21/3	INPUT20 index byte
22/1	INPUT21 high byte
22/2	INPUT21 low byte
22/3	INPUT21 index byte
23/1	INPUT22 high byte
23/2	INPUT22 low byte
23/3	INPUT22 index byte
24/1	INPUT23 high byte
24/2	INPUT23 low byte
24/3	INPUT23 index byte
25/1	INPUT24 high byte
25/2	INPUT24 low byte
25/3	INPUT24 index byte
26/1	INPUT25 high byte

26/2	INPUT25 low byte
26/3	INPUT25 index byte
27/1	INPUT26 high byte
27/2	INPUT26 low byte
27/3	INPUT26 index byte
28/1	INPUT27 high byte
28/2	INPUT27 low byte
28/3	INPUT27 index byte
29/1	INPUT28 high byte
29/2	INPUT28 low byte
29/3	INPUT28 index byte
30/1	INPUT29 high byte
30/2	INPUT29 low byte
30/3	INPUT29 index byte
31/1	spare
31/2	Checksum high byte
31/3	Checksum low byte

8.4.2 Transmit Programmable Input Negated AND Input (3 4 2)

Negated Programmable Input data transferred from relay to PC.

Bit = 0, Enabled when input is opened.
Bit = 1, Enabled when input is closed.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x42
1/3	Total Number of Messages = 21
2/1	INPUT1 high byte (per bits 8-15 in Figure 12, on page 310)
2/2	INPUT1 low byte (per bits 0-7 in Figure 12, on page 310)
2/3	INPUT2 high byte
3/1	INPUT2 low byte
3/2	INPUT3 high byte
3/3	INPUT3 low byte
4/1	INPUT4 high byte
4/2	INPUT4 low byte
4/3	INPUT5 high byte
5/1	INPUT5 low byte
5/2	INPUT6 high byte
5/3	INPUT6 low byte
6/1	INPUT7 high byte
6/2	INPUT7 low byte
6/3	INPUT8 high byte
7/1	INPUT8 low byte
7/2	INPUT9 high byte
7/3	INPUT9 low byte
8/1	INPUT10 high byte
8/2	INPUT10 low byte
8/3	INPUT11 high byte
9/1	INPUT11 low byte
9/2	INPUT12 high byte
9/3	INPUT12 low byte
10/1	INPUT13 high byte
10/2	INPUT13 low byte
10/3	NPUT14 high byte
11/1	INPUT14 low byte
11/2	INPUT15 high byte

11/3	INPUT15 low byte
12/1	INPUT16 high byte
12/2	INPUT16 low byte
12/3	INPUT17 high byte
13/1	INPUT17 low byte
13/2	INPUT18 high byte
13/3	INPUT18 low byte
14/1	INPUT19 high byte
14/2	INPUT19 low byte
14/3	INPUT20 high byte
15/1	INPUT20 low byte
15/2	INPUT21 high byte
15/3	INPUT21 low byte
16/1	INPUT22 high byte
16/2	INPUT22 low byte
16/3	INPUT23 high byte
17/1	INPUT23 low byte
17/2	INPUT24 high byte
17/3	INPUT24 low byte
18/1	INPUT25 high byte
18/2	INPUT25 low byte
18/3	INPUT26 high byte
19/1	INPUT26 low byte
19/2	INPUT27 high byte
19/3	INPUT27 low byte
20/1	INPUT28 high byte
20/2	INPUT28 low byte
20/3	INPUT29 high byte
21/1	INPUT29 low byte
21/2	Checksum high byte
21/3	Checksum low byte

8.4.3 Transmit Programmable Input AND/OR Select (3 4 3)

Bit = 0, Selected inputs are Ored together.
Bit = 1, Selected inputs are ANDed together.

Bit	Logical Input
0	INPUT1
1	INPUT2
.	
.	
.	
27	INPUT28
28	INPUT29
29	not used reserved for 52A
30	not used reserved for 52B
31	not used reserved for 43A

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x43
1/3	Total Number of Messages = 3
2/1	Programmable input AND/OR selection bits 24-31
2/2	Programmable input AND/OR selection bits 16-23
2/3	Programmable input AND/OR selection bits 8-15
3/1	Programmable input AND/OR selection bits 0-7
3/2	Checksum high byte
3/3	Checksum low byte

8.4.4 Transmit Programmable User Defined Input Names (3 4 4)

User definable 8 char input strings. Byte 9 is an implied NULL.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x44
1/3	Total Number of Messages = 37
2/1-4/2	IN1 Character String 8 bytes
4/3-7/1	IN2 Character String 8 bytes
7/2-9/3	IN3 Character String 8 bytes
10/1-12/2	IN4 Character String 8 bytes
12/3-15/1	IN5 Character String 8 bytes
15/2-17/3	IN6 Character String 8 bytes
18/1-20/2	IN7 Character String 8 bytes (DPU2000 and DPU2000R)
20/3-23/1	IN8 Character String 8 bytes (DPU2000 and DPU2000R)
23/2-25/3	IN9 Character String 8 bytes (DPU2000)
26/1-28/2	IN10 Character String 8 bytes (DPU2000)
28/3-31/1	IN11 Character String 8 bytes (DPU2000)
31/2-33/3	IN12 Character String 8 bytes (DPU2000)
34/1-36/2	IN13 Character String 8 bytes (DPU2000)
36/3-37/1	Spare Input Strings
37/2	Checksum high byte
37/3	Checksum low byte

8.4.5 Transmit Programmable Output Select (3 4 5)

Bit Position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPU2000:	N/A	N/A	N/A	N/A	N/A	N/A	Out8	Out7	Out1	Out2	Out3	Out5	Out4	Out6	Close	Trip
DPU2000R:	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	Out1	Out2	Out3	Out5	Out4	Out6	N/A	Trip
DPU1500R:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out1	Out2	Out3	Out5	Out4	Out6	N/A	Trip

Figure 13 – Physical Output Mapping

Bit = 0, Physical Output is selected.
Bit = 1, Physical Output is not selected.
Least significant low byte consists of bits 0 through 7.
Least significant high byte consists of bits 8 through 15.
Most significant low byte consists of bits 16 through 23.
Most significant high byte consists of bits 24 through 31.

Table 4-Programmable Bit Assignments for Outputs

Bit	Logical Output Assigned
0	TRIP (Fixed)
1	CLOSE (Fixed DPU2000, mapping NOT permitted by DPU2000R or DPU1500R)
2	OUTPUT 1
3	OUTPUT 2
4	OUTPUT 3
5	OUTPUT 4
6	OUTPUT 5
7	OUTPUT 6
8	OUTPUT 7
9	OUTPUT 8
10	OUTPUT 9
11	OUTPUT 10
12	OUTPUT 11
13	OUTPUT 12
14	OUTPUT 13
15	OUTPUT 14
16	OUTPUT 15
17	OUTPUT 16
18	OUTPUT 17
19	OUTPUT 18
20	OUTPUT 19
21	OUTPUT 20
22	OUTPUT 21
23	OUTPUT 22
24	OUTPUT 23
25	OUTPUT 24
26	OUTPUT 25
27	OUTPUT 26
28	OUTPUT 27
29	OUTPUT 28
30	OUTPUT 29
31	OUTPUT 30

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x45
1/3	Total Number of Messages = 21
2/1	Contact OUT6 most significant high byte (bits assigned per Table 4, page 319)
2/2	Contact OUT6 most significant low byte
2/3	Contact OUT6 least significant high byte
3/1	Contact OUT6 least significant low byte
3/2	Contact OUT4 most significant high byte
3/3	Contact OUT4 most significant low byte
4/1	Contact OUT4 least significant high byte
4/2	Contact OUT4 least significant low byte
4/3	Contact OUT5 most significant high byte
5/1	Contact OUT5 most significant low byte
5/2	Contact OUT5 least significant high byte
5/3	Contact OUT5 least significant low byte
6/1	Contact OUT3 most significant high byte
6/2	Contact OUT3 most significant low byte
6/3	Contact OUT3 least significant high byte
7/1	Contact OUT3 least significant low byte
7/2	Contact OUT2 most significant high byte

7/3	Contact OUT2 most significant low byte
8/1	Contact OUT2 least significant high byte
8/2	Contact OUT2 least significant low byte
8/3	Contact OUT1 most significant high byte
9/1	Contact OUT1 most significant low byte
9/2	Contact OUT1 least significant high byte
9/3	Contact OUT1 least significant low byte
10/1	Contact OUT7 most significant high byte (DPU2000) DPU2000R FB1 most significant high byte
10/2	Contact OUT7 most significant low byte (DPU2000) DPU2000R FB1 most significant low byte
10/3	Contact OUT7 least significant high byte (DPU2000) DPU2000R FB1 least significant high byte
11/1	Contact OUT7 least significant low byte (DPU2000) DPU2000R FB1 least significant low byte
11/2	Contact OUT8 most significant high byte (DPU2000) DPU2000R FB2 most significant high byte
11/3	Contact OUT8 most significant low byte (DPU2000) DPU2000R FB2 most significant low byte
12/1	Contact OUT8 least significant high byte (DPU2000) DPU2000R FB2 least significant high byte
12/2	Contact OUT8 least significant low byte (DPU2000) DPU2000R FB2 least significant low byte
12/3	DPU2000R FB3 most significant high byte
13/1	DPU2000R FB3 most significant low byte
13/2	DPU2000R FB3 least significant high byte
13/3	DPU2000R FB3 least significant low byte
14/1	DPU2000R FB4 most significant high byte
14/2	DPU2000R FB4 most significant low byte
14/3	DPU2000R FB4 least significant high byte
15/1	DPU2000R FB4 least significant low byte
15/2	DPU2000R FB5 most significant high byte
15/3	DPU2000R FB5 most significant low byte
16/1	DPU2000R FB5 least significant high byte
16/2	DPU2000R FB5 least significant low byte
16/3	DPU2000R FB6 most significant high byte
17/1	DPU2000R FB6 most significant low byte
17/2	DPU2000R FB6 least significant high byte
17/3	DPU2000R FB6 least significant low byte
18/1	DPU2000R FB7 most significant high byte
18/2	DPU2000R FB7 most significant low byte
18/3	DPU2000R FB7 least significant high byte
19/1	DPU2000R FB7 least significant low byte
19/2	DPU2000R FB8 most significant high byte
19/3	DPU2000R FB8 most significant low byte
20/1	DPU2000R FB8 least significant high byte
20/2	DPU2000R FB8 least significant low byte
20/3	Spare
21/1	Spare
21/2	Checksum high byte
21/3	Checksum low byte

8.4.6 Transmit Programmable Output AND/OR Select (3 4 6)

Bit = 0, Selected inputs are Ored together.
Bit = 1, Selected inputs are ANDed together.

Index byte is the offset into the DPU's logical output structure.

Logical Output List for DPU2000 – Requires matrix (32 x 8) to allow user to map 32 Logical Outputs to 8 Physical Outputs. NOTE: first two logicals, ***TRIP*** and ***CLOSE*** are fixed (bits 0 and 1), user is not permitted to remove these from the list.

Logical Outputs include: “TRIP”, “CLOSE”, “ALARM”, “BFA”, “TCFA”, “79LOA”, “TCC”, “PUA”, “51P”, “51N”, “46”, “50P-1”, “50N-1”, “50P-2”, “50N-2”, “50P-3”, “50N-3”, “PATA”, “PBTA”, “PCTA”, “67P”, “67N”, “81S-1”, “81R-1”, “81O-1”, “27-1P”, “59”, “79DA”, “79CA1”, “OCTC”, “KSI”, “PDA”, “NDA”, “PVArA”, “NVArA”, “LOADA”, “50-1D”, “LPFA”, “HPFA”, “ZSC”, “50-2D”, “BFUA”, “STCA”, “PH3-D”, “GRD-D”, “32PA”, “32NA”, “27-3P”, “VarDA”, “79CA2”, “TRIPA”, “TRIPB”, “TRIPC”, “27-1P*”, “46*”, “50P-1*”, “50N-1*”, “50P-2*”, “50N-2*”, “50P-3*”, “50N-3*”, “51P*”, “51N*”, “59*”, “67P*”, “67N*”, “81S-1*”, “81R-1*”, “81O-1*”, “27-3P*”, “TRIPA*”, “TRIPB*”, “TRIPC*”, “ULO1”, “ULO2”, “ULO3”, “ULO4”, “ULO5”, “ULO6”, “ULO7”, “ULO8”, “ULO9”, “81O-2”, “81S-2”, “81R-2”, “81O-2*”, “81S-2*”, “81R-2*”, “CLTA”, “Pwatt1”, “Pwatt2”, “79CA1*”, “79CA2*”, “BFA*”.

Logical Output List for DPU2000R – Requires matrix (31 x 14) to allow user to map 31 Logical Outputs to 6 Physical Outputs plus 8 Feedback Outputs. NOTE: first logical, ***TRIP*** is fixed, user is not permitted to remove Trip logical from the list. Also note, since the ***CLOSE*** logical is specific to DPU2000, mapping of this logical (located at bit 1) is NOT permissible. Logical Outputs include: “TRIP”, “CLOSE”, “ALARM”, “BFA”, “TCFA”, “79LOA”, “TCC”, “PUA”, “51P”, “51N”, “46”, “50P-1”, “50N-1”, “50P-2”, “50N-2”, “50P-3”, “50N-3”, “PATA”, “PBTA”, “PCTA”, “67P”, “67N”, “81S-1”, “81R-1”, “81O-1”, “27-1P”, “59”, “79DA”, “79CA1”, “OCTC”, “KSI”, “PDA”, “NDA”, “PVArA”, “NVArA”, “LOADA”, “50-1D”, “LPFA”, “HPFA”, “ZSC”, “50-2D”, “BFUA”, “STCA”, “PH3-D”, “GRD-D”, “32PA”, “32NA”, “27-3P”, “VarDA”, “79CA2”, “TRIPA”, “TRIPB”, “TRIPC”, “27-1P*”, “46*”, “50P-1*”, “50N-1*”, “50P-2*”, “50N-2*”, “50P-3*”, “50N-3*”, “51P*”, “51N*”, “59*”, “67P*”, “67N*”, “81S-1*”, “81R-1*”, “81O-1*”, “27-3P*”, “TRIPA*”, “TRIPB*”, “TRIPC*”, “ULO1”, “ULO2”, “ULO3”, “ULO4”, “ULO5”, “ULO6”, “ULO7”, “ULO8”, “ULO9”, “81O-2”, “81S-2”, “81R-2”, “81O-2*”, “81S-2*”, “81R-2*”, “CLTA”, /* V1.40 */ “Pwatt1”, “Pwatt2”, “79CA1*”, “79CA2*”. The following were added to CPU V1.60: “SEF*”(*Sensitive Earth Model*), “SEF”(*Sensitive Earth Model*), “BZA”, “BFT”, “ReTrp”, “BFT*”, “ReTrp*”. The following were added to CPU V1.80: “32P-2”, “32N-2”, “32P-2*”, “32N-2*”, “BFA*”.

The following were added to CPU V1.93: “25*”(*Synch Check Model*), “25”(*Synch Check Model*), “SBA”.

The following were added to CPU V3.20: “79V”and “Rclin”, “59G”,”59G*”, “LO1”, lO2”, ”LO3”, ”LO4”, ”LO5”, ”LO6”, ”LO7”, ”LO8”, “TR_ON”, ”TR_OFF”, ”TR_TAG”.

The following were added to CPU V5.0: 59-3P, 59-3P*, 47, 47*, 21P-1, 21P-1*, 21P-2, 21P-2*, 21P-3, 21P-3*, 21P-4, 21P-4*.

Logical Output List for DPU1500R – Requires matrix (31 x 6) to allow user to map 31 Logical Outputs to 6 Physical Outputs. NOTE: first logical, ***TRIP*** is fixed, user is not permitted to remove Trip logical from the list. Also note, since the ***CLOSE*** logical is specific to DPU2000, mapping of this logical (located at bit 1) is NOT permissible. Logical Outputs include: “TRIP”, “CLOSE”, “ALARM”, “BFA”, “TCFA”, “79LOA”, “TCC”, “PUA”, “51P”, “51N”, “46”, “50P-1”, “50N-1”, “50P-2”, “50N-2”, “50P-3”, “50N-3”, “PATA”, “PBTA”, “PCTA”, “27-1P”, “79DA”, “79CA1”, “OCTC”, “KSI”, “PDA”, “NDA”, “PVArA”, “NVArA”, “LOADA”, “50-1D”,”LPFA”, “HPFA”, “ZSC”, “50-2D”, “BFUA”, “STCA”, “PH3-D”, “GRD-D”, “27-3P”, “VarDA”, “79CA2”, “TRIPA”, “TRIPB”, “TRIPC”, “27-1P*”, “46*”, “50P-1*”, “50N-1*”, “50P-2*”, “50N-2*”, “50P-3*”, “50N-3*”, “51P*”, “51N*”, “27-3P*”, “TRIPA*”, “TRIPB*”, “TRIPC*”, “CLTA”, “Pwatt1”, “Pwatt2”, “79CA1*”, “79CA2*”, “SEF*”(*Sensitive Earth Model*), “SEF”(*Sensitive Earth Model*), “BZA”, “BFA*”, “SBA”, “79V” and “Rclin”.

See Table 5 below for a complete listing of Logical Output Offsets and respective definitions.

Table 5-Logical Output Indices & Definitions

Index	Logical Output	Definitions
00	TRIP	Fixed Trip
01	CLOSE	Fixed Close
02	ALARM	Self Check Alarm
03	27-1P	Single Phase Under Voltage
04	46	Negative Sequence Overcurrent
05	50P-1	Phase Inst. Overcurrent
06	50N-1	Neutral Inst. Overcurrent
07	50P-2	Phase Inst. Overcurrent
08	50N-2	Neutral Inst. Overcurrent
09	50P-3	Phase Inst. Overcurrent
10	50N-3	Neutral Inst. Overcurrent
11	51P	Phase Time Overcurrent
12	51N	Neutral Time Overcurrent
13	59	Over Voltage
14	67P	Directional Overcurrent (pos seq)
15	67N	Directional Overcurrent (neg seq)
16	81S-1	Frequency Shed (First stage)
17	81R-1	Frequency Restore (First stage)
18	PATA	Phase A Target
19	PBTA	Phase B Target
20	PCTA	Phase C Target
21	TCFA	Trip Circuit Fail
22	TCC	Tap Changer Cutout
23	79DA	Recloser Disable
24	PUA	Pickup
25	79LOA	Recloser Lockout
26	BFA	Breaker Fail
27	PDA	Phase Peak Demand
28	NDA	Neutral Peak Demand
29	BFUA	Blown Fuse
30	KSI	KiloAmp Summation
31	79CA-1	Reclose Counter1
32	HPFA	High Power Factor
33	LPFA	Low Power Factor
34	OCTC	Overcurrent Trip Counter
35	50-1D	50-1 Element Disable
36	50-2D	50-2 Element Disable
37	STCA	Setting Table Change
38	ZSC	Zone Sequence
39	PH3-D	Phase Torque Control Disable
40	GRD-D	Neutral Torque Control Disable
41	32PA	Directional Pickup (pos seq)
42	32NA	Directional Pickup (neg seq)
43	27-3P	3 Phase Under Voltage
44	VarDA	Var Demand
45	79CA-2	Reclose Counter2
46	TRIPA	Single Pole Trip Phase A
47	TRIPB	Single Pole Trip Phase B
48	TRIPC	Single Pole Trip Phase C
49	27-1P*	Single Phase Under Voltage
50	46*	Negative Sequence Overcurrent
51	50P-1*	Phase Inst. Overcurrent
52	50N-1*	Neutral Inst. Overcurrent
53	50P-2*	Phase Inst. Overcurrent
54	50N-2*	Neutral Inst. Overcurrent
55	50P-3*	Phase Inst. Overcurrent
56	50N-3*	Neutral Inst. Overcurrent
57	51P*	Phase Time Overcurrent
58	51N*	Neutral Time Overcurrent
59	59*	Over Voltage
60	67P*	Directional Overcurrent (pos seq)
61	67N*	Directional Overcurrent (neg seq)
62	81S-1*	Frequency Shed (First stage)
63	81R-1*	Frequency Restore (First stage)
64	81O-1*	Over Frequency (First stage)
65	27-3P*	3 Phase Under Voltage
66	TRIPA*	Single Pole Trip Phase A

Index	Logical Output	Definitions
67	TRIPB*	Single Pole Trip Phase B
68	TRIPC*	Single Pole Trip Phase C
69	ULO1	User Logical Output 1
70	ULO2	User Logical Output 2
71	ULO3	User Logical Output 3
72	ULO4	User Logical Output 4
73	ULO5	User Logical Output 5
74	ULO6	User Logical Output 6
75	ULO7	User Logical Output 7
76	ULO8	User Logical Output 8
77	ULO9	User Logical Output 9
78	PVArA	Positive Var
79	NVArA	Negative Var
80	LOADA	Load Current
81	81O-1	Over Frequency (First Stage)
82	81O-2	Over Frequency (2nd Stage)
83	81S-2	Frequency Shed (2nd Stage)
84	81R-2	Frequency Restore (2nd Stage)
85	81O-2*	Over Frequency (2nd Stage)
86	81S-2*	Frequency Shed (2nd Stage)
87	81R-2*	Frequency Restore (2nd Stage)
88	CLTA	Cold Load Timer
89	Pwatt1	Positive Watt Alarm 1
90	Pwatt2	Positive Watt Alarm 2
91	79CA1*	Recloser Counter 1 Alarm
92	79CA2*	Recloser Counter 2 Alarm
93	SEF*	Sensitive Earth Fault Trip
94	SEF	Sensitive Earth Fault Trip
95	BZA	Bus Zone Alarm
96	BF Trip	Breaker Fail Trip
97	BF Retrip	Breaker Fail Re-Trip
98	BF Trip*	Breaker Fail Trip
99	BF Retrip*	Breaker Fail Re-Trip
100	32P	Phase Directionality Alarm
101	32N	Neutral Directionality Alarm
102	32P*	Phase Directionality Alarm
103	32N*	Neutral Directionality Alarm
104	BFA*	Breaker Failure Alarm
105	25*	In Synchronism
106	25	In Synchronism
107	SBA	Slow Breaker Alarm
108	79V	Recloser
109	Rclin	Recloer init
110	59G	V0 Over Voltage
111	59G*	V0 Over Voltage seal-in
112	LO1	Latching output1
113	LO2	Latching output2
114	LO3	Latching output3
115	LO4	Latching output4
116	LO5	Latching output5
117	LO6	Latching output6
118	LO7	Latching output7
119	LO8	Latching output8
120	TR_ON	Hot Hole Tagging On
121	TR_OFF	Hot Hole Tagging Off
122	TR_TAG	Hot Hole Tagging Tagged
123	59-3P	3 Phase Over Voltage
124	59-3P*	3 Phase Over Voltage Seal-in
125	47	Neg Seq Over Voltage
126	47*	Net Seq Over Voltage Seal-in
127	50-3D	50-3 Element Disable
128	21P-1	Fwd Reach Zone 1 Distance Alarm
129	21P-1*	Fwd Reach Zone 1 Distance Seal-in Alarm
130	21P-2	Fwd Reach Zone 2 Distance Alarm
131	21P-2*	Fwd Reach Zone 2 Distance Seal-in Alarm
132	21P-3	Fwd Reach Zone 3 Distance Alarm
133	21P-3*	Fwd Reach Zone 3 Distance Seal-in Alarm
134	21P-4	Fwd Reach Zone 4 Distance Alarm

Index	Logical Output	Definitions
135	21P-4*	Fwd Reach Zone 4 Distance Seal-in Alarm
136	C1	Control Button 1
137	C2	Control Button 2
138	C3	Control Button 3
139	C4	Control Button 4
140	C5	Control Button 5
141	C6	Control Button 6
142	TripT	Trip Target
143	NTA	Neutral Target
144	TimeT	Time Target
145	InstT	Inst Target
146	NeqSeqT	Negative Seq Target
147	FreqT	Frequency Target
148	DirT	Direction Target
149	VoltT	Volt Target
150	DistT	Distance Target
151	SEFT	Sensitve Earth Fault Target
152	ULO 10	User Logical Output 10
153	ULO 11	User Logical Output 10
154	ULO 12	User Logical Output 10
155	ULO 13	User Logical Output 10
156	ULO 14	User Logical Output 10
157	ULO 15	User Logical Output 10
158	ULO 16	User Logical Output 10
159	HBHL	Hot Bus – Hot Line
160	HBDL	Hot Bus – Dead Line
161	HBHL	Hot Bus – Hot Line
162	HBDL	Hot Bus – Dead Line
163	46A	Negative Sequence Overcurrent, percentage pickup
164	46A*	Negative Sequence Overcurrent, percentage pickup
165	REMOTE_D	Remote Disable
166	PRI-ON	Primary Settings Active
167	ALT1-ON	ALT1 Settings Active
168	ALT2-ON	ALT2 Settings Active
169	SHIFTA-1	Barrel Shift-A Output No. 1
170	SHIFTA-2	Barrel Shift-A Output No. 2
171	SHIFTA-3	Barrel Shift-A Output No. 3
172	SHIFTA-4	Barrel Shift-A Output No. 4
173	SHIFTB-1	Barrel Shift-B Output No. 1
174	SHIFTB-2	Barrel Shift-B Output No. 2
175	SHIFTB-3	Barrel Shift-B Output No. 3
176	SHIFTB-4	Barrel Shift-B Output No. 4

NOTE: SEF, SEF*, and BZA logical outputs are available in Sensitive Earth model only. Also, * indicates sealed in outputs.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x46
1/3	Total Number of Messages = 13
2/1	spare (bits 24-31)
2/2	spare (bits 16-23)
2/3	Programmable output AND/OR selection bits 8-15
3/1	Programmable output AND/OR selection bits 0-7
3/2	OUTPUT1 index byte (index per Table 5, page 322)
3/3	OUTPUT2 index byte
4/1	OUTPUT3 index byte
4/2	OUTPUT4 index byte
4/3	OUTPUT5 index byte
5/1	OUTPUT6 index byte
5/2	OUTPUT7 index byte
5/3	OUTPUT8 index byte
6/1	OUTPUT9 index byte
6/2	OUTPUT10 index byte

6/3	OUTPUT11 index byte
7/1	OUTPUT12 index byte
7/2	OUTPUT13 index byte
7/3	OUTPUT14 index byte
8/1	OUTPUT15 index byte
8/2	OUTPUT16 index byte
8/3	OUTPUT17 index byte
9/1	OUTPUT18 index byte
9/2	OUTPUT19 index byte
9/3	OUTPUT20 index byte
10/1	OUTPUT21 index byte
10/2	OUTPUT22 index byte
10/3	OUTPUT23 index byte
11/1	OUTPUT24 index byte
11/2	OUTPUT25 index byte
11/3	OUTPUT26 index byte
12/1	OUTPUT27 index byte
12/2	OUTPUT28 index byte
12/3	OUTPUT29 index byte
13/1	OUTPUT30 index byte
13/2	Checksum high byte
13/3	Checksum low byte

8.4.7 Transmit Programmable Output User Defined Strings (3 4 7)

User definable 8 char output strings. Byte 9 is an implied NULL

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x47
1/3	Total Number of Messages = 37
2/1-4/2	OUT1 Character String 8 bytes
4/3-7/1	OUT2 Character String 8 bytes
7/2-9/3	OUT3 Character String 8 bytes
10/1-12/2	OUT4 Character String 8 bytes
12/3-15/1	OUT5 Character String 8 bytes
15/2-17/3	OUT6 Character String 8 bytes
18/1-20/2	OUT7 Character String 8 bytes (DPU2000)
20/3-23/1	OUT8 Character String 8 bytes (DPU2000)
23/2-25/3	Spare Character String 8 bytes
26/1-28/2	Spare Character String 8 bytes
28/3-31/1	Spare Character String 8 bytes
31/2-33/3	Spare Character String 8 bytes
34/1-36/2	Spare Character String 8 bytes
36/3-39/1	Spare Character String 8 bytes
39/2	Checksum high byte
39/3	Checksum low byte

8.4.8 Transmit Relay Settings (3 4 x)

(3 4 8) = Primary Settings
(3 4 9) = Alternate 1 Settings
(3 4 10) = Alternate 2 Settings

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

The following functions are available in the DPU1500R: 51P, 50P-1, 50P-2, 50P-3, 46, 51N, 50N-1, 50N-2, 50N-3, 79 and 27.

8.4.8.1 Standard ANSI Curves for DPU2000 and DPU2000R

Table 6 – ANSI Curve Selection Type I

Index	Overcurrent Curve
0	Extremely Inverse
1	Very Inverse
2	Inverse
3	Short Time Inverse
4	Definite Time
5	Long Time Extremely Inverse
6	Long Time Very Inverse
7	Long Time Inverse
8	Recloser Curve
9	User Curve 1
10	User Curve 2
11	User Curve 3

Table 7 – ANSI Curve Selection Type II

Index	Overcurrent Curve
0	Extremely Inverse
1	Very Inverse
2	Inverse
3	Short Time Inverse
4	Definite Time
5	Long Time Extremely Inverse
6	Long Time Very Inverse
7	Long Time Inverse
8	Recloser Curve
9	Disable
10	User Curve 1
11	User Curve 2
12	User Curve 3

Table 8 – ANSI Curve Selection Type III

Index	Overcurrent Curve
0	Disable
1	Standard
2	Inverse
3	Definite Time
4	Short Time Inverse
5	Short Time Extremely Inverse
6	User Curve 1
7	User Curve 2
8	User Curve 3

8.4.8.2 Recloser Curves for DPU2000 and DPU2000R

NOTE: Catalog Numbers XXXXXXXX-XX2XX and XXXXXXXX-XX3XX use the following curve types for 51P, 50P-1, 51N, and 50N-1 functions. Also, in addition to the Time Dial fields, include 51P, 50P-1, 51N and 50N-1 Minimum Response fields.

Table 9 – Recloser Curve (51P)

Index	Recloser Curve
0	A
1	B
2	C
3	D
4	E
5	K
6	N
7	R
8	W
9	User Curve 1
10	User Curve 2
11	User Curve 3

Table 10 – Recloser Curve (51N)

Index	Recloser Curve
0	2
1	3
2	8
3	8*
4	8+
5	9
6	11
7	Disable
8	User Curve 1
9	User Curve 2
10	User Curve 3

Table 11 – Recloser Curve (50P-1)

Index	Recloser Curve
0	Disable
1	A
2	B
3	C
4	D
5	E
6	K
7	N
8	R
9	W
10	User Curve 1
11	User Curve 2
12	User Curve 3

Table 12 – Recloser Curve (50N-1)

Index	Recloser Curve
0	Disable
1	2
2	3
3	8
4	8*
5	8+
6	9
7	11
8	User Curve 1
9	User Curve 2
10	User Curve 3

8.4.8.3 IEC Curves for DPU2000R

NOTE: The following curves are available in IEC DPU2000R, Catalog Number 687XXXXX-XXXXX. All IEC type curves except Definite Time Curves, use Time Multipliers in place of Time Dials.

Table 13 – IEC Curve Selection Type I

Index	Overcurrent Curve
0	Extremely Inverse
1	Very Inverse
2	Inverse
3	Long Time Inverse
4	Definite Time
5	User Curve 1
6	User Curve 2
7	User Curve 3

Table 14 – IEC Curve Selection Type II

Index	Overcurrent Curve
0	Disable
1	Extremely Inverse
2	Very Inverse
3	Inverse
4	Long Time Inverse
5	Definite Time
6	User Curve 1
7	User Curve 2
8	User Curve 3

Table 15 – IEC Curve Selection Type III

Index	Overcurrent Curve
0	Disable
1	Standard
2	Definite Time
3	User Curve 1
4	User Curve 2
5	User Curve 3

8.4.8.4 ANSI/IEC Curves for DPU1500R

NOTE: All IEC type curves, use Time Multipliers in place of Time Dials.

Table 16 – 1500R Curve Selection Type I

Index	Overcurrent Curve
0	Extremely Inverse
1	Very Inverse
2	Inverse
3	Short Time Inverse
4	Definite Time
5	Long Time Extremely Inverse
6	Long Time Very Inverse
7	Long Time Inverse
8	Recloser Curve
9	IEC Extremely Inverse
10	IEC Very Inverse
11	IEC Inverse
12	IEC Long Time Inverse
13	User Curve 1
14	User Curve 2
15	User Curve 3

Table 17 – 1500R Curve Selection Type II

Index	Overcurrent Curve
0	Extremely Inverse
1	Very Inverse
2	Inverse
3	Short Time Inverse
4	Definite Time
5	Long Time Extremely Inverse
6	Long Time Very Inverse
7	Long Time Inverse
8	Recloser Curve
9	Disable
10	IEC Extremely Inverse
11	IEC Very Inverse
12	IEC Inverse
13	IEC Long Time Inverse
14	User Curve 1
15	User Curve 2
16	User Curve 3

Table 18 – 1500R Curve Selection Type III

Index	Overcurrent Curve
0	Disable
1	Standard
2	Inverse
3	Definite Time
4	Short Time Inverse
5	Short Time Extremely Inverse
6	User Curve 1
7	User Curve 2
8	User Curve 3

8.4.8.5 79-X Select Bit Pattern for DPU2000/2000R/1500R

Table 19 – 79 Lockout & Enable/Disable Bit Pattern

Bit	Function Low byte (bits 0-7): 0=No Lockout/Disable, 1=Enabled High byte (bits 8-15): 0=Enable, 1=Lockout
0, 8	50N-1
1, 9	50N-2
2, 10	50N-3
3, 11	51N
4, 12	50P-1
5, 13	50P-2
6,14	50P-3
7,15	Reserved

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = (Prim = 0x48, Alt1 = 0x49, Alt2 = 0x4a)
1/3	Total Number of Messages = 36
2/1	51P Curve Select byte (Type I or Recloser)
2/2	51P Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
2/3	51P Time dial(1-10 *20)/delay byte(0-10 * 20)
	IEC Curve 51P Time Multiplier (.05-1.00 *200)
3/1	50P-1 Curve Select byte (Type III or Recloser)
3/2	50P-1 Pickup X byte (0.5-20 *10)
3/3	50P-1 Timedial (1-10 *10)/delay(0-9.99 *100) high byte
	IEC Curve –50P-1 Time Multiplier (.05-1.00 *200)
4/1	50P-1 Timedial/delay low byte
4/2	50P-2 Select byte (0=Disable, 1=Enable)
4/3	50P-2 Pickup X byte (0.5-20 *10)
5/1	50P-2 Timedelay high byte (0-9.99 *100)
5/2	50P-2 Timedelay low byte
5/3	50P-3 Select byte (0=Disable, 1=Enable)
6/1	50P-3 Pickup X byte (0.5-20 *10)
6/2	46 Curve Select byte (Type II)
6/3	46 Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
7/1	46 Time dial(1-10 *20)/delay byte(0-10 * 20)
	IEC Curve –46 Time Multiplier (.05-1.00 *200)
7/2	51N Curve Select byte (Type II or Recloser)
7/3	51N Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
8/1	51N Time dial(1-10 *20)/delay byte(0-10 * 20)
	IEC Curve –51N Time Multiplier (.05-1.00 *200)
8/2	50N-1 Curve Select byte (Type III or Recloser)
8/3	50N-1 Pickup X byte (0.5-20 *10)
9/1	50N-1 Timedial/delay high byte (1-10 *10, 0-9.99 *100)
	IEC Curve –50N-1 Time Multiplier (.05-1.00 *200)
9/2	50N-1 Timedial/delay low byte
9/3	50N-2 Select byte (0 = Disable, 1 = Enable)
	Sensitive Earth Model (0=Disable, 1=Standard, 2=SEF, 3=Directional SEF)
10/1	50N-2 Pickup X byte (0.5-20 *10)
10/2	50N-2 Timedelay high byte (0-9.99 *100)
	SEF or Directional SEF Selects – 50N-2 Time Delay (0.5 to 180.0)*200
10/3	50N-2 Timedelay low byte
11/1	50N-3 Select byte (0=Disable, 1=Enable)
11/2	50N-3 Pickup X byte (0.5-20 *10)
11/3	79 Reset Time byte (3-200)
12/1	79-1 Select high byte (Lockout Type)
12/2	79-1 Select low byte (Enable Type)

12/3 79-1 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
13/1 79-1 Open Interval Time low byte
13/2 79-2 Select high byte (Lockout Type)
13/3 79-2 Select low byte (Enable Type)
14/1 79-2 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
14/2 79-2 Open Interval Time low byte
14/3 79-3 Select high byte (Lockout)
15/1 79-3 Select low byte (Enable)
15/2 79-3 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
15/3 79-3 Open Interval Time low byte
16/1 79-4 Select high byte (Lockout Type)
16/2 79-4 Select low byte (Enable Type)
16/3 79-4 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
17/1 79-4 Open Interval Time low byte
17/2 79-5 Select high byte (Lockout Type)
17/3 79-5 Select low byte (Enable Type)
18/1 79-5 Open Interval Time high byte (always lockout)
18/2 79-5 Open Interval Time low byte
18/3 79 Cutout Time byte (1 –201) (201 = Disable)
19/1 Cold Load Time byte (1 –254) (255 = Disable)
19/2 2 Phase Voting byte (0=Disable, 1=Enable)
19/3 67P Select byte (0=Disable, 1=Enable, 2=Lockout)
20/1 67P Curve Select byte (Type I)
20/2 67P Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
20/3 67P Time dial(1-10 *20)/delay(0-10 * 20) byte
IEC Curve –67P Time Multiplier (.05-1.00 *200)
21/1 67P Torque Angle byte (0-355 /5)
21/2 67N Select byte (0=Disable, 1=Enable Neg Polar, 2=Enable Zero Polar, 3=Lockout Neg Polar, 4=Lockout Zero Polar)
Sensitive Earth Model (0=Disable, 1=Enable-Neg Sequence, 2=Lockout-Neg Sequence, 5=Enable-Pos Sequence, 6=Lockout Pos Sequence)
21/3 67N Curve Select byte (Type I)
22/1 67N Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
22/2 67N Time dial(1-10 *20)/delay(0-10 * 20) byte
IEC Curve –67N Time Multiplier (.05-1.00 *200)
22/3 67N Torque Angle byte (0-355 /5)
23/1 81 Select byte (0=Disable,1=81-1, 2=81-2, 3=Special)
23/2 81s-1 Pickup Frequency high byte
(60hz: 56-64 *100, 6401=Disable, 50hz: 46-54 *100, 5401=Disable)
23/3 81s-1 Pickup Frequency low byte
24/1 81s-1 Timedelay high byte (0.08-9.98 *100)
24/2 81s-1 Timedelay low byte
24/3 81r-1 Pickup Frequency high byte
(60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
25/1 81r-1 Pickup Frequency low byte
25/2 81r-1 Timedelay high byte (0-999)
25/3 81r-1 Timedelay low byte
26/1 81v Voltage Block high byte (40-200)
26/2 81v Voltage Block low byte
26/3 27 Select byte (0=Disable, 1=Enable)
27/1 27 Pickup Voltage high byte (10-200)
27/2 27 Pickup Voltage low byte
27/3 27 Timedelay byte (0-60)
28/1 79v Select byte (0=Disable, 1=Enable)
28/2 79v Pickup Voltage high byte (10-200)

28/3	79v Pickup Voltage low byte
29/1	79v Timedelay byte (4-200)
29/2	59 Select byte (0=Disable, 1=Enable)
29/3	59 Pickup Voltage high byte (70-250)
30/1	59 Pickup Voltage low byte
30/2	59 Timedelay byte (0-60)
30/3	51 P Minimum Response (0 – 60 cycles)
31/1	51 N Minimum Response (0 – 60 cycles)
31/2	50 P-1 Minimum Response (0 – 60 cycles)
31/3	50 N-1 Minimum Response (0 – 60 cycles)
32/1	Unit Configuration byte bit 0 : neutral tap range if bit 7 is 0 use range: 0=1-12A, 1=0.2-2.4A if bit 7 is 1 use range: 0=0.5-6.0A, 1=0.2-2.4A bit 1 : phase tap range if bit 7 is 0 use range: 0=1-12A, 1=0.2-2.4A if bit 7 is 1 use range: 0=1-12A, 1=0.5-6.0A bit 2 : frequency range (0=60Hz, 1=50Hz) bit 3 : cold load timer mode (0=seconds, 1=minutes) bit 4 : user definable curves (0=disabled, 1=enabled) bit 5 : recloser curves (0=disabled, 1=enabled) bit 6 : Version Select (0=ANSI, 1=IEC) bit 7 : phase & neutral tap ranges (0=1-12 and 0.2-2.4, 1=1-12, 0.2-2.4 and 0.5-6.0)
32/2	81s-2 Pickup Frequency high byte (60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
32/3	81s-2 Pickup Frequency low byte
33/1	81s-2 Timedelay high byte (0.08-9.98 *100)
33/2	81s-2 Timedelay low byte
33/3	81r-2 Pickup Frequency high byte (60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
34/1	81r-2 Pickup Frequency low byte
34/2	81r-2 Timedelay high byte (0-999)
34/3	81r-2 Timedelay low byte
35/1	Sensitive Earth Model – SEF Torque Angle (0-355 /5)
35/2	Sensitive Earth Model – SEF 50N-2 Pickup mA high byte (.005-.060 *2000)
35/3	SEF 50N-2 Pickup mA low byte
36/1	Sensitive Earth Model- Neutral Cold Load (1-254)(255= Disable)
36/2	Checksum high byte
36/3	Checksum low byte

8.4.9 Transmit Configuration Settings (3 4 11)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x4b
1/3	Total Number of Messages = 23
2/1	Phase CT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R/1500R)
2/2	Phase CT Ratio low byte
2/3	Neutral CT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R)
3/1	Neutral CT Ratio low byte
3/2	VT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R/1500R)
3/3	VT Ratio low byte
4/1	VT Connection high byte (0=69V Wye,1=120V Wye, 2=120V Delta, 3=208V Delta, 4=69V Wye 3V0 I, 5=120V Wye 3V0 I)

4/2	VT Connection low byte
4/3	Positive Sequence Reactance high byte (1-4 *1000)
5/1	Positive Sequence Reactance low byte
5/2	Positive Sequence Resistance high byte (1-4 *1000)
5/3	Positive Sequence Resistance low byte
6/1	Zero Sequence Reactance high byte (1-4 *1000)
6/2	Zero Sequence Reactance low byte
6/3	Zero Sequence Resistance high byte (1-4 *1000)
7/1	Zero Sequence Resistance low byte
7/2	Distance in Miles high byte (0.1-50 *10) IEC Version (0.1-200 *10) km
7/3	Distance in Miles low byte
8/1	Trip Failure Time high byte (5-60)
8/2	Trip Failure Time low byte
8/3	Close Failure Time high byte (18-999)
9/1	Close Failure Time low byte
9/2	Phase Rotation high byte (0=ABC, 1=ACB)
9/3	Phase Rotation low byte
10/1	Configuration Flag high byte
10/2	Configuration Flag low byte bit 0: Protection Mode (0=Fund, 1=RMS) bit 1: Reset Mode (0=Instant, 1=Delayed) bit 2: Zone Sequence (0=Disabled, 1=Enabled) bit 3: Target Display Mode (0=Last, 1=All) bit 4: Local Edit (0=Disabled, 1=Enabled) bit 5: Remote Edit (0=Disabled, 1=Enabled) bit 6: WHr/VarHr Mtr Mode (0=KWHr, 1=MWHr) bit 7: LCD Light (0=Timer, 1=On) bit 8: Multi Device Trip (0=Disabled, 1=Enabled) bit 9: VCN Special Mode (0=Normal, 1=Inverted) bit10: Cold Load Timer Mode(0=Seconds, 1=Minutes) bit11: IEC Mode Bit, Not supported as of V1.70, Reserved bit 12: 79V Timer Mode(0= sec., 1= min.) bit 13: Voltage Display Mode(0= Vln, 1= Vll) bit 14: Password Viewer (0= Disable, 1= Enable)
10/3	ALT 1 Setting Enable high byte(0=Disable, 1=Enable)
11/1	ALT 1 Setting Enable low byte
11/2	ALT 2 Setting Enable high byte(0=Disable, 1=Enable)
11/3	ALT 2 Setting Enable low byte
12/1	Demand Time Constant high byte
12/2	Demand Time Constant low byte (0=5 min, 1=15 min, 2=30 min, 3=60 min)
12/3	Sensitive Earth CT Ratio high byte (1-2000), (DPU2000R/1500R)
13/1	Sensitive Earth CT Ratio low byte
13/2-18/1	Unit Name character 1-15
18/2	OCI configuration byte (0 = disable, 1 = enable) Bit 0: OCI Control Button Bit 1: Breaker Control Button Bits 2 – 7: reserved for future use
18/3	Sensitive Earth V0 PT Ratio high byte (1-2000) , (DPU2000R/1500R)
19/1	Sensitive Earth V0 PT Ratio low byte
19/2	Spare
19/3	Spare
20/1	LCD Contrast Adjustment high byte(0-63)
20/2	LCD Contrast Adjustment low byte
20/3	Relay Password character 1
21/1	Relay Password character 2
21/2	Relay Password character 3
21/3	Relay Password character 4
22/1	Test Password character 1

22/2	Test Password character 2
22/3	Test Password character 3
23/1	Test Password character 4
23/2	Checksum high byte
23/3	Checksum low byte

8.4.10 Transmit Counter Settings (3 4 12)

NOTE: This command is used in DPU2000 versions prior to CPU V1.41.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x4c
1/3	Total Number of Messages = 9
2/1	KSI Sum A Counter high byte(0-9999)
2/2	KSI Sum A Counter low byte
2/3	KSI Sum B Counter high byte(0-9999)
3/1	KSI Sum B Counter low byte
3/2	KSI Sum C Counter high byte(0-9999)
3/3	KSI Sum C Counter low byte
4/1	Overcurrent Trip Counter high byte(0-9999)
4/2	Ovecurrent Trip Counter low byte
4/3	Breaker Operations Counter high byte(0-9999)
5/1	Breaker Operations Counter low byte
5/2	Reclose Counter 1 high byte(0-9999)
5/3	Reclose Counter 1 low byte
6/1	1st Reclose Counter high byte(0-9999)
6/2	1st Reclose Counter low byte
6/3	2nd Reclose Counter high byte(0-9999)
7/1	2nd Reclose Counter low byte
7/2	3rd Reclose Counter high byte(0-9999)
7/3	3rd Reclose Counter low byte
8/1	4th Reclose Counter high byte(0-9999)
8/2	4th Reclose Counter low byte
8/3	Reclose Counter 2 high byte(0-9999)
9/1	Reclose Counter 2 low byte
9/2	Checksum high byte
9/3	Checksum low byte

8.4.11 Transmit Alarm Settings (3 4 13)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x4d
1/3	Total Number of Messages = 13
2/1	KSI Summation Alarm Threshold high byte (1-9999,10000=Disables)
2/2	KSI Summation Alarm Threshold low byte
2/3	Overcurrent Trip Counter Alarm high byte (1-9999,10000=Disables)
3/1	Overcurrent Trip Counter Alarm Threshold low byte
3/2	Reclosure Counter 1 Alarm high byte (1-9999,10000=Disables)
3/3	Reclosure Counter 1 Alarm Threshold low byte
4/1	Phase Demand Alarm high byte (1-9999,10000=Disables)
4/2	Phase Demand Alarm low byte
4/3	Neutral Demand Alarm high byte (1-9999,10000=Disables)
5/1	Neutral Demand Alarm low byte
5/2	Low PF Alarm high byte (0.5-1.0 *100, 101=Disables)

5/3	Low PF Alarm low byte
6/1	High PF Alarm high byte (0.5-1.0 *100, 101=Disables)
6/2	High Pf Alarm low byte
6/3	Reclosure Counter 2 Alarm high byte (1-9999,10000=Disables)
7/1	Reclosure Counter 2 Alarm Threshold low byte
7/2	3 Phase kVAR Alarm high byte (10-99990 /10,10000=Disables)
7/3	3 Phase kVAR Alarm Threshold low byte
8/1	Load Current Alarm high byte (1-9999,10000=Disables)
8/2	Load Current Alarm low byte
8/3	Positive kVAR Alarm high byte (10-99990 /10,10000=Disable)
9/1	Positive kVAR Alarm low byte
9/2	Negative kVAR Alarm high byte (10-99990 /10,10000=Disable)
9/3	Negative kVAR Alarm high byte
10/1	Pos Watt Alarm 1 high byte (1-9999, 10000=Disable)
10/2	Pos Watt Alarm 1 low byte
10/3	Pos Watt Alarm 2 high byte (1-9999, 10000=Disable)
11/1	Pos Watt Alarm 2 low byte
11/2	Spare
11/3	Spare
12/1	Spare
12/2	Spare
12/3	Spare
13/1	Spare
13/2	Checksum high byte
13/3	Checksum low byte

NOTE: Positive Watt Alarm 1 and Positive Watt Alarm 2 units are displayed in either KWhr or MWhr according to bit 6 of Configuration Flag (Command 3 4 11, message 10/2). If bit is set to one, use MWhr, if bit is zero, use KWhr.

8.4.12 Transmit Real Time Clock (3 4 14)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x4e
1/3	Total Number of Messages = 4
2/1	Hours byte (0-23)
2/2	Minutes byte (0-59)
2/3	Seconds byte (0-59)
3/1	Day byte (0-31)(0=Clock shutdown)
3/2	Month byte (1-12)
3/3	Year byte (0-99)
4/1	Spare
4/2	Checksum high byte
4/3	Checksum low byte

8.4.13 Transmit Programmable Output Delays (3 4 15)

Msg Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x4f
1/3	Total Number of Messages = 8
2/1	OUT 6 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
2/2	OUT 6 delay low byte
2/3	OUT 4 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
3/1	OUT 4 delay low byte
3/2	OUT 5 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
3/3	OUT 5 delay low byte
4/1	OUT 3 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
4/2	OUT 3 delay low byte
4/3	OUT 2 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
5/1	OUT 2 delay low byte

5/2	OUT 1 delay high byte (0.00-60, DPU2000 and 0.00-250, DPU2000R/1500R, *100)
5/3	OUT 1 delay low byte
6/1	OUT 7 delay high byte (0.00-60, DPU2000)
6/2	OUT 7 delay low byte
6/3	OUT 8 delay high byte (0.00-60, DPU2000)
7/1	OUT 8 delay low byte
7/2	Spare
7/3	Spare
8/1	Spare
8/2	Checksum high byte
8/3	Checksum low byte

8.5 Transmit Buffer "35N" Commands (3 5 n)

When n=0 then the previous Receive Number command would define the number "N". Otherwise this command would take the number "N" defined by the subcmd field (1 – 15).

N	Definition
0	Repeat last command
1	Show Load Metered Data
2	Show Demand Metered Data
3	Show Maximum Peak Demand Metered Data
4	Show Minimum Peak Demand Metered Data
5	Show Load Meter Data
6	Show Average Load Current
7	Show Quick 3-Phase Meter Data
8	Send First Fault Record
9	Send Next Fault Record
10	Send First Fault Summary Record
11	Send Next Fault Summary Record
12	Send First Operation Record
13	Send Next Operation Record
14	Breaker Status (including contact inputs)
15	Power Fail Data

8.5.1 Show Load Metered Data (3 5 1)

Msg byte	Definition
1/1	Relay Status Command (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x51
1/3	Total Number of Messages = 35
2/1	Aux. Status byte Bit 0 : 0 = Wye, 1 = Delta Bit 1 : 0 = kWhr 1 = Mwhr Bit 2 : 0= V(line-neutral) , 1= V(line-line)
2/2	IA Hi byte (Load Currents)
2/3	IA Lo byte
3/1	IA Angle Hi byte
3/2	IA Angle Lo byte
3/3	IB Hi byte
4/1	IB Lo byte
4/2	IB Angle Hi byte
4/3	IB Angle Lo byte
5/1	IC Hi byte
5/2	IC Lo byte
5/3	IC Angle Hi byte
6/1	IC Angle Lo byte
6/2	IN Hi byte
6/3	IN Lo byte
7/1	IN Angle Hi byte
7/2	IN Angle Lo byte
7/3	Kvan/Kvab (Mag) Hi byte (*100)
8/1	Kvan/Kvab (Mag) Lo byte
8/2	Kvan/Kvab (Ang) Hi byte
8/3	Kvan/Kvab (Ang) Lo byte
9/1	KVbn/KVbc (Mag) Hi byte (*100)
9/2	KVbn/KVbc (Mag) Lo byte
9/3	KVbn/KVbc (Ang) Hi byte
10/1	KVbn/KVbc (Ang) Lo byte
10/2	KVcn/Kvca (Mag) Hi byte (*100)

10/3	KVcn/Kvca (Mag) Lo byte
11/1	KVcn/Kvca (Ang) Hi byte
11/2	KVcn/Kvca (Ang) Lo byte
11/3	Kwan Hi byte
12/1	Kwan Mid byte
12/2	Kwan Lo byte
12/3	KWbn Hi byte
13/1	KWbn Mid byte
13/2	KWbn Lo byte
13/3	KWcn Hi byte
14/1	KWcn Mid byte
14/2	KWcn Lo byte
14/3	KW3 Hi byte
15/1	KW3 Mid byte
15/2	KW3 Lo byte
15/3	KVARan Hi byte
16/1	KVARan Mid byte
16/2	KVARan Lo byte
16/3	KVARbn Hi byte
17/1	KVARbn Mid byte
17/2	KVARbn Lo byte
17/3	KVARcn Hi byte
18/1	KVARcn Mid byte
18/2	KVARcn Lo byte
18/3	KVAR3 Hi byte
19/1	KVAR3 Mid byte
19/2	KVAR3 Lo byte
19/3	KWHra Hi byte
20/1	KWHra Mid byte
20/2	KWHra Lo byte
20/3	KWHrb Hi byte
21/1	KWHrb Mid byte
21/2	KWHrb Lo byte
21/3	KWHrc Hi byte
22/1	KWHrc Mid byte
22/2	KWHrc Lo byte
22/3	KWHr3 Hi byte
23/1	KWHr3 Mid byte
23/2	KWHr3 Lo byte
23/3	KVARHra Hi byte
24/1	KVARHra Mid byte
24/2	KVARHra Lo byte
24/3	KVARHrb Hi byte
25/1	KVARHrb Mid byte
25/2	KVARHrb Lo byte
25/3	KVARHrc Hi byte
26/1	KVARHrc Mid byte
26/2	KVARHrc Lo byte
26/3	KVARHr3 Hi byte
27/1	KVARHr3 Mid byte
27/2	KVARHr3 Lo byte
27/3	I0 Hi byte
28/1	I0 Lo byte
28/2	I0 Angle Hi byte
28/3	I0 Angle Lo byte
29/1	I1 Hi byte
29/2	I1 Lo byte
29/3	I1 Angle Hi byte
30/1	I1 Angle Lo byte

30/2	I2 Hi byte
30/3	I2 Lo byte
31/1	I2 Angle Hi byte
31/2	I2 Angle Lo byte
31/3	KV1 Hi byte (*100)
32/1	KV1 Lo byte
32/2	KV1 Angle Hi byte
32/3	KV1 Angle Lo byte
33/1	KV2 Hi byte (*100)
33/2	KV2 Lo byte
33/3	KV2 Angle Hi byte
34/1	KV2 Angle Lo byte
34/2	Frequency Hi byte (*100)
34/3	Frequency Lo byte
35/1	Power Factor bit 0-6 : Power factor value (*100) bit 7 : 0 = Leading, 1 = Lagging
35/2	Spare
35/3	Spare

8.5.2 Show Demand Metered Data (3 5 2)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x52
1/3	Total Number of Messages = 12
2/1	Aux. Status byte (see command 3 5 1, msg 2/1)
2/2	Demand Ia Hi byte (Load Currents)
2/3	Demand Ia Lo byte
3/1	Demand Ib Hi byte
3/2	Demand Ib Lo byte
3/3	Demand Ic Hi byte
4/1	Demand Ic Lo byte
4/2	Demand In Hi byte
4/3	Demand In Lo byte
5/1	Demand Kwan Hi byte
5/2	Demand Kwan Mid byte
5/3	Demand Kwan Lo byte
6/1	Demand KWbn Hi byte
6/2	Demand KWbn Mid byte
6/3	Demand KWbn Lo byte
7/1	Demand KWcn Hi byte
7/2	Demand KWcn Mid byte
7/3	Demand KWcn Lo byte
8/1	Demand KW3 Hi byte
8/2	Demand KW3 Mid byte
8/3	Demand KW3 Lo byte
9/1	Demand KVARan Hi byte
9/2	Demand KVARan Mid byte
9/3	Demand KVARan Lo byte
10/1	Demand KVARbn Hi byte
10/2	Demand KVARbn Mid byte
10/3	Demand KVARbn Lo byte
11/1	Demand KVARcn Hi byte
11/2	Demand KVARcn Mid byte
11/3	Demand KVARcn Lo byte
12/1	Demand KVAR3 Hi byte
12/2	Demand KVAR3 Mid byte
12/3	Demand KVAR3 Lo byte

8.5.3 Show Maximum Peak Demand Metered Data (3 5 3)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x53
1/3	Total Number of Messages = 32
2/1	Aux. Status byte (see command 3 5 1, msg 2/1)
50	Peak Dem Ia Hi byte (Load Currents)
50	Peak Dem Ia Lo byte
3/1	Peak Dem Ia time yy
50	Peak Dem Ia time mn
50	Peak Dem Ia time dd
4/1	Peak Dem Ia time hh
50	Peak Dem Ia time mm
50	Peak Dem Ib Hi byte
5/1	Peak Dem Ib Lo byte
50	Peak Dem Ib time yy
50	Peak Dem Ib time mn
6/1	Peak Dem Ib time dd
50	Peak Dem Ib time hh
50	Peak Dem Ib time mm
7/1	Peak Dem Ic Hi byte
50	Peak Dem Ic Lo byte
50	Peak Dem Ic time yy
8/1	Peak Dem Ic time mn
50	Peak Dem Ic time dd
50	Peak Dem Ic time hh
9/1	Peak Dem Ic time mm
50	Peak Dem In Hi byte
50	Peak Dem In Lo byte
10/1	Peak Dem In time yy
50	Peak Dem In time mn
50	Peak Dem In time dd
11/1	Peak Dem In time hh
50	Peak Dem In time mm
50	Peak Dem Kwan Hi byte
12/1	Peak Dem Kwan Mid byte
50	Peak Dem Kwan Lo byte
50	Peak Dem Kwan time yy
13/1	Peak Dem Kwan time mn
50	Peak Dem Kwan time dd
50	Peak Dem Kwan time hh
14/1	Peak Dem Kwan time mm
50	Peak Dem KWbn Hi byte
50	Peak Dem KWbn Mid byte
15/1	Peak Dem KWbn Lo byte
50	Peak Dem KWbn time yy
50	Peak Dem KWbn time mn
16/1	Peak Dem KWbn time dd
50	Peak Dem KWbn time hh
50	Peak Dem KWbn time mm
17/1	Peak Dem KWcn Hi byte
50	Peak Dem KWcn Mid byte
50	Peak Dem KWcn Lo byte
18/1	Peak Dem KWcn time yy
50	Peak Dem KWcn time mn
50	Peak Dem KWcn time dd
19/1	Peak Dem KWcn time hh
50	Peak Dem KWcn time mm

50	Peak Dem KW3 Hi byte
20/1	Peak Dem KW3 Mid byte
50	Peak Dem KW3 Lo byte
50	Peak Dem KW3 time yy
21/1	Peak Dem KW3 time mn
50	Peak Dem KW3 time dd
50	Peak Dem KW3 time hh
22/1	Peak Dem KW3 time mm
50	Peak Dem KVARan Hi byte
50	Peak Dem KVARan Mid byte
23/1	Peak Dem KVARan Lo byte
50	Peak Dem KVARan time yy
50	Peak Dem KVARan time mn
24/1	Peak Dem KVARan time dd
50	Peak Dem KVARan time hh
50	Peak Dem KVARan time mm
25/1	Peak Dem KVARbn Hi byte
50	Peak Dem KVARbn Mid byte
50	Peak Dem KVARbn Lo byte
26/1	Peak Dem KVARbn time yy
50	Peak Dem KVARbn time mn
50	Peak Dem KVARbn time dd
27/1	Peak Dem KVARbn time hh
50	Peak Dem KVARbn time mm
50	Peak Dem KVARcn Hi byte
28/1	Peak Dem KVARcn Mid byte
50	Peak Dem KVARcn Lo byte
50	Peak Dem KVARcn time yy
29/1	Peak Dem KVARcn time mn
50	Peak Dem KVARcn time dd
50	Peak Dem KVARcn time hh
30/1	Peak Dem KVARcn time mm
50	Peak Dem KVAR3 Hi byte
50	Peak Dem KVAR3 Mid byte
31/1	Peak Dem KVAR3 Lo byte
50	Peak Dem KVAR3 time yy
50	Peak Dem KVAR3 time mn
32/1	Peak Dem KVAR3 time dd
32/2	Peak Dem KVAR3 time hh
32/3	Peak Dem KVAR3 time mm

8.5.4 Show Minimum Peak Demand Metered Data (3 5 4)

Substitute minimum peak for maximum peak and this command is the same as the Show Maximum Peak Demand Metered Data command (3 5 3), except for byte 2 of message 1. The command + subcommand (Msg 1/byte 2) is 0x54, not 0x53.

8.5.5 Show Load Metered Data (3 5 5)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x55
1/3	Total Number of Messages = 4
2/1	Aux. Status byte (see command 3 5 1, msg 2/1)
2/2	a high byte (Load Currents)
2/3	Ia (low byte)
3/1	Ib (high byte)
3/2	Ib (low byte)
3/3	Ic (high byte)
4/1	Ic (low byte)
4/2	In (high byte)

4/3	In (low byte)

8.5.6 Show Average Load Current (3 5 6)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x56
1/3	Total Number of Messages = 2
2/1	Aux. Status byte (see command 3 5 1, msg 2/1)
2/2	Iavg (high byte)
2/3	Iavg (low byte)

8.5.7 Show Quick 3-Phase Meter (3 5 7)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x57
1/3	Total Number of Messages = 4
2/1	Aux. Status (see command 3 5 1, msg 2/1)
2/2	Iavg (high byte)
2/3	Iavg (low byte)
3/1	KW3 Hi byte
3/2	KW3 Mid byte
3/3	KW3 Lo byte
4/1	KVAR3 Hi byte
4/2	KVAR3 Mid byte
4/3	KVAR3 Lo byte

8.5.8 Send First Fault Record (3 5 8)

Table 20 - Codes for Fault Element Type

Fault Element Type	Message Number
51P	0
51N	1
50P-1	2
50N-1	3
50P-2	4
50N-2	5
50P-3	6
50N-3	7
67P (DPU2000 & DPU2000R)	8
67N (DPU2000 & DPU2000R)	9
46	10
81 (DPU2000 & DPU2000R	11
Zone Step	12
ECI-1	13
ECI-2	14
SEF (for SE model)	15

Table 21 - Active Settings and Reclose Sequence Definitions

Value	Definition
0x11	Primary-1
0x12	Primary-2
0x13	Primary-3
0x14	Primary-4
0x15	Primary-Lockout
0x21	Alternate 1-1
0x22	Alternate 1-2
0x23	Alternate 1-3
0x24	Alternate 1-4
0x25	Alternate 1-Lockout
0x41	Alternate 2-1
0x42	Alternate 2-2
0x43	Alternate 2-3
0x44	Alternate 2-4
0x45	Alternate 2-Lockout

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x58
1/3	Total Number of Messages = 27
2/1	Fault Type (element) (Table 20, p. 342)
2/2	Active Set and Reclosing Sequence byte (Table 21, p. 343) bit 0-3 : 1=1, 2=2, 3=3, 4=4, 5=L bit 4-7 : 1=Prim, 2=Alt1, 4=Alt2
2/3	Fault Number (high byte)
3/1	Fault Number (low byte)
3/2	Year
3/3	Month
4/1	Day
4/2	Hours or Most significant high byte millisec time since midnight
4/3	Minutes or Most significant low byte millisec time since midnight
5/1	Seconds or Least significant high byte millisec time since midnight
5/2	Hundredths of seconds or Least significant low byte millisec time since midnight, see note below.
5/3	IA Hi byte (/i_scale see msg 8/2)
6/1	IA Lo byte
6/2	IB Hi byte (/i_scale see msg 8/2)
6/3	IB Lo byte
7/1	IC Hi byte (/i_scale see msg 8/2)
7/2	IC Lo byte
7/3	IN Hi byte (/i_scale see msg 8/2)
8/1	IN Lo byte
8/2	Current Scale (0,1 : i_scale=1, 10 : i_scale=10)
8/3	Spare
9/1	Ia Angle (Hi byte)
9/2	Ia Angle (Lo byte)
9/3	Ib Angle (Hi byte)
10/1	Ib Angle (Lo byte)
10/2	Ic Angle (Hi byte)
10/3	Ic Angle (Lo byte)
11/1	In Angle (Hi byte)
11/2	In Angle (Lo byte)
11/3	Zero Seq I (Mag) Hi byte (/i_scale see msg 8/2)
12/1	Zero Seq I (Mag) Lo byte
12/2	Pos Seq I (Mag) Hi byte (/i_scale see msg 8/2)

12/3	Pos Seq I (Mag) Lo byte
13/1	Neg Seq I (Mag) Hi byte (/i_scale see msg 8/2)
13/2	Neg Seq I (Mag) Lo byte
13/3	Zero Seq I (Ang) Hi byte
14/1	Zero Seq I (Ang) Lo byte
14/2	Pos Seq I (Ang) Hi byte
14/3	Pos Seq I (Ang) Lo byte
15/1	Neg Seq I (Ang) Hi byte
15/2	Neg Seq I (Ang) Lo byte
15/3	Kvab/Kvan (Mag) Hi byte (*100)
16/1	Kvab/Kvan (Mag) Lo byte (*100)
16/2	KVbc/KVbn (Mag) Hi byte (*100)
16/3	KVbc/KVbn (Mag) Lo byte (*100)
17/1	Kvca/KVcn (Mag) Hi byte (*100)
17/2	Kvca/KVcn (Mag) Lo byte (*100)
17/3	Vab/Van (Ang) Hi byte
18/1	Vab/Van (Ang) Lo byte
18/2	Vbc/Vbn (Ang) Hi byte
18/3	Vbc/Vbn (Ang) Lo byte
19/1	Vca/Vcn (Ang) Hi byte
19/2	Vca/Vcn (Ang) Lo byte
19/3	Pos Seq KV (Mag) Hi byte (*100)
20/1	Pos Seq KV (Mag) Lo byte
20/2	Neg Seq KV (Mag) Hi byte (*100)
20/3	Neg Seq KV (Mag) Lo byte
21/1	Pos Seq V (Ang) Hi byte
21/2	Pos Seq V (Ang) Lo byte
21/3	Neg Seq V (Ang) Hi byte
22/1	Neg Seq V (Ang) Lo byte
22/2	Fault location (high byte) (*10)
22/3	Fault location (low byte)
23/1	Fault impedance, real part (high byte) (*1000)
23/2	Fault impedance, real part |
23/3	Fault impedance, real part |
24/1	Fault impedance, real part (low byte)
24/2	Breaker Operate Time (high byte) (*1000)
24/3	Breaker Operate Time |
25/1	Breaker Operate Time |
25/2	Breaker Operate Time (low byte)
25/3	Relay Operate Time (high byte) (*1000)
26/1	Relay Operate Time |
26/2	Relay Operate Time |
26/3	Relay Operate Time (low byte)
27/1	Record Status (high byte)
27/2	Record Status (low byte) bit 0 : 0 = Wye Connection , 1 = Delta Connection bit 1 : 0 = Fault , 1 = Event Capture
27/3	Spare

If no fault data entry is present then send all 0s for 2/1 through 27/3.

NOTE: If IRIG is enabled using Enable-mmm option in Communications Command, then the most significant bit of the hour byte will be set to indicate that the four time bytes (Hours, Minutes, Seconds, and Hundreths of Seconds should be combined to form a long value indicating the time in milliseconds since midnight.

8.5.9 Send Next Fault Record (3 5 9)

Same format as (3 5 8) except Msg 1/2 = 0x59.

8.5.10 Send First Fault Summary Record (3 5 10)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x5a
1/3	Total Number of Messages = 8
2/1	Fault Type (element) (Table 20, p. 342)
2/2	Active Set and Reclosing Sequence byte bit 0-3 : 1=Prim, 2=Alt1, 4=Alt2 bit 4-7 : 1=1, 2=2, 3=3, 4=4, 5=L
2/3	Fault Number (high byte)
3/1	Fault Number (low byte)
3/2	Year
3/3	Month
4/1	Day
4/2	Hours or Most significant high byte millisec time since midnight
4/3	Minutes or Most significant low byte millisec time since midnight
5/1	Seconds or Least significant high byte millisec time since midnight
5/2	Hundredths of seconds or Least significant low byte millisec time since midnight, see note in command 3 5 8.
5/3	IA Hi byte (/i_scale see msg 8/2)
6/1	IA Lo byte
6/2	IB Hi byte (/i_scale see msg 8/2)
6/3	IB Lo byte
7/1	IC Hi byte (/i_scale see msg 8/2)
7/2	IC Lo byte
7/3	IN Hi byte (/i_scale see msg 8/2)
8/1	IN Lo byte
8/2	Current Scale (0,1 : i_scale=1, 10 : i_scale=10)
8/3	Spare

If no fault data entry is present then send all 0s for 2/1 through 8/3.

8.5.11 Send Next Fault Summary Record (3 5 11)

Same format as (3 5 10) except Msg 1/2 = 0x5b.

8.5.12 Send First Operations Record (3 5 12)

Table 22 - Operation Record Definitions

Index	Operation Record Description
0	51P Trip
1	51N Trip
2	50P-1 Trip
3	50N-1 Trip
4	50P-2 Trip
5	50N-2 Trip
6	50P-3 Trip
7	50N-3 Trip
8	67P Trip
9	67N Trip
10	46 Trip
11	27-1P Alarm
12	59 Alarm
13	79V Block
14	81S-1 Trip
15	81R-1 Restore
16	81V Block

Index	Operation Record Description
17	TOC Pickup-No Trip
18	27-3P Alarm
19	SEF Trip
20	External Trip
21	External Close
22	Breaker Opened
23	Breaker Closed
24	Open Trip Contact
25	Recloser Lockout
26	Direct Trip
27	Direct Close
28	MDT Close
29	Ext. Trip and ARC
30	Reclose Initiated
31	CB Failed To Trip
32	CB Failed To Close
33	CB Pops Open
34	CB Pops Closed
35	CB State Unknown
36	CB Stuck Closed
37	Ext. Trip CB Stuck
38	Springs Discharged
39	- reserved for future use -
40	Manual Trip
41	Manual Close
42	Ground TC Enabled
43	Ground TC Disabled
44	Phase TC Enabled
45	Phase TC Disabled
46	Primary Set Active
47	Alt1 Set Active
48	Alt2 Set Active
49	Zone Step
50	Recloser Enabled
51	Recloser Disabled
52	Zone Seq Enabled
53	Zone Seq Disabled
54	50P/N-1 Disabled
55	50P/N-2 Disabled
56	50P/N-3 Disabled
57	50P/N-1 Enabled
58	50P/N-2 Enabled
59	50P/N-3 Enabled
60	81S-2 Trip
61	81R-2 Restore
62	81O-1 Overfreq.
63	81O-2 Overfreq
64	CloseFailed/NoSync
65	LBLL
66	LBDL
67	DBLL
68	DBDL
69	SOFTWARE ERROR
70	Blown Fuse Alarm
71	OC Trip Counter
72	Accumulated KSI
73	79 Counter1 Alarm
74	Phase Demand Alarm

Index	Operation Record Description
75	Neutral Demand Alm
76	Low PF Alarm
77	High PF Alarm
78	Trip Coil Failure
79	kVAR Demand Alarm
80	79 Counter2 Alarm
81	Pos. kVAR Alarm
82	Neg. kVAR Alarm
83	Load Alarm
84	Cold Load Alarm
85	Pos. Watt Alarm 1
86	Pos. Watt Alarm 2
87	32P Trip
88	32N Trip
89	- reserved for future use -
90	Event Capture #1
91	Event Capture #2
92	Waveform Capture
93	BFT Operation
94	ReTrip Operation
95	Ext. BFI Enabled
96	Ext. BFI Disabled
97	BFI Enabled
98	BFI Disabled
99	- reserved for future use -
100	ROM Failure
101	RAM Failure
102	Self Test Failed
103	EEPROM Failure
104	BATRAM Failure
105	DSP Failure
106	Control Power Fail
107	Editor Access
108	System Reboot Init.
109	Interrupt Overlap
110	DSP COP Status
111	System Booting
112	- reserved for future use -
113	- reserved for future use -
114	- reserved for future use -
115	Suprvsr Stack Pointer
116	User Stack Pointer
117	Task Control Block
118	Stack Base
119	Task Address
120	- reserved for future use -
121	- reserved for future use -
122	- reserved for future use -
123	- reserved for future use -
124	- reserved for future use -
125	- reserved for future use -
126	- reserved for future use -
127	- reserved for future use -
128	Springs Charged
129	Springs Discharged
130	79S Input Enabled
131	79S Input Disabled
132	79M Input Enabled

Index	Operation Record Description
133	79M Input Disabled
134	TCM Input Closed
135	TCM Input Opened
136	ALT1 Input Enabled
137	ALT1 Input Disabled
138	ALT2 Input Enabled
139	ALT2 Input Disabled
140	Ext Trip Enabled
141	Ext Trip Disabled
142	Event Cap1 Init
143	Event Cap1 Reset
144	Event Cap2 Init
145	Event Cap2 Reset
146	Wave Cap. Init
147	Wave Cap. Reset
148	Ext Close Enabled
149	Ext Close Disabled
150	52a Closed
151	52a Opened
152	52b Closed
153	52b Opened
154	43a Closed
155	43a Opened
156	46 Unit Enabled
157	46 Unit Disabled
158	67P Unit Enabled
159	67P Unit Disabled
160	67N Unit Enabled
161	67N Unit Disabled
162	ULI1 Input Closed
163	ULI1 Input Opened
164	ULI2 Input Closed
165	ULI2 Input Opened
166	ULI3 Input Closed
167	ULI3 Input Opened
168	ULI4 Input Closed
169	ULI4 Input Opened
170	ULI5 Input Closed
171	ULI5 Input Opened
172	ULI6 Input Closed
173	ULI6 Input Opened
174	ULI7 Input Closed
175	ULI7 Input Opened
176	ULI8 Input Closed
177	ULI8 Input Opened
178	ULI9 Input Closed
179	ULI9 Input Opened
180	CRI Input Closed
181	CRI Input Opened
182	ARC Blocked
183	ARC Enabled
184	TARC Input Opened
185	SEF Enabled
186	SEF Disabled
187	User Display On
188	User Display Off
189	Sync Check Enabled
190	Sync Check Disabled

Index	Operation Record Description
191	Lines Synced
192	Line Sync Lost
193	CB Slow To Trip
194	Supervisory Disable
195	Supervisory Enabled
196	Sync Bypass Enabled
197	Sync Bypass Disable
198	Failed to Sync
199	Catalog Nmbr Updtd
200	- reserved for future use -
201	- reserved for future use -
202	- reserved for future use -
203	- reserved for future use -
204	- reserved for future use -
205	- reserved for future use -
206	- reserved for future use -
207	- reserved for future use -
208	- reserved for future use -
209	- reserved for future use -
210	- reserved for future use -
211	- reserved for future use -
212	- reserved for future use -
213	- reserved for future use -
214	- reserved for future use -
215	59G Alarm
216	TGT Enabled
217	TGT Disabled
218	SIA Enabled
219	SIA Disabled
220	LIS Asserted
221	LIR Asserted
222	LIS Deasserted
223	LIR Deasserted
224	LO Asserted
225	LO Deasserted
226	TR_SET Asserted
227	TR_RST Asserted
228	TR_SET Deasserted
229	TR_RST Deasserted
230	TR_ON Asserted
231	TR_OFF Asserted
232	TR_TAG Asserted
233	59-3P Alarm
234	47 Alarm
235	21P-1 Zone 1 Trip
236	21P-2 Zone 2 Trip
237	21P-3 Zone 3 Trip
238	21P-4 Zone 4 Trip
239	ULI10 Input Closed
240	ULI10 Input Opened
241	ULI11 Input Closed
242	ULI11 Input Opened
243	ULI12 Input Closed
244	ULI12 Input Opened
245	ULI13 Input Closed
246	ULI13 Input Opened
247	ULI14 Input Closed
248	ULI14 Input Opened

Index	Operation Record Description
249	ULI15 Input Closed
250	ULI15 Input Opened
251	ULI16 Input Closed
252	ULI16 Input Opened
253	46A Trip
254	46A Unit Enabled
255	46A Unit Disabled
256	Not applicable!!

Note – the operation record index can not be greater than 255.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x5c
1/3	Total Number of Messages = 5
2/1	Year
2/2	Month
2/3	Day
3/1	Hours or Most significant high byte millisec time since midnight
3/2	Minutes or Most significant low byte millisec time since midnight
3/3	Seconds or Least significant high byte millisec time since midnight
4/1	Hundredths of seconds or Least significant low byte millisec time since midnight, see note in command 3 5 8.
4/2	Message Number
4/3	Value (if any) Hi byte
5/1	Value (if any) Lo byte
5/2	Operation Number (high byte)
5/3	Operation Number (low byte)

If the operation entry doesn't exist then send 0's in all the bytes 2/1 through 5/3.

8.5.13 Send Next Operations Record (3 5 13)

Same format as (3 5 12) except Msg 1/2 = 0x5d.

8.5.14 Breaker Status (Including I/O Status) (3 5 14)

Input status bit 0=opened, 1=closed.
Output status bit 0=de-energized, 1=energized.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x5e
1/3	Total Number of Messages = 3
2/1	Contact Input Status (high byte) Bit 0 – Input 6 (DPU2000 and DPU2000R) Bit 1 – Input 7 (DPU2000 and DPU2000R) Bit 2 – Input 8 (DPU2000 and DPU2000R) or Input 6 (DPU1500R) Bit 3 – Input 9 (DPU2000) Bit 4 – Input 10 (DPU2000) Bit 5 – Input 11 (DPU2000) Bit 6 – Input 12 (DPU2000) Bit 7 – Input 13 (DPU2000)
2/2	Contact Input Status (low byte) Bit 0 – 52a (DPU2000) Bit 1 – 52b (DPU2000) Bit 2 – 43a (DPU2000)

Bit 3 – Input 1
Bit 4 – Input 2
Bit 5 – Input 3
Bit 6 – Input 4
Bit 7 – Input 5

2/3 Self Test Status (high byte)
Bit 0 – DSP ROM
Bit 1 – DSP Internal RAM
Bit 2 – DSP External RAM
Bit 3 – DSP +/-5V
Bit 4 – DSP +/-15V
Bit 5 – DSP +5V
Bit 6 – DSP Comm. Failure
Bit 7 – ADC Failure

3/1 Self Test Status (low byte)
Bit 0 – CPU RAM
Bit 1 – CPU EPROM
Bit 2 – CPU NVRAM
Bit 3 – CPU EEPROM
Bit 4 –
Bit 5 –
Bit 6 –
Bit 7 –

3/2 Output Contact Status (high byte)
Bit 0 – Output 7 (DPU2000)
Bit 1 – Output 8 (DPU2000)

3/3 Output Contact Status (low byte)
Bit 0 – Trip
Bit 1 – Close (DPU2000)
Bit 2 – Output 1
Bit 3 – Output 2
Bit 4 – Output 3
Bit 5 – Output 4
Bit 6 – Output 5
Bit 7 – Output 6

8.5.15 Power Fail Data (3 5 15)

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0x5f
1/3	Total Number of Messages = 4
2/1	Year
2/2	Month
2/3	Day
3/1	Hour
3/2	Minute
3/3	Second
4/1	Hundredths of second
4/2	Power Fail Type Bit 0: DC Control Bit 1: +5/+15V
4/3	Breaker Status (state)

8.6 Load Profile/Record Commands (3 6 n)

N	Definition
0	Define Load Profile Settings
1	Start Load Profile Data Accumulation
2	Freeze Load Profile Data
3	Report Load Profile Header-All
4	Report Next Load Profile Data Block
5	Retransmit Last Load Profile Data Block
6	Report Load Profile Header-Last
8	Report Oldest Unreported Fault Record
9	Report Oldest Unreported Operations Record

8.6.1 Load Profile Settings (3 6 0)

Reserved for user configuration.

8.6.2 Accumulate Load Profile Data (3 6 1)

Start load profile data collection.

8.6.3 Freeze Load Profile Data (3 6 2)

Stop load profile data collection.

8.6.4 Report Load Profile Data Header (All Data) (3 6 3)

This command is used to initialize the unit to report the entire contents of the accumulated load profile.

Msg byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2-4/1	Report Column (1-9) Attribute Number
4/2	spare
4/3-9/3	Unit Id Name (16 chars)
10/1-11/2	Time Tag of the first Block reporting (5 bytes :yy,mn,dd,hh,mm in order)
11/3	spare
12/1-12/2	Report Column 1 Attribute Scale (high, low byte)
12/3-17/3	Report Column (2-9) Attribute Scale

Attr#	Description	Dynamic Scale
0	Demand kW-A	122
1	Demand kW-B	122
2	Demand kW-C	122
3	Demand kVar-A	122
4	Demand kVar-B	122
5	Demand kVar-C	122
6	Van	10
7	Vbn	10
8	Vcn	10
9	Demand kW-3P	367
10	Demand kVar-3P	367
11	Demand Ia	1
12	Demand Ib	1
13	Demand Ic	1
14	Vab	10
15	Vbc	10
16	Vca	10

8.6.5 Report Next Load Profile Data Block (3 6 4)

Msg byte	Definition
1/1	Demand Interval (5/15/30/60 Mins)
1/2-1/3	Record # (a number starting from 1 to #of blocks)
2/1	Total Number Data Bytes (1 through 126)
2/2-3/3	Time Tag of the first Block (5 bytes : hh,mm,dd,mn,yy in order) **NOTE**: Different than command 363 time stamp
4/1-45/3	Data Blocks (up to 126 bytes of data)

Each data block is a two-byte word that has the following bit configuration:

bit 0-13:	data values
bit 14:	sign bit (1=multiply bits 0-13 by –1)
bit 15:	scale bit (0=multiply bits 0-13 by 1, 1=multiply bits 0-13 by attribute scale)

Example: Report column 1 is profiling attribute #0 (Demand kW-A) and has a dynamic scale = 122

Data word	Binary pattern	Scale	Reported value
8,000	0001111101000000	1	8,000 kW
24,384	0101111101000000	-1	-8,000 kW
16,776	0100000011000100	122	23,912 kW
49,384	1100000011000100	-122	-23,912 kW

To obtain the reported value column from the data word, a listing for a C routine should look as follows:

```
long int  ConvertData(unsigned short ,unsigned short );
long int                report_value;
unsigned short int      data_word;

report_value = ConvertData( data_word ,attribute_scale);
{
        int scale=1;

        if ( data_word & 0x4000 ) /* is sign bit set ? */
        {
           scale = -1;
        }

        if ( data_word & 0x8000 ) /* is scale bit set ? */
        {
           scale *= attribute_scale;
        }

        return( (data_word & 0x3fff) * scale );
}
```

8.6.6 Retransmit the Last Load Profile Data Block (3 6 5)

Same as Report Next Load Profile Data Block except it's the previous data sent.

8.6.7 Report Load Profile Data Header(Last Data) (3 6 6)

This command is used to initialize the unit to report the entire contents of the accumulated load profile.

8.6.8 Oldest Unreported Fault Record (3 6 8)

This command will report the oldest unreported fault record. The 3 0 4 command can be issued to determine how many unreported records exist in units queue. The issuance of the 3 6 8 command will decrement the counter by one record.

Unreported Command byte (0=Get Oldest Unreported, 1= Get Last Reported)

Data Byte	Definition
1/1	Unreported Command Byte
1/2	Unreported Command Byte (Duplicate)
1/3	Unreported Command Byte (Triplicate)

Msg Byte	Definition

Same format as (3 5 8) except Msg 1/2 = 0x68.

8.6.9 Oldest Unreported Operations Record (3 6 9)

This command will report the oldest unreported operations record. The 3 0 4 command can be issued to determine how many unreported records exist in units queue. The issuance of the 3 6 9 command will decrement the counter by one record.

Unreported Command byte (0=Get Oldest Unreported, 1= Get Last Reported)

Data Byte	Definition
1/1	Unreported Command Byte
1/2	Unreported Command Byte (Duplicate)
1/3	Unreported Command Byte (Triplicate)

Msg Byte	Definition

Same format as (3 5 12) except Msg 1/2 = 0x69.

8.7 Miscellaneous Commands (3 9 n)

N	Definition
0	Trip Command
1	Close Command
2	Energize Output Contact Command
3	Set/Reset Output Contacts Command
4	Close Command-Independent of 43A
5	Set Forced Physical Inputs Command
6	Forced Logical Inputs Information
7	Forced Physical Outputs Command

8.7.1 Trip Command (3 9 0)

The TRIP command will be issued to the DPU. This command has a data message that contains the Password and a command verification code for trip. NOTE: To issue the trip command, the DPU2000 must be in the CLOSED state, 52A closed and 52B opened.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0x90

8.7.2 CLOSE Command (3 9 1)

The CLOSE command will be issued to the DPU. This command has a data message that contains the Password and a command verification code for Close. NOTE: To issue the close command, the DPU2000 must be in the OPEN state and the 43A input must be asserted, 52A opened, 52B closed and 43A closed.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0x91

8.7.3 Energize Output Contact Command (3 9 2)

The test output contact command would be issued to the DPU. This command has a data message that contains the Password and a command verification code and a 16-bit word indicating which contacts should be closed.

The output contact will be a momentary closure for the time period specified in the configuration menu for trip failure time.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0x92
3/1	Output Contact State (high byte) Bit 0 – OUT7 (DPU2000) Bit 1 – OUT8 (DPU2000) Bit 2-7 – Spare
3/2	Output Contact State (low byte) Bit 0 – TRIP Bit 1 – CLOSE (DPU2000)

Bit 2 – OUT1
Bit 3 – OUT2
Bit 4 – OUT3
Bit 5 – OUT4
Bit 6 – OUT5
Bit 7 – OUT6

3/3 Output Contact State Confirmation (high byte)
Bit 0 – OUT7 (DPU2000)
Bit 1 – OUT8 (DPU2000)
Bit 2-7 – Spare

4/1 Output Contact State Confirmation (low byte)
Bit 0 – TRIP
Bit 1 – CLOSE (DPU2000)
Bit 2 – OUT1
Bit 3 – OUT2
Bit 4 – OUT3
Bit 5 – OUT4
Bit 6 – OUT5
Bit 7 – OUT6

4/2 Checksum high byte
4/3 Checksum low byte

8.7.4 Set/Reset Output Contacts Command (3 9 3)

This command allows for the assertion/deassertion of the ULO1-9 logical outputs. It also provides the means to reset the sealed in logical output contacts. Outputs denoted with '*' are sealed in and can only be reset.

Bit = 0, Output Not Energized/No Change in Status.
Bit = 1, Output Energized/Change in Status.

Bit	Output Byte1	Output Byte2	Output Byte3
7	27*	51P*	27-3P*
6	46*	51N*	TRIPA*
5	50P-1*	59* (DPU2000/R)	TRIPB*
4	50N-1*	67P* (DPU2000/R)	TRIPC*
3	50P-2*	67N* (DPU2000/R)	ULO1 (DPU2000/R)
2	50N-2*	81S-1* (DPU2000/R)	ULO2 (DPU2000/R)
1	50P-3*	81R-1* (DPU2000/R)	ULO3 (DPU2000/R)
0	50N-3*	81O-1* (DPU2000/R)	ULO4 (DPU2000/R)

Bit	Output Byte4	Output Byte5	Output Byte6
7	ULO5 (DPU2000/R)	79CA1*	25* (DPU2000R w/Synch Check)
6	ULO6 (DPU2000/R)	79CA2*	59G* (DPU2000R)
5	ULO7 (DPU2000/R)	SEF* (SE Models, DPU2000R/1500R)	59-3p* (DPU2000R)
4	ULO8 (DPU2000/R)	BFT* (DPU2000/R)	47* (DPU2000R)
3	ULO9 (DPU2000/R)	RETRIP* (DPU2000/R)	21P-1* (DPU2000R)
2	81O-2* (DPU2000/R)	32P-2* (DPU2000/R)	21P-2* (DPU2000R)
1	81S-2* (DPU2000/R)	32N-2* (DPU2000/R)	21P-3* (DPU2000R)
0	81R-2* (DPU2000/R)	BFA*	21P-4* (DPU2000R)

Bit	Output Byte7	Output Byte8
7		
6		
5		
4		
3		
2		
1		

0

Example: To Send a command to clear 27-3P* and set ULO4 the following command bytes should be issued:

Set/Reset Output Byte3 = 01 hex
Status Change Output Byte3 = 81 hex

This allows a change to occur for outputs in bit position 7 and 0. Note you can only clear "*" outputs.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0x93
3/1	Set/Reset Output Byte 1
3/2	Set/Reset Output Byte 2
3/3	Set/Reset Output Byte 3
4/1	Set/Reset Output Byte 4
4/2	Set/Reset Output Byte 5
4/3	Set/Reset Output Byte 6
5/1	Set/Reset Output Byte 7
5/2	Set/Reset Output Byte 8
5/3	Spare
6/1	Spare
6/2	Spare
6/3	Spare
7/1	Status Change Output Byte 1
7/2	Status Change Output Byte 2
7/3	Status Change Output Byte 3
8/1	Status Change Output Byte 4
8/2	Status Change Output Byte 5
8/3	Status Change Output Byte 6
9/1	Status Change Output Byte 7
9/2	Status Change Output Byte 8
9/3	Spare
10/1	Spare
10/2	Spare
10/3	Spare
11/1	Spare
11/2	Checksum high byte
11/3	Checksum low byte

8.7.5 CLOSE Command (3 9 4)

The CLOSE command will be issued to the DPU. This command has a data message that contains the Password and a command verification code for Close. NOTE: To issue the close command, the DPU2000 must be in the OPEN state (independent of 43A input).

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0x94

8.7.6 Force Physical Input (3 9 5)

This command is available in DPU2000R and DPU1500R.

This command is issued to the unit and contains a data message that indicates the Password and a command verification code plus two 16 bit words, Normal State mask and Forcing State mask, which indicate which inputs to force and the state to which they are being forced. If the bit specific to an input is reset in the Normal State mask then all input operations for that input will proceed according to normal logical conditions. If the Normal State mask bit specific to an input is set then all input operations for that input will be ignored and the Forcing State mask will be utilized to force the input condition indicated by the Forcing State mask.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0x95
3/1	high byte of Change state mask
3/2	low byte of Change state mask
3/3	high byte of Normal state mask
4/1	low byte of Normal state mask
4/2	high byte of Forcing state mask
4/3	low byte of Forcing state mask
5/1	Spare
5/2	Spare
5/3	Spare
6/1	Spare
6/2	Checksum high byte
6/3	Checksum low byte

Change State mask (Bit definition):
0 = No change, 1 = Associated input is defined by the states in the Normal and Forcing masks. Refer to Figure 14 (p. 365) for the bit assignments.

Normal State mask (Bit definition):
0 = Normal State, 1 = Normal State over ride. Refer to Figure 14 (p. 365) for the bit assignments.

Forcing State mask (Bit definition):
0 = Forcing Reset state, 1 = Forcing Set State. Refer to Figure 14 (p. 365) for the bit assignments.

8.7.7 Force Logical Input (3 9 6)

This command is available in DPU2000R and DPU1500R.

This command is issued to the unit and contains a data message that indicates the Password and a command verification code plus four 32 bit words, the Normal State masks and Forcing State masks, which indicate which inputs to force and the state to which they are being forced. If the bit specific to an input is reset in the Normal State masks then all input operations for that input will proceed according to normal logical conditions. If the Normal State mask bit specific to an input is set in the Normal State masks then all input operations for that input will be ignored and the Forcing State mask will be utilized to force the input condition indicated by the Forcing State mask.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0x96
3/1	Most significant high byte of 1st unsigned long word Change state mask
3/2	Most significant low byte of 1st unsigned long word for Change state mask
3/3	Least significant high byte of 1st unsigned long word Change state mask
4/1	Least significant low byte of 1st unsigned long word for Change state mask
4/2	Most significant high byte of 1st unsigned long word for Normal State mask
4/3	Most significant low byte of 1st unsigned long word for Normal State mask

5/1	Least significant high byte of 1st unsigned long word for Normal State mask
5/2	Least significant low byte of 1st unsigned long word for Normal State mask
5/3	Most significant high byte of 1st unsigned long word for Forcing State mask
6/1	Most significant low byte of 1st unsigned long word for Forcing State mask
6/2	Least significant high byte of 1st unsigned long word for Forcing State mask
6/3	Least significant low byte of 1st unsigned long word for Forcing State mask
7/1	Spare
7/2	Spare
7/3	Spare
8/1	Spare
8/2	Checksum high byte
8/3	Checksum low byte

Both unsigned long words for the Change State mask, the Normal State mask and the Forcing State mask, break down as follows for the DPU2000R and DPU1500R:

Bits 31:FLI31	Bits 23:FLI23	Bits 15: FLI15	Bits 07: FLI07
Bits 30:FLI30	Bits 22:FLI22	Bits 14: FLI14	Bits 06: FLI06
Bits 29:FLI29	Bits 21:FLI21	Bits 13: FLI13	Bits 05: FLI05
Bits 28:FLI28	Bits 20:FLI20	Bits 12: FLI12	Bits 04: FLI04
Bits 27:FLI27	Bits 19:FLI19	Bits 11: FLI11	Bits 03: FLI03
Bits 26:FLI26	Bits 18:FLI18	Bits 10: FLI10	Bits 02: FLI02
Bits 25:FLI25	Bits 17:FLI17	Bits 09: FLI09	Bits 01: FLI01
Bits 24:FLI24	Bits 16:FLI16	Bits 08: FLI08	Bits 00: FLI00

8.7.8 Force Physical Output Contact Command (3 9 7)

This command is available in DPU2000R and DPU1500R.

This command is issued to the unit and contains a data message that indicates the Password and a command verification code plus two 16 bit words, Normal State mask and Forcing State mask, which indicate which outputs to force and the state to which they are being forced. If the bit specific to an output is reset in the Normal State mask then all output operations for that output will proceed according to normal logical conditions. If the Normal State mask bit specific to an output is set then all output operations for that output will be ignored and the Forcing State mask will be utilized to force the output condition indicated by the Forcing State mask.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0x97
3/1	high byte of Change state mask
3/2	low byte of Change state mask
3/3	high byte of Normal state mask
4/1	low byte of Normal state mask
4/2	high byte of Forcing state mask
4/3	low byte of Forcing state mask
5/1	Spare
5/2	Spare
5/3	Spare
6/1	Spare
6/2	Checksum high byte
6/3	Checksum low byte

Change State mask (Bit definition):
0 = No change, 1 = Associated input is defined by the states in the Normal and Forcing masks. Refer to Figure 15 (p. 369) for the bit assignments.

Normal State mask (Bit definition):

0 = Normal State, 1 = Normal State over ride. Refer to Figure 15 (p. 369) for the bit assignments.

Forcing State mask (Bit definition):
0 = Forcing Reset state, 1 = Forcing Set State. Refer to Figure 15 (p. 369) for the bit assignments.

8.8 Receive Buffer "N" Commands (3 10 n)

N	Definition
0	Reserved for repeat 3 10 n
1	Communications Settings
2	Counter Settings
3	Master Trip Output Assignment
4	Breaker Failure Settings

8.8.1 Receive Communications Settings (3 10 1)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Port configuration byte

bit 0-3 = port baud rate (0=300,1=1200,2=2400,3=4800, 4=9600,5=19200,6=38400)
bit 4-5 = parity (0=None, 1=Odd,2=Even)
bit 6 = number of data bits (0=seven, 1=eight)
bit 7 = number of stop bits (0=one, 1=two)

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xa1
3/1	Unit Address high byte
3/2	Unit Address low byte
3/3	Front Panel RS232 configuration byte
4/1	Rear Panel RS232 or INCOM configuration byte
4/2	Rear Panel RS485 configuration byte
4/3	Rear Panel IRIG byte (0=Disable; 1=Enable-cc, time stamp reporting will be HH:MM:SS.cc; 2=Enable-mmm, time stamp reporting will be HH:MM:SS.mmm)
5/1	Spare
5/2	Spare
5/3	Aux Port Parameter 1 byte (0-255)
6/1	Aux Port Parameter 2 byte (0-255)
6/2	Aux Port Parameter 3 byte (0-255)
6/3	Aux Port Parameter 4 byte (0-255)
7/1	Aux Port Parameter 5 byte (0-255)
7/2	Aux Port Parameter 6 byte (0-255)
7/3	Aux Port Parameter 7 byte (0-255)
8/1	Aux Port Parameter 8 byte (0-255)
8/2	Aux Port Parameter 9 byte (0-255)
8/3	Aux Port Parameter 10 byte (0-255)
9/1	Aux Port Parameter Mode byte (0-255) Bit 0: Par Mode 1 (0=Disable, 1=Enable) Bit 1: Par Mode 2 (0=Disable, 1=Enable) Bit 2: Par Mode 3 (0=Disable, 1=Enable) Bit 3: Par Mode 4 (0=Disable, 1=Enable) Bit 4: Par Mode 5 (0=Disable, 1=Enable) Bit 5: Par Mode 6 (0=Disable, 1=Enable) Bit 6: Par Mode 7 (0=Disable, 1=Enable) Bit 7: Par Mode 8 (0=Disable, 1=Enable)
9/2	Spare
9/3	Spare

10/1	Spare
10/2	Checksum high byte
10/3	Checksum low byte

8.8.2 Receive Counter Settings (3 10 2)

NOTE: Overcurrent Trip Counters A, B, C, and N are available with Recloser Curve Software option, catalog numbers XXXXXXXX-XXX2X or XXXXXXXX-XXX3X. In DPU2000 series, CPU V1.41 or higher is required for the Recloser Curve Software option.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xa2
3/1	KSI Sum A Counter high byte(0-9999)
3/2	KSI Sum A Counter low byte
3/3	KSI Sum B Counter high byte(0-9999)
4/1	KSI Sum B Counter low byte
4/2	KSI Sum C Counter high byte(0-9999)
4/3	KSI Sum C Counter low byte
5/1	Over Current Trip Counter high byte (0-9999)
5/2	Over Current Trip Counter low byte
5/3	Breaker Operations Counter high byte (0-9999)
6/1	Breaker Operations Counter low byte
6/2	Reclose Counter 1 high byte (0-9999)
6/3	Reclose Counter 1 low byte
7/1	1st Reclose Counter high byte (0-9999)
7/2	1st Reclose Counter low byte
7/3	2nd Reclose Counter high byte (0-9999)
8/1	2nd Reclose Counter low byte
8/2	3rd Reclose Counter high byte (0-9999)
8/3	3rd Reclose Counter low byte
9/1	4th Reclose Counter high byte (0-9999)
9/2	4th Reclose Counter low byte
9/3	Reclose Counter 2 high byte (0-9999)
10/1	Reclose Counter 2 low byte
10/2	Overcurrent Trip A Counter high byte (0-9999), (DPU2000/R)
10/3	Overcurrent Trip A Counter low byte
11/1	Overcurrent Trip B Counter high byte (0-9999), (DPU2000/R)
11/2	Overcurrent Trip B Counter low byte
11/3	Overcurrent Trip C Counter high byte (0-9999), (DPU2000/R)
12/1	Overcurrent Trip C Counter low byte
12/2	Overcurrent Trip N Counter high byte (0-9999), (DPU2000/R)
12/3	Overcurrent Trip N Counter low byte
13/1	SPARE
13/2	SPARE
13/3	SPARE
14/1	SPARE
14/2	SPARE
14/3	SPARE
15/1	SPARE
15/2	SPARE
15/3	SPARE
16/1	SPARE
16/2	Checksum high byte
16/3	Checksum low byte

8.8.3 Receive Master Trip Output Assignment (3 10 3)

NOTE: DPU2000 series requires CPU version 1.70 and above.

Msg/Byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xa3
3/1	Master Trip Assignment, Byte 1 Bit 0: SPARE Bit 1: SPARE Bit 2: SPARE Bit 3: SPARE Bit 4: SPARE Bit 5: SPARE Bit 6: SPARE Bit 7: SPARE
3/2	Master Trip Assignment, Byte 2 Bit 0: SPARE Bit 1: SPARE Bit 2: SPARE Bit 3: SPARE Bit 4: SPARE Bit 5: SPARE Bit 6: SPARE Bit 7: SPARE
3/3	Master Trip Assignment, Byte 3 Bit 0: 67P (DPU2000 and DPU2000R) Bit 1: 67N (DPU2000 and DPU2000R) Bit 2: 46 Bit 3: SPARE Bit 4: SPARE Bit 5: SPARE Bit 6: SPARE Bit 7: SPARE
4/1	Master Trip Assignment, Byte 4 Bit 0: 50N-1 Bit 1: 50N-2 Bit 2: 50N-3 Bit 3: 51N Bit 4: 50P-1 Bit 5: 50P-2 Bit 6: 50P-3 Bit 7: 51P
4/2	Spare
4/3	Spare
5/1	Spare
5/2	Spare
5/3	Spare
6/1	Spare
6/2	Checksum, high byte
6/3	Checksum, low byte

8.8.4 Breaker Failure Settings (3 10 4)

NOTE: This command is NOT available in DPU1500R. DPU2000 series requires CPU version 1.70 and above.

Msg/Byte	Definition

1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xa4
3/1	Enable (1=ON, 0=OFF)
3/2	BFT Pickup Time Delay (high byte)
3/3	BFT Pickup Time Delay (low byte)
4/1	BFT Drop Time Delay
4/2	BFT Starters Bit 0: External input Bit 1: Phase Level Detector Bit 2: Neutral Level Detector
4/3	ReTrip Pickup Time Delay (high byte)
5/1	ReTrip Pickup Time Delay (low byte)
5/2	ReTrip Drop Time Delay
5/3	ReTrip Starters Bit 0: External input Bit 1: Phase Level Detector Bit 2: Neutral Level Detector
6/1	Phase Level Detector Pickup (5 to 100% of 51P)
6/2	Neutral Level Detector Pickup (5 to 100% of 51N)
6/3	Spare
7/1	Spare
7/2	Spare
7/3	Spare
8/1	Spare
8/2	Checksum, high byte
8/3	Checksum, low byte

8.9 Receive Edit Buffer "N" Commands (3 11 n)

N	Definition
0	Reserved for Repeat
1	Programmable Input Select and Index Tables
2	Programmable Input Negated AND Table
3	Programmable Input AND/OR Table
4	Programmable Input User Defined Input Names
5	Programmable Ouptut Select Table
6	Programmable Output AND/OR Table
7	Programmable Output User Defined Output Names
8	Primary Relay Settings
9	Alternate 1 Relay Settings
10	Alternate 2 Relay Settings
11	Configuration Settings
12	Counter Settings
13	Alarm Settings
14	Real Time Clock
15	Programmable Output Delays

8.9.1 Receive Programmable Input Select and Index (3 11 1)

Bit Position:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPU2000:	IN3	IN4	IN9	IN2	IN10	43A	52B	52A	IN1	IN11	IN8	IN7	IN6	IN5	IN13	IN12
DPU2000R:	IN3	IN4	FB1	IN2	FB2	FB3	FB4	FB5	IN1	FB6	IN8	IN7	IN6	IN5	FB7	FB8
DPU1500R:	IN3	IN4	N/A	IN2	N/A	N/A	N/A	N/A	IN1	N/A	IN6	N/A	N/A	IN5	N/A	N/A

Figure 14 – Physical Input Index

Bit = 0, Physical Input is selected.
Bit = 1, Physical Input is not selected.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.
Index byte is the offset into the DPU's logical input structure.

Logical Input List for DPU2000 – Requires matrix (29 x 16) to allow user to map 29 Logical Inputs to 13 Physical Inputs plus "43A", "52A", and "52B". Logical Inputs include: "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "UDI".

Logical Input List for DPU2000R – Requires matrix (29 x 16) to allow user to map 29 Logical Inputs to 8 Physical Inputs plus 8 Feedback Inputs. Logical Inputs include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "67P", "67N", "ULI1", "ULI2", "ULI3", "ULI4", "ULI5", "ULI6", "ULI7", "ULI8", "ULI9", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "EXTBF", "BFI", "UDI", "25"(*Synch Check Model*), "25By"(*Synch Check Model*). The following logical inputs are available in CPU versions greater than 1.92: "LOCAL", "TGT", "SIA", The following logical inputs are available in CPU version greater than 4.02 (2.01 for PTH): LIS1, LIS2, LIS3, LIS4, LIS5, LIS6, LIS7, LIS8, LIR1, LIR2, LIR3, LIR4, LIR5, LIR6, LIR7, LIR8, TR_SET, TR_RST.

Logical Input List for DPU1500R – Requires matrix (29 x 6) to allow user to map 29 Logical Inputs to 6 Physical Inputs. Logical Inputs include: "52A", "52B", "43A", "TCM", "GRD", "PH3", "50-1", "50-2", "50-3", "ALT1", "ALT2", "ZSC", "SCC", "79S", "79M", "OPEN", "CLOSE", "ECI1", "ECI2", "WCI", "46", "CRI", "ARCI", "TARC", "SEF" (*Sensitive Earth Model*), "UDI", "LOCAL", "TGT", "SIA".

Refer to Table 3 on page 313 for the complete listing of Logical Input Offsets and their respective definitions.

Msg byte	Definition
1/1	Most significant high byte of password

1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xb1
3/1	INPUT1 high byte
3/2	INPUT1 low byte
3/3	INPUT1 index byte
4/1	INPUT2 high byte
4/2	INPUT2 low byte
4/3	INPUT2 index byte
5/1	INPUT3 high byte
5/2	INPUT3 low byte
5/3	NPUT3 index byte
6/1	INPUT4 high byte
6/2	INPUT4 low byte
6/3	INPUT4 index byte
7/1	INPUT5 high byte
7/2	INPUT5 low byte
7/3	INPUT5 index byte
8/1	INPUT6 high byte
8/2	INPUT6 low byte
8/3	INPUT6 index byte
9/1	INPUT7 high byte
9/2	INPUT7 low byte
9/3	INPUT7 index byte
10/1	INPUT8 high byte
10/2	INPUT8 low byte
10/3	INPUT8 index byte
11/1	INPUT9 high byte
11/2	INPUT9 low byte
11/3	INPUT9 index byte
12/1	INPUT10 high byte
12/2	INPUT10 low byte
12/3	INPUT10 index byte
13/1	INPUT11 high byte
13/2	INPUT11 low byte
13/3	INPUT11 index byte
14/1	INPUT12 high byte
14/2	INPUT12 low byte
14/3	INPUT12 index byte
15/1	INPUT13 high byte
15/2	INPUT13 low byte
15/3	INPUT13 index byte
16/1	INPUT14 high byte
16/2	INPUT14 low byte
16/3	INPUT14 index byte
17/1	INPUT15 high byte
17/2	INPUT15 low byte
17/3	INPUT15 index byte
18/1	INPUT16 high byte
18/2	INPUT16 low byte
18/3	INPUT16 index byte
19/1	INPUT17 high byte
19/2	INPUT17 low byte
19/3	INPUT17 index byte
20/1	INPUT18 high byte
20/2	INPUT18 low byte
20/3	INPUT18 index byte

21/1	INPUT19 high byte
21/2	INPUT19 low byte
21/3	INPUT19 index byte
22/1	INPUT20 high byte
22/2	INPUT20 low byte
22/3	INPUT20 index byte
23/1	INPUT21 high byte
23/2	INPUT21 low byte
23/3	INPUT21 index byte
24/1	INPUT22 high byte
24/2	INPUT22 low byte
24/3	INPUT22 index byte
25/1	INPUT23 high byte
25/2	INPUT23 low byte
25/3	INPUT23 index byte
26/1	INPUT24 high byte
26/2	INPUT24 low byte
26/3	INPUT24 index byte
27/1	INPUT25 high byte
27/2	INPUT25 low byte
27/3	INPUT25 index byte
28/1	INPUT26 high byte
28/2	INPUT26 low byte
28/3	INPUT26 index byte
29/1	INPUT27 high byte
29/2	INPUT27 low byte
29/3	INPUT27 index byte
30/1	INPUT28 high byte
30/2	INPUT28 low byte
30/3	INPUT28 index byte
31/1	INPUT29 high byte
31/2	INPUT29 low byte
31/3	INPUT29 index byte
32/1	Spare
32/2	Checksum high byte
32/3	Checksum low byte

8.9.2 Receive Programmable Input Negated AND (3 11 2)

Bit = 0, Enabled when input is opened.
Bit = 1, Enabled when input is closed.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb2
3/1	INPUT1 high byte
3/2	INPUT1 low byte
3/3	INPUT2 high byte
4/1	INPUT2 low byte
4/2	INPUT3 high byte
4/3	INPUT3 low byte
5/1	INPUT4 high byte
5/2	INPUT4 low byte
5/3	INPUT5 high byte

6/1	INPUT5 low byte
6/2	INPUT6 high byte
6/3	INPUT6 low byte
7/1	INPUT7 high byte
7/2	INPUT7 low byte
7/3	INPUT8 high byte
8/1	INPUT8 low byte
8/2	INPUT9 high byte
8/3	INPUT9 low byte
9/1	INPUT10 high byte
9/2	INPUT10 low byte
9/3	INPUT11 high byte
10/1	INPUT11 low byte
10/2	INPUT12 high byte
10/3	INPUT12 low byte
11/1	INPUT13 high byte
11/2	INPUT13 low byte
11/3	INPUT14 high byte
12/1	INPUT14 low byte
12/2	INPUT15 high byte
12/3	INPUT15 low byte
13/1	INPUT16 high byte
13/2	INPUT16 low byte
13/3	INPUT17 high byte
14/1	INPUT17 low byte
14/2	INPUT18 high byte
14/3	INPUT18 low byte
15/1	INPUT19 high byte
15/2	INPUT19 low byte
15/3	INPUT20 high byte
16/1	INPUT20 low byte
16/2	INPUT21 high byte
16/3	INPUT21 low byte
17/1	INPUT22 high byte
17/2	INPUT22 low byte
17/3	INPUT23 high byte
18/1	INPUT23 low byte
18/2	INPUT24 high byte
18/3	INPUT24 low byte
19/1	INPUT25 high byte
19/2	INPUT25 low byte
19/3	INPUT26 high byte
20/1	INPUT26 low byte
20/2	INPUT27 high byte
20/3	INPUT27 low byte
21/1	INPUT28 high byte
21/2	INPUT28 low byte
21/3	INPUT29 high byte
22/1	INPUT29 low byte
22/2	Checksum high byte
22/3	Checksum low byte

8.9.3 Receive Programmable Input AND/OR Select (3 11 3)

Bit = 0, Selected inputs are Ored together.
Bit = 1, Selected inputs are ANDed together.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password

1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb3
3/1	Programmable input AND/OR selection bits 24-31
3/2	Programmable input AND/OR selection bits 16-23
3/3	Programmable input AND/OR selection bits 8-15
4/1	Programmable input AND/OR selection bits 0-7
4/2	Checksum high byte
4/3	Checksum low byte

Bit	Logical Input
50	INPUT1
50	INPUT2
	.
	.
	.
50	INPUT28
50	INPUT29
50	not used reserved for 52A
50	not used reserved for 52B
50	not used reserved for 43A

8.9.4 Receive Programmable Input User Defined Strings (3 11 4)

User definable 8 chars input strings. Byte 9 is an implied NULL

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb4
3/1-5/2	IN1 Character String 8 bytes
5/3-8/1	IN2 Character String 8 bytes
8/2-10/3	IN3 Character String 8 bytes
11/1-13/2	IN4 Character String 8 bytes
13/3-16/1	IN5 Character String 8 bytes
16/2-18/3	IN6 Character String 8 bytes
19/1-21/2	IN7 Character String 8 bytes (DPU2000/2000R)
21/3-24/1	IN8 Character String 8 bytes (DPU2000/2000R)
24/2-26/3	IN9 Character String 8 bytes (DPU2000)
27/1-29/2	IN10 Character String 8 bytes (DPU2000)
29/3-32/1	IN11 Character String 8 bytes (DPU2000)
32/2-34/3	IN12 Character String 8 bytes (DPU2000)
35/1-37/2	IN13 Character String 8 bytes (DPU2000)
37/3-38/1	spares
38/2	Checksum high byte
38/3	Checksum low byte

8.9.5 Receive Programmable Output Select (3 11 5)

NOTE: Feedback terms are available in DPU2000R, CPU version 1.60 and above.

Bit Position:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPU2000:	Trip	Close	Out6	Out4	Out5	Out3	Out2	Out1	Out7	Out8	N/A	N/A	N/A	N/A	N/A	N/A
DPU2000R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	FB1	FB2	FB3	FB4	FB5	FB6	FB7	FB8
DPU1500R:	Trip	N/A	Out6	Out4	Out5	Out3	Out2	Out1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Figure 15 – Physical Output Index

Programmable Output data transferred from PC to relay.

Bit = 0, Physical Output is selected.
Bit = 1, Physical Output is not selected.
Least significant low byte consists of bits 0 through 7.
Least significant high byte consists of bits 8 through 15.
Most significant low byte consists of bits 16 through 23.
Most significant high byte consists of bits 24 through 31.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb5
3/1	Contact OUT6 most significant high byte
3/2	Contact OUT6 most significant low byte
3/3	Contact OUT6 least significant high byte
4/1	Contact OUT6 least significant low byte
4/2	Contact OUT4 most significant high byte
4/3	Contact OUT4 most significant low byte
5/1	Contact OUT4 least significant high byte
5/2	Contact OUT4 least significant low byte
5/3	Contact OUT5 most significant high byte
6/1	Contact OUT5 most significant low byte
6/2	Contact OUT5 least significant high byte
6/3	Contact OUT5 least significant low byte
7/1	Contact OUT3 most significant high byte
7/2	Contact OUT3 most significant low byte
7/3	Contact OUT3 least significant high byte
8/1	Contact OUT3 least significant low byte
8/2	Contact OUT2 most significant high byte
8/3	Contact OUT2 most significant low byte
9/1	Contact OUT2 least significant high byte
9/2	Contact OUT2 least significant low byte
9/3	Contact OUT1 most significant high byte
10/1	Contact OUT1 most significant low byte
10/2	Contact OUT1 least significant high byte
10/3	Contact OUT1 least significant low byte
11/1	Contact OUT7 most significant high byte (DPU2000) DPU2000R FB1 most significant high byte
11/2	Contact OUT7 most significant low byte (DPU2000) DPU2000R FB1 most significant low byte
11/3	Contact OUT7 least significant high byte (DPU2000) DPU2000R FB1 least significant high byte
12/1	Contact OUT7 least significant low byte (DPU2000) DPU2000R FB1 least significant low byte
12/2	Contact OUT8 most significant high byte (DPU2000) DPU2000R FB2 most significant high byte
12/3	Contact OUT8 most significant low byte (DPU2000) DPU2000R FB2 most significant low byte
13/1	Contact OUT8 least significant high byte (DPU2000) DPU2000R FB2 least significant high byte
13/2	Contact OUT8 least significant low byte (DPU2000) DPU2000R FB2 least significant low byte
13/3	DPU2000R FB3 most significant high byte
14/1	DPU2000R FB3 most significant low byte
14/2	DPU2000R FB3 least significant high byte

14/3	DPU2000R FB3 least significant low byte
15/1	DPU2000R FB4 most significant high byte
15/2	DPU2000R FB4 most significant low byte
15/3	DPU2000R FB4 least significant high byte
16/1	DPU2000R FB4 least significant low byte
16/2	DPU2000R FB5 most significant high byte
16/3	DPU2000R FB5 most significant low byte
17/1	DPU2000R FB5 least significant high byte
17/2	DPU2000R FB5 least significant low byte
17/3	DPU2000R FB6 most significant high byte
18/1	DPU2000R FB6 most significant low byte
18/2	DPU2000R FB6 least significant high byte
18/3	DPU2000R FB6 least significant low byte
19/1	DPU2000R FB7 most significant high byte
19/2	DPU2000R FB7 most significant low byte
19/3	DPU2000R FB7 least significant high byte
20/1	DPU2000R FB7 least significant low byte
20/2	DPU2000R FB8 most significant high byte
20/3	DPU2000R FB8 most significant low byte
21/1	DPU2000R FB8 least significant high byte
21/2	DPU2000R FB8 least significant low byte
21/3	Spare
22/1	Spare
22/2	Checksum high byte
22/3	Checksum low byte

8.9.6 Receive Programmable Output AND/OR/Index (3 11 6)

Bit = 0, Selected outputs are Ored together.
Bit = 1, Selected outputs are ANDed together.
Index byte is the offset into the DPU's logical output structure.

Logical Output List for DPU2000 – Requires matrix (32 x 8) to allow user to map 32 Logical Outputs to 8 Physical Outputs. NOTE: first two logicals, ***TRIP*** and ***CLOSE*** are fixed (bits 0 and 1), user is not permitted to remove these from the list. Logical Outputs include: "TRIP", "CLOSE", "ALARM", "BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "67P", "67N", "81S-1", "81R-1", "81O-1", "27-1P", "59", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA", "50-1D", "LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "32PA", "32NA", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "59*", "67P*", "67N*", "81S-1*", "81R-1*", "81O-1*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "ULO1", "ULO2", "ULO3", "ULO4", "ULO5", "ULO6", "ULO7", "ULO8", "ULO9", "81O-2", "81S-2", "81R-2", "81O-2*", "81S-2*", "81R-2*", "CLTA", "Pwatt1", "Pwatt2", "79CA1*", "79CA2*", "BFA*".

Logical Output List for DPU2000R – Requires matrix (31 x 14) to allow user to map 31 Logical Outputs to 6 Physical Outputs plus 8 Feedback Outputs. NOTE: first logical, ***TRIP*** is fixed, user is not permitted to remove Trip logical from the list. Also note, since the ***CLOSE*** logical is specific to DPU2000, mapping of this logical (located at bit 1) is NOT permissible. Logical Outputs include: "TRIP", "CLOSE", "ALARM", "BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "67P", "67N", "81S-1", "81R-1", "81O-1", "27-1P", "59", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA", "50-1D", "LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "32PA", "32NA", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "59*", "67P*", "67N*", "81S-1*", "81R-1*", "81O-1*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "ULO1", "ULO2", "ULO3", "ULO4", "ULO5", "ULO6", "ULO7", "ULO8", "ULO9", "81O-2", "81S-2", "81R-2", "81O-2*", "81S-2*", "81R-2*", "CLTA", /* V1.40 */ "Pwatt1", "Pwatt2", "79CA1*", "79CA2*". The following were added to CPU V1.60: "SEF*"(*Sensitive Earth Model*), "SEF"(*Sensitive Earth Model*), "BZA", "BFT", "ReTrp", "BFT*", "ReTrp*". The following were added to CPU V1.80: "32P-2", "32N-2", "32P-2*", "32N-2*", "BFA*".

The following were added to CPU V1.93: "25*"(*Synch Check Model*), "25"(*Synch Check Model*), "SBA".

The following were added to CPU V3.20: "79V"and "Rclin","59G","59G*", "LO1", LO2", "LO3", "LO4", "LO5", "LO6", "LO7", "LO8", "TR_ON","TR_OFF","TR_TAG".

The following were added to CPU V5.0: 59-3P, 59-3P*, 47, 47*, 21P-1, 21P-1*, 21P-2, 21P-2*, 21P-3, 21P-3*, 21P-4, 21P-4*.

Logical Output List for DPU1500R – Requires matrix (31 x 6) to allow user to map 31 Logical Outputs to 6 Physical Outputs. NOTE: first logical, ***TRIP*** is fixed, user is not permitted to remove Trip logical from the list. Also note, since the ***CLOSE*** logical is specific to DPU2000, mapping of this logical (located at bit 1) is NOT permissible. Logical Outputs include: "TRIP", "CLOSE", "ALARM", "BFA", "TCFA", "79LOA", "TCC", "PUA", "51P", "51N", "46", "50P-1", "50N-1", "50P-2", "50N-2", "50P-3", "50N-3", "PATA", "PBTA", "PCTA", "27-1P", "79DA", "79CA1", "OCTC", "KSI", "PDA", "NDA", "PVArA", "NVArA", "LOADA", "50-1D","LPFA", "HPFA", "ZSC", "50-2D", "BFUA", "STCA", "PH3-D", "GRD-D", "27-3P", "VarDA", "79CA2", "TRIPA", "TRIPB", "TRIPC", "27-1P*", "46*", "50P-1*", "50N-1*", "50P-2*", "50N-2*", "50P-3*", "50N-3*", "51P*", "51N*", "27-3P*", "TRIPA*", "TRIPB*", "TRIPC*", "CLTA", "Pwatt1", "Pwatt2", "79CA1*", "79CA2*", "SEF*"(*Sensitive Earth Model*), "SEF"(*Sensitive Earth Model*), "BZA", "BFA*", "SBA", "79V" and "Rclin".

Refer to Table 5, on page 322, for a complete listing of Logical Output Offsets and their respective definitions.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb6
3/1	spare (bits 24-31)
3/2	spare (bits 16-23)
3/3	Programmable output AND/OR selection bits 8-15
4/1	Programmable output AND/OR selection bits 0-7
4/2	OUTPUT1 index byte
4/3	OUTPUT2 index byte
5/1	OUTPUT3 index byte
5/2	OUTPUT4 index byte
5/3	OUTPUT5 index byte
6/1	OUTPUT6 index byte
6/2	OUTPUT7 index byte
6/3	OUTPUT8 index byte
7/1	OUTPUT9 index byte
7/2	OUTPUT10 index byte
7/3	OUTPUT11 index byte
8/1	OUTPUT12 index byte
8/2	OUTPUT13 index byte
8/3	OUTPUT14 index byte
9/1	OUTPUT15 index byte
9/2	OUTPUT16 index byte
9/3	OUTPUT17 index byte
10/1	OUTPUT18 index byte
10/2	OUTPUT19 index byte
10/3	OUTPUT20 index byte
11/1	OUTPUT21 index byte
11/2	OUTPUT22 index byte
11/3	OUTPUT23 index byte
12/1	OUTPUT24 index byte
12/2	OUTPUT25 index byte
12/3	OUTPUT26 index byte
13/1	OUTPUT27 index byte
13/2	OUTPUT28 index byte
13/3	OUTPUT29 index byte
14/1	OUTPUT30 index byte
14/2	Checksum high byte
14/3	Checksum low byte

Bit	Logical Output
50	TRIP
50	CLOSE (This bit available for mapping in DPU2000 only)
50	OUTPUT1
50	OUTPUT2
.	
.	
.	
50	OUTPUT29
50	OUTPUT30

8.9.7 Receive Programmable Output User Defined Names (3 11 7)

User definable 8 char output strings. Byte 9 is an implied NULL.

Msg byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xb7
3/1-5/2	OUT1 Character String 8 bytes
5/3-8/1	OUT2 Character String 8 bytes
8/2-10/3	OUT3 Character String 8 bytes
11/1-13/2	OUT4 Character String 8 bytes
13/3-16/1	OUT5 Character String 8 bytes
16/2-18/3	OUT6 Character String 8 bytes
19/1-21/2	OUT7 Character String 8 bytes (DPU2000)
21/3-24/1	OUT8 Character String 8 bytes (DPU2000)
24/2-26/3	Spare Character String 8 bytes
27/1-29/2	Spare Character String 8 bytes
29/3-32/1	Spare Character String 8 bytes
32/2-34/3	Spare Character String 8 bytes
35/1-37/2	Spare Character String 8 bytes
37/3-40/1	Spare Character String 8 bytes
40/2	Checksum high byte
40/3	Checksum low byte

8.9.8 Receive Relay Settings (3 11 x)

(3 11 8) = Primary Settings
(3 11 9) = Alternate 1 Settings
(3 11 10) = Alternate 2 Settings
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

The following functions are available in the DPU1500R: 51P, 50P-1, 50P-2, 50P-3, 46, 51N, 50N-1, 50N-2, 50N-3, 79 and 27.

8.9.8.1 Standard ANSI Curves for DPU2000 and DPU2000R

Refer to Table 6 (p. 326), Table 7 (p. 326), and Table 8 (p. 326) for the Curve Select assignments.

8.9.8.2 Recloser Curves for DPU2000 and DPU2000R

NOTE: Catalog Numbers XXXXXXXX-XX2XX and XXXXXXXX-XX3XX use the following curve types for 51P, 50P-1, 51N, and 50N-1 functions. Also, in addition to the Time Dial fields, include 51P, 50P-1, 51N and 50N-1 Minimum Response fields.

Refer to Table 9 (p. 327), Table 10 (p. 327), Table 11 (p. 327), and Table 12 (p. 328) for the Curve Select assignments.

8.9.8.3 IEC Curves for DPU2000R

NOTE: The following curves are available in IEC DPU2000R, Catalog Number 687XXXXX-XXXXX. All IEC type curves except Definite Time Curves, use Time Multipliers in place of Time Dials.

Refer to Table 13 (p. 328), Table 14 (p. 328), and Table 15 (p. 328) for the Curve Select assignments.

8.9.8.4 ANSI/IEC Curves for DPU1500R

NOTE: All IEC type curves, use Time Multipliers in place of Time Dials.

Refer to Table 16 (p. 329), Table 17 (p. 329), and Table 18 (p. 329) for the Curve Select assignments.

8.9.8.5 79-X Select Bit Pattern for DPU2000/2000R/1500R

Refer to Table 19 (p. 330) for the 79 lockout and enable/disable bit pattern assignments.

Msg byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = (Prim=0xb8, Alt1=0xb9, Alt2=0xba)
3/1	51P Curve Select byte (Type I or Recloser)
3/2	51P Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
3/3	51P Time dial (0.05-1*200)/delay byte(0-10 *20)
	IEC Curve –51P Time Multiplier (.05-1.00 *200)
4/1	50P-1 Curve Select byte (Type III or Recloser)
4/2	50P-1 Pickup X byte (0.5-20 *10)
4/3	50P-1 Timedial (1-10*10)/delay (0-9.99*100)high byte
	IEC Curve –50P-1 Time Multiplier (.05-1.00 *200)
5/1	50P-1 Timedial/delay low byte
5/2	50P-2 Select byte (0=Disable, 1=Enable)
5/3	50P-2 Pickup X byte (0.5-20 *10)
6/1	50P-2 Timedelay high byte (0-9.99 *100)
6/2	50P-2 Timedelay low byte
6/3	50P-3 Select byte (0=Disable, 1=Enable)
7/1	50P-3 Pickup X byte (0.5-20 *10)
7/2	46 Curve Select byte (Type II)
7/3	46 Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
8/1	46 Time dial(1-10 *20)/delay byte(0-10 * 20)
	IEC Curve –46 Time Multiplier (.05-1.00 *200)
8/2	51N Curve Select byte (Type II or Recloser)
8/3	51N Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
9/1	51N Time dial(1-10 *20)/delay byte(0-10 * 20)
	IEC Curve –51N Time Multiplier (.05-1.00 *200)
9/2	50N-1 Curve Select byte (Type III or Recloser)
9/3	50N-1 Pickup X byte (0.5-20 *10)
10/1	50N-1 Timedial(1-10*10)/delay(0-9.99*100)high byte
10/2	50N-1 Timedial/delay low byte
10/3	50N-2 Select byte (0=Disable, 1=Enable)
	Sensitive Earth Model (0=Disable, 1=Standard, 2=SEF, 3=Directional SEF)
11/1	50N-2 Pickup X byte (0.5-20 *10)
11/2	50N-2 Timedelay high byte (0-9.99 *100)
	SEF or Directional SEF Selects – 50N-2 Time Delay (0.5 to 180.0)*200
11/3	50N-2 Timedelay low byte
12/1	50N-3 Select byte (0=Disable, 1=Enable)
12/2	50N-3 Pickup X byte (0.5-20 *10)

12/3 79 Reset Time byte (3-200)
13/1 79-1 Select high byte (Lockout Type)
13/2 79-1 Select low byte (Enable Type)
13/3 79-1 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
14/1 79-1 Open Interval Time low byte
14/2 79-2 Select high byte (Lockout Type)
14/3 79-2 Select low byte (Enable Type)
15/1 79-2 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
15/2 79-2 Open Interval Time low byte
15/3 79-3 Select high byte (Lockout)
16/1 79-3 Select low byte (Enable)
16/2 79-3 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
16/3 79-3 Open Interval Time low byte
17/1 79-4 Select high byte (Lockout Type)
17/2 79-4 Select low byte (Enable Type)
17/3 79-4 Open Interval Time high byte (0.1 – 200 *10, 2001 = Lockout)
Sensitive Earth Model (0.1 to 1800 *10, 18001=Lockout)
18/1 79-4 Open Interval Time low byte
18/2 79-5 Select high byte (Lockout Type)
18/3 79-5 Select low byte (Enable Type)
19/1 79-5 Open Interval Time high byte (always lockout)
19/2 79-5 Open Interval Time low byte
19/3 79 Cutout Time byte (1 –201) (201 = Disable)
20/1 Cold Load Time byte (1 –254) (255 = Disable)
20/2 2 Phase Voting byte (0=Disable, 1=Enable)
20/3 67P Select byte (0=Disable, 1=Enable, 2=Lockout)
21/1 67P Curve Select byte (Type I)
21/2 67P Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
21/3 67P Time dial(1-10 *20)/delay(0-10 * 20) byte
IEC Curve –67P Time Multiplier (.05-1.00 *200)
22/1 67P Torque Angle byte (0-355 /5)
22/2 67N Select byte (0=Disable, 1=Enable, 2=Lockout)
Sensitive Earth Model (0=Disable, 1=Enable-Neg Sequence, 2=Lockout-Neg Sequence, 5=Enable-Pos Sequence, 6=Lockout Pos Sequence)
22/3 67N Curve Select byte (Type I)
23/1 67N Pickup Amps byte (1-12Amp *10, 0.2-2.4Amp *50)
23/2 67N Time dial(1-10 *20)/delay(0-10 * 20) byte
IEC Curve –67N Time Multiplier (.05-1.00 *200)
23/3 67N Torque Angle byte (0-355 /5)
24/1 81 Select byte (0=Disable,1=81-1,2=81-2,3=Special)
24/2 81s-1 Pickup Frequency high byte
(60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
24/3 81s-1 Pickup Frequency low byte
25/1 81s-1 Timedelay high byte (0.08-9.98 *100)
25/2 81s-1 Timedelay low byte
25/3 81r-1 Pickup Frequency high byte
(60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
26/1 81r-1 Pickup Frequency low byte
26/2 81r-1 Timedelay high byte (0-999)
26/3 81r-1 Timedelay low byte
27/1 81v Voltage Block high byte (40-200)
27/2 81v Voltage Block low byte
27/3 27 Select byte (0=Disable, 1=Enable)
28/1 27 Pickup Voltage high byte (10-200)
28/2 27 Pickup Voltage low byte
28/3 27 Timedelay byte (0-60)

29/1	79v Select byte (0=Disable, 1=Enable)
29/2	79v Pickup Voltage high byte (10-200)
29/3	79v Pickup Voltage low byte
30/1	79v Timedelay byte (4-200)
30/2	59 Select byte (0=Disable, 1=Enable)
30/3	59 Pickup Voltage high byte (70-250)
31/1	59 Pickup Voltage low byte
31/2	59 Timedelay byte (0-60)
31/3	51 P Minimum Response (0 – 60 cycles)
32/1	51 N Minimum Respons (0 – 60 cycles)
32/2	50 P-1 Minimum Response (0 – 60 cycles)
32/3	50 N-1 Minimum Response (0 – 60 cycles)
33/1	Unit Configuration byte(for transmit only)
33/2	81s-2 Pickup Frequency high byte (60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
33/3	81s-2 Pickup Frequency low byte
34/1	81s-2 Timedelay high byte (0.08-9.98 *100)
34/2	81s-2 Timedelay low byte
34/3	81r-2 Pickup Frequency high byte (60hz: 56-64 *100, 6401=Disable 50hz: 46-54 *100, 5401=Disable)
35/1	81r-2 Pickup Frequency low byte
35/2	81r-2 Timedelay high byte (0-999)
35/3	81r-2 Timedelay low byte
36/1	Sensitive Earth Model – SEF Torque Angle (0-355 /5)
36/2	Sensitive Earth Model – SEF 50N-2 Pickup mA high byte (10-400)/2
36/3	Sensitive Earth Model – SEF 50N-2 Pickup mA low byte
37/1	Sensitive Erth Model neutral cold load time(1-254)(255= disable)
37/2	Checksum high byte
37/3	Checksum low byte

8.9.9 Receive Configuration Settings (3 11 11)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xbb
3/1	Phase CT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R/1500R)
3/2	Phase CT Ratio low byte
3/3	Neutral CT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R)
4/1	Neutral CT Ratio low byte
4/2	VT Ratio high byte (1-999 DPU2000, 1-2000 DPU2000R/1500R)
5/1	VT Connection high byte
5/2	VT Connection low byte (0=69V Wye, 1=120V Wye, 2=120V Delta, 3=208V Delta, 4=69V Wye 3V0 I, 5=120V Wye 3V0 I)
5/3	Positive Sequence Reactance high byte (1-4 *1000)
6/1	Positive Sequence Reactance low byte
6/2	Positive Sequence Resistance high byte (1-4 *1000)
6/3	Positive Sequence Resistance low byte
7/1	Zero Sequence Reactance high byte (1-4 *1000)
7/2	Zero Sequence Reactance low byte
7/3	Zero Sequence Resistance high byte (1-4 *1000)
8/1	Zero Sequence Resistance low byte
8/2	Distance in Miles high byte (0.1-50 *10)
8/3	Distance in Miles low byte

9/1	Trip Failure Time high byte(5-60)
9/2	Trip Failure Time low byte
9/3	Close Failure Time high byte(18-999)
10/1	Close Failure Time low byte
10/2	Phase Rotation high byte (0=ABC, 1=ACB)
10/3	Phase Rotation low byte
11/1	Configuration Flag high byte
11/2	Configuration Flag low byte bit 0: Protection Mode (0=Fund, 1=RMS) bit 1: Reset Mode (0=Instant, 1=Delayed) bit 2: Zone Sequence (0=Disabled, 1=Enabled) bit 3: Target Display Mode (0=Last, 1=All) bit 4: Local Edit (0=Disabled, 1=Enabled) bit 5: Reserved (Remote Edit, 0=Disabled, 1=Enabled) bit 6: WHr/VarHr Mtr Mode (0=KWHr, 1=MWHr) bit 7: LCD Light (0=Timer, 1=On) bit 8: Multi Device Trip (0=Disabled, 1=Enabled) bit 9: VCN Special Mode (0=Normal, 1=Inverted) bit10: Cold Load Timer Mode(0=Seconds, 1=Minutes) bit11: Reserved bit 12: 79V Timer Mode (0= sec., 1=min.) bit 13: Voltage Display Mode (0= vln, 1=Vll) bit 14: Reserved
11/3	ALT 1 Setting Enable high byte(0=Disable,1=Enable)
12/1	ALT 1 Setting Enable low byte
12/2	ALT 2 Setting Enable high byte(0=Disable,1=Enable)
12/3	ALT 2 Setting Enable low byte
13/1	Demand Time Constant high byte
13/2	Demand Time Constant low byte (0=5 min, 1=15 min, 2=30 min, 3=60 min)
13/3	Sensitive Earth CT Ratio high byte (1-2000)
14/1	Sensitive Earth CT Ratio low byte
14/2-19/1	Unit Name character 1-15
19/2	OCI configuration byte (0 = disable, 1 = enable) Bit 0: OCI Control Button Bit 1: Breaker Control Button Bits 2 – 7: reserved for future use
19/3	Sensitive Earth V0 PT Ratio high byte (1-2000)
20/1	Sensitive Earth V0 PT Ratio low byte
20/2	Spare
20/3	Spare
21/1	LCD Contrast Adjustment high byte(0-63)
21/2	LCD Contrast Adjustment low byte
21/3	Relay Password character 1
22/1	Relay Password character 2
22/2	Relay Password character 3
22/3	Relay Password character 4
23/1	Test Password character 1
23/2	Test Password character 2
23/3	Test Password character 3
24/1	Test Password character 4
24/2	Checksum high byte
24/3	Checksum low byte

8.9.10 Receive Counter Settings (3 11 12)

NOTE: This command is used in versions prior to CPU V1.41.
Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition

1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xbc
3/1	KSI Sum A Counter high byte
3/2	KSI Sum A Counter low byte
3/3	KSI Sum B Counter high byte
4/1	KSI Sum B Counter low byte
4/2	KSI Sum C Counter high byte
4/3	KSI Sum C Counter low byte
5/1	Over Current Trip Counter high byte
5/2	Over Current Trip Counter low byte
5/3	Breaker Operations Counter high byte
6/1	Breaker Operations Counter low byte
6/2	Reclose Counter 1 high byte
6/3	Reclose Counter 1 low byte
7/1	1st Reclose Counter high byte
7/2	1st Reclose Counter low byte
7/3	2nd Reclose Counter high byte
8/1	2nd Reclose Counter low byte
8/2	3rd Reclose Counter high byte
8/3	3rd Reclose Counter low byte
9/1	4th Reclose Counter high byte
9/2	4th Reclose Counter low byte
9/3	Reclose Counter 2 high byte
10/1	Reclose Counter 2 low byte
10/2	Checksum high byte
10/3	Checksum low byte

8.9.11 Receive Alarm Settings (3 11 13)

Low byte consists of bits 0 through 7.
High byte consists of bits 8 through 15.

Msg byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xbd
3/1	KSI Summation Alarm Threshold high byte (1-9999,10000=Disables)
3/2	KSI Summation Alarm Threshold low byte
3/2	Overcurrent Trip Counter Alarm Threshold high byte (1-9999,10000=Disables)
4/1	Overcurrent Trip Counter Alarm Threshold low byte
4/2	Reclosure Counter 1 Alarm Threshold high byte (1-9999,10000=Disables)
4/3	Reclosure Counter 1 Alarm Threshold low byte
5/1	Phase Demand Alarm high byte (1-9999,10000=Disables)
5/2	Phase Demand Alarm low byte
5/3	Neutral Demand Alarm high byte (1-9999,10000=Disables)
6/1	Neutral Demand Alarm low byte
6/2	Low PF Alarm high byte (0.5-1.0 *100, 101=Disables)
6/3	Low PF Alarm low byte
7/1	High PF Alarm high byte (0.5-1.0 *100, 101=Disables)
7/2	High Pf Alarm low byte
7/3	Reclosure Counter 2 Alarm Threshold high byte (1-9999,10000=Disables)
8/1	Reclosure Counter 2 Alarm Threshold low byte
8/2	3 Phase kVAR Alarm Threshold high byte (10-99990 /10,10000=Disables)

8/3	3 Phase kVAR Alarm Threshold low byte
9/1	Load Current Alarm high byte (1-9999,10000=Disables)
9/2	Load Current Alarm low byte
9/3	Positive kVAR Alarm high byte (10-99990 /10,10000=Disable)
10/1	Positive kVAR Alarm low byte
10/2	Negative kVAR Alarm high byte (10-99990 /10,10000=Disable)
10/3	Negative kVAR Alarm high byte
11/1	Pos Watt Alarm 1 high byte (1-9999, 10000=Disable)
11/2	Pos Watt Alarm 1 low byte
11/3	Pos Watt Alarm 2 high byte (1-9999, 10000=Disable)
12/1	Pos Watt Alarm 2 low byte
12/2	Spare
12/3	Spare
13/1	Spare
13/2	Spare
13/3	Spare
14/1	Spare
14/2	Checksum high byte
14/3	Checksum low byte

NOTE: Positive Watt Alarm 1 and Positive Watt Alarm 2 units are displayed in either KWhr or MWhr according to bit 6 of Configuration Flag (Command 3 4 11, message 10/2). If bit is set to one, use MWhr, if bit is zero, use KWhr.

8.9.12 Receive Real Time Clock (3 11 14)

Msg byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	spare
2/3	Command + Subcommand = 0xbe
3/1	Hours byte (0-23)
3/2	Minutes byte (0-59)
3/3	Seconds byte (0-59)
4/1	Day byte (0-31) (0= Clock Shutdown)
4/2	Month byte (1-12)
4/3	Year byte (0-99)
5/1	spare
5/2	Checksum high byte
5/3	Checksum low byte

8.9.13 Receive Programmable Output Delays (3 11 15)

Msg Byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xbf
3/1	OUT 6 delay high byte
3/2	OUT 6 delay low byte
3/3	OUT 4 delay high byte
4/1	OUT 4 delay low byte
4/2	OUT 5 delay high byte
4/3	OUT 5 delay low byte
5/1	OUT 3 delay high byte
5/2	OUT 3 delay low byte
5/3	OUT 2 delay high byte
6/1	OUT 2 delay low byte

6/2	OUT 1 delay high byte
6/3	OUT 1 delay low byte
7/1	OUT 7 delay high byte (DPU2000)
7/2	OUT 7 delay low byte
7/3	OUT 8 delay high byte (DPU2000)
8/1	OUT 8 delay low byte
8/2	Spare
8/3	Spare
9/1	Spare
9/2	Checksum high byte
9/3	Checksum low byte

8.10 Programmable Curve Commands (3 13 n)

n	Definition
0	Repeat Last Command
1	Receive Curve Parameters
2	Receive First Curve Data Set
3	Receive Next Curve Data Set
4	Receive Curve Pointer Table
5	Show Curve Parameters
6	Show Curve Data Set
7	Show Curve Pointer Table

8.10.1 Receive Curve Parameters (3 13 1)

For the unit to receive the curve data the following sequence of commands must be issued:

3 13 1 (Curve parameters)
3 13 2 (8 Alpha-Beta segments) block 0
3 13 3 (8 Alpha-Beta segments) block 1
3 13 3 (8 Alpha-Beta segments) block 2
3 13 3 (8 Alpha-Beta segments) block 3
3 13 3 (8 Alpha-Beta segments) block 4
3 13 3 (8 Alpha-Beta segments) block 5
3 13 3 (8 Alpha-Beta segments) block 6
3 13 4 (60 pointer offsets)

Data Byte	Definition
1/1	Most significant high byte of password
½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xd1
3/1	Programmable curve number
3/2	Coefficient A (high byte)
3/3	Coefficient A |
4/1	Coefficient A |
4/2	Coefficient A (low byte)
4/3	Coefficient B (high byte)
5/1	Coefficient B |
5/2	Coefficient B |
5/3	Coefficient B (low byte)
6/1	Coefficient C (high byte)
6/2	Coefficient C |
6/3	Coefficient C |
7/1	Coefficient C (low byte)
7/2	Coefficient P (high byte)
7/3	Coefficient P |
8/1	Coefficient P |
8/2	Coefficient P (low byte)
8/3	Spare
9/1	Spare
9/2	Checksum (high byte)
9/3	Checksum (low byte)

8.10.2 Receive First Curve Data Set (3 13 2)

Data Byte	Definition
1/1	Most significant high byte of password

½	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xd2
3/1	Programmable curve number
3/2	Segment 0: Endrange (high byte)
3/3	Segment 0: Endrange (low byte)
4/1	Segment 0: Alpha (high byte)
4/2	Segment 0: Alpha |
4/3	Segment 0: Alpha |
5/1	Segment 0: Alpha (low byte)
5/2	Segment 0: Beta (high byte)
5/3	Segment 0: Beta |
6/1	Segment 0: Beta |
6/2	Segment 0: Beta (low byte)
6/3-9/3	Segment 1 (same as segment 0)
10/1-13/1	Segment 2 (same as segment 0)
13/2-16/2	Segment 3 (same as segment 0)
16/3-19/3	Segment 4 (same as segment 0)
20/1-23/1	Segment 5 (same as segment 0)
23/2-26/2	Segment 6 (same as segment 0)
26/3-29/3	Segment 7 (same as segment 0)
30/1	Spare
30/2	Checksum (high byte)
30/3	Checksum (low byte)

8.10.3 Receive Next Curve Data Set (3 13 3)

Same format as (3 13 2).

8.10.4 Receive Curve Pointer Table (3 13 4)

Data Byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xd4
3/1	Programmable curve number
3/2	Pointer offset 0
3/3	Pointer offset 1
4/1	Pointer offset 2
4/2	Pointer offset 3
4/3	Pointer offset 4
5/1	Pointer offset 5
5/2	Pointer offset 6
5/3	Pointer offset 7
6/1	Pointer offset 8
6/2	Pointer offset 9
6/3	Pointer offset 10
7/1	Pointer offset 11
7/2	Pointer offset 12
7/3	Pointer offset 13
8/1	Pointer offset 14
8/2	Pointer offset 15
8/3	Pointer offset 16
9/1	Pointer offset 17
9/2	Pointer offset 18

9/3	Pointer offset 19
10/1	Pointer offset 20
10/2	Pointer offset 21
10/3	Pointer offset 22
11/1	Pointer offset 23
11/2	Pointer offset 24
11/3	Pointer offset 25
12/1	Pointer offset 26
12/2	Pointer offset 27
12/3	Pointer offset 28
13/1	Pointer offset 29
13/2	Pointer offset 30
13/3	Pointer offset 31
14/1	Pointer offset 32
14/2	Pointer offset 33
14/3	Pointer offset 34
15/1	Pointer offset 35
15/2	Pointer offset 36
15/3	Pointer offset 37
16/1	Pointer offset 38
16/2	Pointer offset 39
16/3	Pointer offset 40
17/1	Pointer offset 41
17/2	Pointer offset 42
17/3	Pointer offset 43
18/1	Pointer offset 44
18/2	Pointer offset 45
18/3	Pointer offset 46
19/1	Pointer offset 47
19/2	Pointer offset 48
19/3	Pointer offset 49
20/1	Pointer offset 50
20/2	Pointer offset 51
20/3	Pointer offset 52
21/1	Pointer offset 53
21/2	Pointer offset 54
21/3	Pointer offset 55
22/1	Pointer offset 56
22/2	Pointer offset 57
22/3	Pointer offset 58
23/1	Pointer offset 59
23/2	Spare
23/3	Spare
24/1	Spare
24/2	Spare
24/3	Spare
25/1	Spare
25/2	Spare
25/3	Spare
26/1	Spare
26/2	Checksum (high byte)
26/3	Checksum (low byte)

8.10.5 Send Curve Parameters (3 13 5)

For the unit to receive the curve data the following sequence of commands must be issued:

3 13 5 (Curve parameters)
3 13 6 (8 Alpha-Beta segments) block 0
3 13 6 (8 Alpha-Beta segments) block 1

3 13 6 (8 Alpha-Beta segments) block 2
3 13 6 (8 Alpha-Beta segments) block 3
3 13 6 (8 Alpha-Beta segments) block 4
3 13 6 (8 Alpha-Beta segments) block 5
3 13 6 (8 Alpha-Beta segments) block 6
3 13 7 (60 pointer offsets)

Data Byte	Definition
1/1	Curve Number
1/2	Curve Number
1/3	Curve Number

Msg Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0xd5
1/3	Total Number of Messages = 8
2/1	Coefficient A (high byte)
2/2	Coefficient A |
2/3	Coefficient A |
3/1	Coefficient A (low byte)
3/2	Coefficient B (high byte)
3/3	Coefficient B |
4/1	Coefficient B |
4/2	Coefficient B (low byte)
4/3	Coefficient C (high byte)
5/1	Coefficient C |
5/2	Coefficient C |
5/3	Coefficient C (low byte)
6/1	Coefficient P (high byte)
6/2	Coefficient P |
6/3	Coefficient P |
7/1	Coefficient P (low byte)
7/2	Spare
7/3	Spare
8/1	Spare
8/2	Checksum (high byte)
8/3	Checksum (low byte)

8.10.6 Send Curve Data Set (3 13 6)

Data Byte	Definition
1/1	Programmable curve number
½	Block number
1/3	Programmable curve number + Block number

Msg Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
½	Command + Subcommand = 0xd6
1/3	Total Number of Messages = 29
2/1	Programmable curve number
2/2	Block number
2/3	Segment 0: Endrange (high byte)
3/1	Segment 0: Endrange (low byte)
3/2	Segment 0: Alpha (high byte)
3/3	Segment 0: Alpha |
4/1	Segment 0: Alpha |
4/2	Segment 0: Alpha (low byte)
4/3	Segment 0: Beta (high byte)
5/1	Segment 0: Beta |
5/2	Segment 0: Beta |

5/3	Segment 0: Beta (low byte)
6/1-9/1	Segment 1 (same as segment 0)
9/2-12/2	Segment 2 (same as segment 0)
12/3-15/3	Segment 3 (same as segment 0)
16/1-19/1	Segment 4 (same as segment 0)
19/2-22/2	Segment 5 (same as segment 0)
22/3-25/3	Segment 6 (same as segment 0)
26/1-29/1	Segment 7 (same as segment 0)
29/2	Checksum (high byte)
29/3	Checksum (low byte)

8.10.7 Send Curve Pointer Table (3 13 7)

Data Byte	Definition
1/1	Programmable curve number
½	Programmable curve number
1/3	Programmable curve number

Msg Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
½	Command + Subcommand = 0xd7
1/3	Total Number of Messages = 25
2/1	Programmable curve number
2/2	Pointer offset 0
2/3	Pointer offset 1
3/1	Pointer offset 2
3/2	Pointer offset 3
3/3	Pointer offset 4
4/1	Pointer offset 5
4/2	Pointer offset 6
4/3	Pointer offset 7
5/1	Pointer offset 8
5/2	Pointer offset 9
5/3	Pointer offset 10
6/1	Pointer offset 11
6/2	Pointer offset 12
6/3	Pointer offset 13
7/1	Pointer offset 14
7/2	Pointer offset 15
7/3	Pointer offset 16
8/1	Pointer offset 17
8/2	Pointer offset 18
8/3	Pointer offset 19
9/1	Pointer offset 20
9/2	Pointer offset 21
9/3	Pointer offset 22
10/1	Pointer offset 23
10/2	Pointer offset 24
10/3	Pointer offset 25
11/1	Pointer offset 26
11/2	Pointer offset 27
11/3	Pointer offset 28
12/1	Pointer offset 29
12/2	Pointer offset 30
12/3	Pointer offset 31
13/1	Pointer offset 32
13/2	Pointer offset 33
13/3	Pointer offset 34
14/1	Pointer offset 35
14/2	Pointer offset 36

14/3	Pointer offset 37
15/1	Pointer offset 38
15/2	Pointer offset 39
15/3	Pointer offset 40
16/1	Pointer offset 41
16/2	Pointer offset 42
16/3	Pointer offset 43
17/1	Pointer offset 44
17/2	Pointer offset 45
17/3	Pointer offset 46
18/1	Pointer offset 47
18/2	Pointer offset 48
18/3	Pointer offset 49
19/1	Pointer offset 50
19/2	Pointer offset 51
19/3	Pointer offset 52
20/1	Pointer offset 53
20/2	Pointer offset 54
20/3	Pointer offset 55
21/1	Pointer offset 56
21/2	Pointer offset 57
21/3	Pointer offset 58
22/1	Pointer offset 59
22/2	Spare
22/3	Spare
23/2	Spare
23/3	Spare
23/2	Spare
24/3	Spare
24/2	Spare
24/3	Spare
25/1	Spare
25/2	Checksum (high byte)
25/3	Checksum (low byte)

8.11 Waveform Capture Commands (3 14 n)

The waveform capture feature was replaced by the digital fault recorder (DFR) feature in V5.20 DPU2000R. There for the 3 14 n commands are not supported in V5.20 DPU2000R and later versions. Refer to the extended Modbus register set (i.e. INCOM commands 3-1-2, 3-1-3, and 3-1-6) for the digital fault recorder feature.

N	Definition
0	Define waveform capture settings
1	Show waveform capture settings
2	Start waveform data accumulation
3	Stop waveform data accumulation
4	Report waveform record data headers
5	Fetch first block of a record
6	Fetch next block of a record
7	Retransmit last block of a record
8	Fetch Acquistion Status

8.11.1 Define Waveform Capture Settings (3 14 0)

Note the trigger sources are logically OR'ed together.

Example: if 3/1 is Hex 07; trigger on 50N-1 or 50N-2 or 50N-3 pickup. The capture is 8 cycles of waveform with 32 samples per cycle. We then have 7 inputs each of 8 cycles capture. The inputs are Ia, Ib, Ic, In, VA, Vb, and Vc . The data is sent from thr DPU in quarter cyle records, that is 32/4 samples per analog variable.

Data Byte	Definition
1/1	Most significant high byte of password
1/2	Most significant low byte of password
1/3	Least significant high byte of password
2/1	Least significant low byte of password
2/2	Spare
2/3	Command + Subcommand = 0xe0
3/1	Trigger source (byte 1) Bit 0: 50N-1 Bit 1: 50N-2 Bit 2: 50N-3 Bit 3: 51N Bit 4: 50P-1 Bit 5: 50P-2 Bit 6: 50P-3 Bit 7: 51P
3/2	Trigger source (byte 2) Bit 0: 67P (DPU2000 and DPU2000R) Bit 1: 67N (DPU2000 and DPU2000R) Bit 2: 46 Bit 3: 27 Bit 4: 59 (DPU2000 and DPU2000R) Bit 5: 79 Bit 6: 81S (DPU2000 and DPU2000R) Bit 7: 81R (DPU2000 and DPU2000R)
3/3	Trigger source :reserved (byte 3) Bit 0: Trip issued signal Bit 1: Breaker open Bit 2: External (WCI) Bit 5: 59G Bit 6 : 32P (DPU2000 and DPU2000R) Bit 7 : 32N (DPU2000 and DPU2000R)
4/1	Trigger source:reserved (byte 4)
4/2	Trigger position(qtr cycle): 0 to 255 (for 64 qtr cycle record)

0 to 128 (for 32 qtr cycle records)
0 to 64 (for 16 qtr cycle records)
0 to 32 (for 8 qtr cycle records)

4/3 Mode/Record Size
bit 0,1: 00 = 8 rec of 8 qtr cycle record
01 = 4 rec of 16 qtr cycle records
Table 3 = 2 rec of 32 qtr cycle records
11 = 1 rec of 64 qtr cycle records
bit 6 : Single Shot Mode (0=off, 1=on)
bit 7 : Append Record Mode (0=off, 1=on)

5/1 Spare
5/2 Checksum (high byte)
5/3 Checksum (low byte)

8.11.2 Report Waveform Capture Settings (3 14 1)

Data Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0xe1
1/3	Total Number of Messages = 9
2/1 – 6/3	Unit ID Name (15 characters)
7/1	Trigger source (byte 1) Bit 0: 50N-1 Bit 1: 50N-2 Bit 2: 50N-3 Bit 3: 51N Bit 4: 50P-1 Bit 5: 50P-2 Bit 6: 50P-3 Bit 7: 51P
7/2	Trigger source (byte 2) Bit 0: 67P (DPU2000 and DPU2000R) Bit 1: 67N (DPU2000 and DPU2000R) Bit 2: 46 Bit 3: 27 Bit 4: 59 (DPU2000 and DPU2000R) Bit 5: 79 Bit 6: 81S (DPU2000 and DPU2000R) Bit 7: 81R (DPU2000 and DPU2000R)
7/3	Trigger source (byte 3) Bit 0: Trip issued signal Bit 1: Breaker open Bit 2: External (WCI) Bit 5: 59G Bit 6 : 32P (DPU2000 and DPU2000R) Bit 7 : 32N (DPU2000 and DPU2000R)
8/1	Trigger source (byte 4)
8/2	Trigger position
8/3	Mode/Record Size bit 0,1: 00 = 8 rec of 8 qtr cycle record 01 = 4 rec of 16 qtr cycle records Table 3 = 2 rec of 32 qtr cycle records 11 = 1 rec of 64 qtr cycle records bit 6 : Single Shot Mode (0=off, 1=on) bit 7 : Append Record Mode (0=off, 1=on)
9/1	Spare
9/2	Checksum (high byte)
9/3	Checksum (low byte)

8.11.3 Arm Waveform Data Accumulation (3 14 2)

Start Waveform data collection.

8.11.4 Disarm Waveform Data Accumulation (3 14 3)

Stop Waveform data collection.

8.11.5 Report Waveform Record Data Headers (3 14 4)

Msg Byte	Definition
1/1	Relay Status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0xe4
1/3	Total Number of Messages = 38
2/1 – 6/3	Unit ID Name (15 characters)
7/1	Record 0: Trigger position
7/2	Record 0: Year
7/3	Record 0: Month
8/1	Record 0: Date
8/2	Record 0: Hours or Most significant high byte millisec time since midnight
8/3	Record 0: Minutes or Most significant low byte millisec time since midnight
9/1	Record 0: Seconds or Least significant high byte millisec time since midnight
9/2	Record 0: Hundredths of seconds or Least significant low byte millisec time since midnight, see note in command 3 5 8.
9/3	Record 0: Voltage Scale High byte
10/1	Record 0: Voltage Scale Low byte
10/2	Record 0: Mode/Record Size bit 0,1 :00 = 8 rec of 8 qtr cycle record 01 = 4 rec of 16 qtr cycle records

Table 3 = 2 rec of 32 qtr cycle records

	11 = 1 rec of 64 qtr cycle records bit 6 : Single Shot Mode (0=off, 1=on) bit 7 : Append Record Mode (0=off, 1=on)
10/3	Record 0: Spare
11/1 – 14/3	Record 1 (same as record 0)
15/1 – 18/3	Record 2 (")
19/1 – 22/3	Record 3 (")
23/1 – 26/3	Record 4 (")
27/1 – 30/3	Record 5 (")
31/1 – 34/3	Record 6 (")
35/1 – 38/3	Record 7 (")

8.11.6 Fetch First Block of a Record (3 14 5)

Data Byte	Definition
1/1	Record number (0 to 7)
1/2	Record number(Duplicate)
1/3	Record number(Triplicate)

Msg Byte	Definition
1/1	Relay status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0xe5
1/3	Total Number of Messages = 34
2/1	Record number
2/2	Block number
2/3	Sample 0: Ia (high byte)
3/1	Sample 0: Ia (low byte)
3/2	Sample 0: Ib (high byte)
3/3	Sample 0: Ib (low byte)
4/1	Sample 0: Ic (high byte)

4/2	Sample 0: Ic (low byte)
4/3	Sample 0: In (high byte)
5/1	Sample 0: In (low byte)
5/2	Sample 0: Va (high byte)
5/3	Sample 0: Va (low byte)
6/1	Sample 0: Vb (high byte)
6/2	Sample 0: Vb (low byte)
6/3	Sample 0: Vc (high byte)
7/1	Sample 0: Vc (low byte)
7/2 – 11/3	Sample 1 data
12/1 – 16/2	Sample 2 data
16/3 – 21/1	Sample 3 data
21/2 – 25/3	Sample 4 data
26/1 – 30/2	Sample 5 data
30/3 – 35/1	Sample 6 data
35/2 – 39/3	Sample 7 data
40/1	Phase scale (high byte)
40/2	Phase scale (low byte)
40/3	Neutral scale (high byte)
41/1	Neutral scale (low byte)
41/2	Input status (high byte). See Figure 14 (p. 365) for bit assignments.
41/3	Input status (low byte)
42/1	Output status byte
42/2	Miscellaneous status byte Bit 0: Trip Bit 1: Breaker failure Bit 2 : Bit 3 : Bit 4 : 32P Fault (DPU2000 and DPU2000R) Bit 5 : 32N Fault (DPU2000 and DPU2000R) Bit 6 : 32P Pickup (DPU2000 and DPU2000R) Bit 7 : 32N Pickup (DPU2000 and DPU2000R)
42/3	Pickup status (high byte) Bit 0: 50N-1 Bit 1: 50N-2 Bit 2: 50N-3 Bit 3: 51N Bit 4: 50P-1 Bit 5: 50P-2 Bit 6: 50P-3 Bit 7: 51P
43/1	Pickup status (low byte) Bit 0: 67P (DPU2000 and DPU2000R) Bit 1: 67N (DPU2000 and DPU2000R) Bit 2: 46 Bit 3: 27 Bit 4: 59 (DPU2000 and DPU2000R) Bit 5: 79 Bit 6: 81S (DPU2000 and DPU2000R) Bit 7: 81R (DPU2000 and DPU2000R)
43/2	Fault status (high byte) Format same as 42/3
43/3	Fault status (low byte) Format same as 43/1

8.11.7 Fetch Next Block of a Record (3 14 6)

Same message format as (3 14 5)

8.11.8 Retransmit Last Block of a Record (3 14 7)

Same message format as (3 14 5)

8.11.9 Fetch Acquisition Status (3 14 8)

Msg Byte	Definition
1/1	Relay status (see command 3 4 1, msg 1/1)
1/2	Command + Subcommand = 0xe8
1/3	Total Number of Messages = 32
2/1	Mode/Record Size
	bit 0,1 :00 = 8 rec of 8 qtr cycle record
	01 = 4 rec of 16 qtr cycle records

Table 3 = 2 rec of 32 qtr cycle records

	11 = 1 rec of 64 qtr cycle records
	bit 6 : Single Shot Mode (0=off, 1=on)
	bit 7 : Append Record Mode (0=off, 1=on)
2/2	Records Remaining (single shot mode)
2/3	State of Accumulation (0=running,1=stopped)

Appendix B - ASCII CODE

Decimal Value	Hexadecimal Value	Control Character	Character
0	00	NUL (CTRL @)	Null
1	01	SOH (CTRL A)	
2	02	STX (CTRL B)	
3	03	ETX (CTRL C)	
4	04	EOT (CTRL D)	
5	05	ENQ (CTRL E)	
6	06	ACK(CTRL F)	
7	07	BEL (CTRL G)	Beep
8	08	BS (CTRL H)	Backspace
9	09	HT (CTRL I)	Tab
10	0A	LF (CTRL J)	Line-feed
11	0B	VT (CTRL K)	Cursor home
12	0C	FF (CTRL M)	Form-feed
13	0D	CR (CTRL N)	Carriage Return (Enter)
14	0E	SO (CTRL O)	Shift Out
15	OF	SI (CTRL P)	Shift In
16	10	DLE	Data Link Escape
17	11	DCI	
18	12	DC2	
19	13	DC3	
20	14	DC4	
21	15	NAK	

22	16	SYN	
23	17	ETB	
24	18	CAN	
25	19	EM	
26	1A	SUB	
27	1B	ESC	
28	1C		Cursor right
29	1D		Cursor left
30	1E		Cursor up
31	1F		Cursor down
32	20		Space
33	21		!
34	22		“
35	23		#
36	24		$
37	25		%
38	26		&
39	27		‘
40	28		(
41	29		(
42	2A		*
43	2B		+
44	2C		,
45	2D		-
46	2E		.
47	2F		/
48	30		0
49	31		1
50	32		2
51	33		3
52	34		4
53	35		5
54	36		6
55	37		7
56	38		8
57	39		9
58	3A		
59	3B		
60	3C		<
61	3D		
62	3E		>
63	3F		?
64	40		@
65	41		A
66	42		B
67	43		C
68	44		D
69	45		E
70	46		F
71	47		G
72	48		H
73	49		I
74	4A		J
75	4B		K
76	4C		L
77	4D		M
78	4E		*N*
79	4F		O
80	50		P

81	51	Q
82	52	R
83	53	S
84	54	T
85	55	U
86	56	V
87	57	W
88	58	X
89	59	Y
90	5A	Z
91	5B	[
92	5C	\
93	5D	]
94	5E	^
95	5F	_
96	60	`
97	61	a
98	62	b
99	63	c
100	64	d
101	65	e
102	66	f
103	67	g
104	68	h
105	69	i
106	6A	j
107	6B	k
108	6C	l
109	6D	m
110	6E	n
111	6F	o
112	70	p
113	71	q
114	72	r
115	73	s
116	74	t
117	75	u
118	76	v
119	77	w
120	78	x
121	79	y
122	7A	z
123	7B	{
124	7C	|
125	7D	}
126	7E	~
127	7F	DEL

Appendix C - Modbus Plus Communication Between an ABB Protective Relay and a Modicon PLC

ABSTRACT: Modbus Plus Capable devices are continuously being introduced into the utility environment. This Application Note is intended to educate the user with the method to use the protective relay and PLC's Modbus Plus capabilities to allow for data access and control capabilities. A simple communication example is intended to give the reader a simple method to establish communication between devices using PLC Ladder Logic. This Application Note relies upon the reader's understanding of Ladder Logic programming of a Modicon PLC and Modbus Plus application.

Modbus Plus General Information

Modbus Plus is a communication protocol, which encompasses the physical layer, data link, transport and application link layer definition within the ISO model representation. The physical layer is a hybrid-defined interface, which allows up to 64 devices to be multi-dropped along a serial interconnection. The interface also allows devices to communicate to each other with a data rate (baud rate) of 1 megabaud. The combination of protocol implementation and baud rate selection make Modbus Plus an excellent high performance protocol desirable for the substation environment.

However, Modbus Plus has been given additional capabilities, which exceed the benefits of a fast baud rate. Modbus Plus is based upon a hybrid implementation of HDLC (High-level Data Link Control) protocol. This implementation allows multiple devices to communicate along a single cable interface. Modbus Plus allows up to 32 (or 64 with the addition of repeaters) devices to communicate along a network connection. Additionally, each device can be capable of transmitting/receiving data of a length of 32 data words, which can be seen by all nodes, attached to the network. Modbus Plus has the Modbus Protocol imbedded within its data transport structure.

Modbus Plus is a deterministic network in that the response time to a command can be reasonably calculated. The method of determinism employed is referred to as "Token Passing". Please refer to both ABB and Schneider Electric documentation referencing network throughput calculation. Each node attached to the network can read/write information in a calculated amount of time which is determined by data transferred along the network and the amount of nodes along the network receiving the token. The amount of time in which to transfer the token to each network is referred to as "Token Rotation Time".

Modbus Plus Communication Between Devices

Modicon Programmable Logic Controllers (PLC's) can communicate with Modbus Plus Capable devices using two methods: Method 1 is using Peer Cop,. Method 2 is using a Master Block.

Peer Cop is a capability used only to allow devices by Schneider Electric to communicate with each other. It enables one device to be configured to read or write from/to each other along a Modbus Plus connection path. It's throughput is dependent upon the Modbus Plus token rotation time.

A Master Block is the PLC's method of using an instruction, which is inserted within the PLC's Ladder Logic scan to access data from another Modbus Plus capable device. A Master Block performs the following data access tasks:

- Write 4X Data to other devices
- Read 4X Data from other devices
- Get Local Modbus Plus Network Statistics
- Clear Local Modbus Plus Network Statistics
- Write Global Database
- Read Global Database
- Get Remote Modbus Plus Network Statistics
- Clear Remote Modbus Plus Network Statistics
- Obtain Node Peer Cop Health Statistics

Data transfer (read or write) is explained later in this document. Network Statistics is a count of each of the node's good / bad transmission counts. If a bad transmission occurs, the nature of the failure is tallied on a table. Local statistics are those from nodes on the same Modbus Plus network, Remote Statistics are those gathered from nodes on other interconnected Modbus Plus networks.

An ABB protective relay has Modbus Plus "HOST" addressing implementation. An additional path entry is required for address assignment for devices which are designed with Modbus Plus "HOST" implementation. An ABB protective relay has the following Modbus Plus features available:

- Place 32 Registers of Data in the Global Database for access by other devices.
- Reply to 4X Read Data Requests from a Host or PLC Device.
- Perform Operations when 4X Write Data Requests are sent by a Host Device.
- Respond to Local and Remote Network Statistics Requests.
- Respond to Clear Local and Remote Local Statistics Requests.

In summary, the ABB protective relay responds to commands from a Modicon PLC as well as place data into the Global Register buffer for retrieval from a host device.

Modbus Plus Node Addressing and Path Designation

Modbus Plus Node addressing for a Modicon PLC is determined by a thumbwheel switch or dipswitch configuration on the appropriate PLC. Please reference the appropriate Schneider Electric Product Manual for further information.

Figure 1 illustrates the Modicon PLC's resident data paths. The PLC has four data slave paths resident in its device. An Additional Global Data Read Data Slave Path is available. It is through these paths that the PLC shall obtain the relay information.

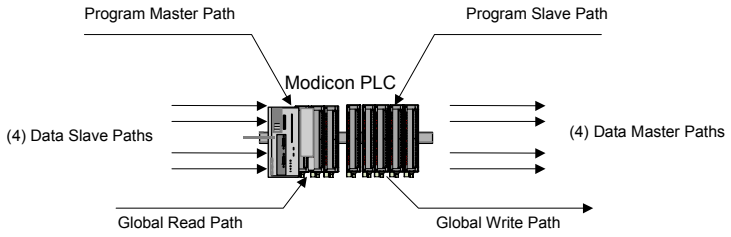


Figure 16. Typical Modicon PLC Modbus Plus Path Definition

The ABB Relay implementation host paths are shown in Figure 2. A comparison of the data paths shows the similarities and differences between the PLC and ABB Relay implementation.

The ABB Relay however, requires an additional path added to its base address to complete the full Modbus Plus address. As per the Figure 2 implementation, 8 data slave paths are incorporated within the relay. For a PLC to access the data within the relay, a base address of the node and one of the eight path addresses must be given for the address.

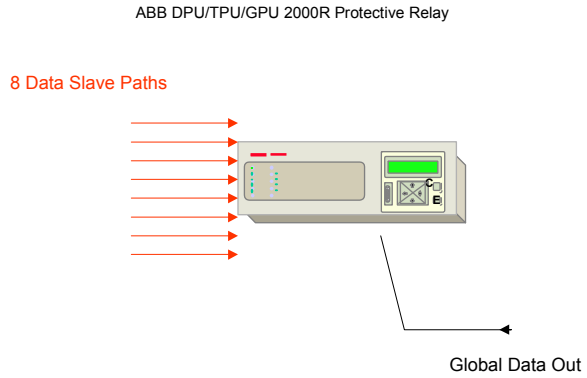


Figure 2. ABB Protective Relay Path Implementation

Setting the address, of the ABB protective relay is accomplished via the front panel interface or via the ECP programming software accessible via the programming port. The address is in HEX encoding.

For example, if the PLC in Figure 1 was configured for address 1 and the ABB Protective Relay was configured for address 10 decimal (or configured as ADDRESS "A" hex through the front panel or ECP), the PLC would address the relay through one of any of the following addresses:

- 10.1.0.0.0 - Address 10 Path 1
- 10.2.0.0.0 - Address 10 Path 2
- 10.3.0.0.0 - Address 10 Path 3
- 10.4.0.0.0 - Address 10 Path 4
- 10.5.0.0.0 - Address 10 Path 5
- 10.6.0.0.0 - Address 10 Path 6
- 10.7.0.0.0 - Address 10 Path 7
- 10.8.0.0.0 - Address 10 Path 8

The Master Block Explained

The Modicon PLC allows for 4X data retrieval via Modbus Plus. The PLC scans ladder logic as such: Read PLC INPUTS -→ Execute LADDER LOGIC → Write PLC Outputs. The PLC scan is illustrated in Figure 3. The PLC reads the physical inputs wired into the unit, executes the program written in the PLC's native language (icon based Ladder Logic), and writes the status to the physical Output modules to control the hardwired components.

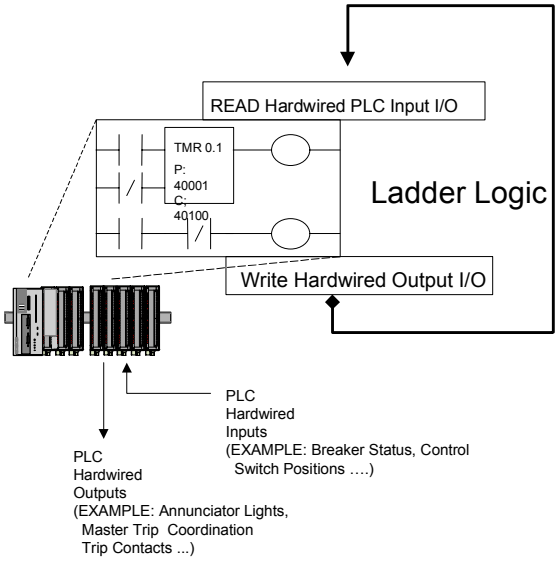


Figure 3. Typical PLC Logic Execution

Within the PLC, a Master Instruction should be programmed within the unit which when scanned and executed, the PLC will transmit/receive data over the Modbus Plus Network. It may take more than one PLC scan to obtain the data over the network. The PLC scan is never stopped to wait for the data. The PLC will continue with its logic execution and upon a new ladder logic scan, a determination will be made by the instruction as to whether it received the information in the appropriate amount of time. The throughput of the data acquisition is determined by a variety of factors:

- Ladder Logic Execution Speed.
- Token Rotation Speed of Modbus Plus.
- Amount of data travelling over the network at the time of the request.
- Latency of the receiving device to respond to the request when received.

The MSTR (Master) Block is illustrated in Figure 4. A single PLC may have up to four Master Blocks active at any one time accessing data from the ABB protective relay. The amount of data, which may be requested by a PLC, is determined by the amount of free data paths available on the PLC. The ABB protective relay has up to 8 data paths, which may be accessed and busy at one time. The MSTR instruction block is parameterized via the PLC's Ladder Logic to perform the intended functions as illustrated via the function codes. If one was to obtain data from the GLOBAL data path, the amount of active MSTR instructions could be in a number greater than four.

The MSTR instruction is executed whenever the ENABLE instruction leg is energized. If the instruction is enabled, the ACTIVE output at the right side of the instruction shall energize. When the instruction has executed correctly, the COMPLETE instruction leg shall energize and the ACTIVE leg shall de-energize. If an error occurs within parameterization or timeout of the network without a response, the ERROR leg shall energize and the ACTIVE leg shall de-energize. The parameterization shall occur through configuration of the correct 4XXXX registers via the table provided for the instruction. If an error occurs, register 4XXXX +1 shall contain a number other than 0 indicating the failure. If a successful communication occurs, the data will be transferred into register block 4YYYY to 4YYYY + NNN (if a read operation or network statistics read operation) or data transferred from the PLC block 4YYY to 4YYYY + NNN if the MSTR operation is a write.

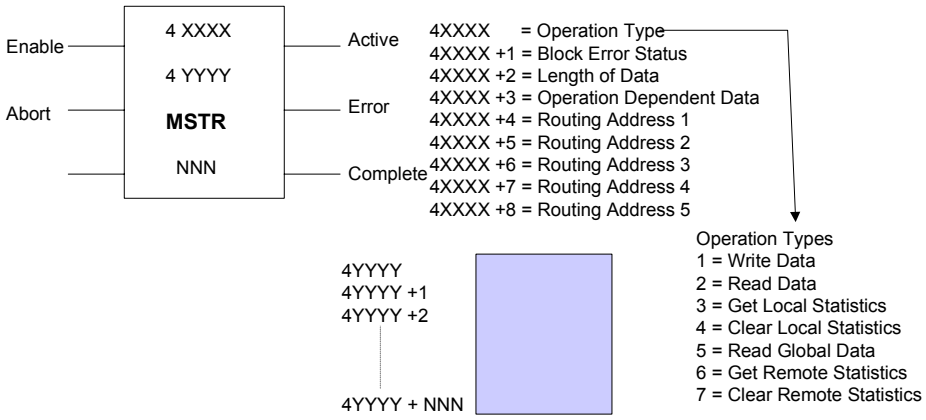


Figure 4. Modbus Plus Master Instruction

Meter Data Access To a PLC Host From an ABB Relay

Figure 5 illustrates a typical installation in which a PLC is to access data from an ABB DPU2000R using a Master Instruction.

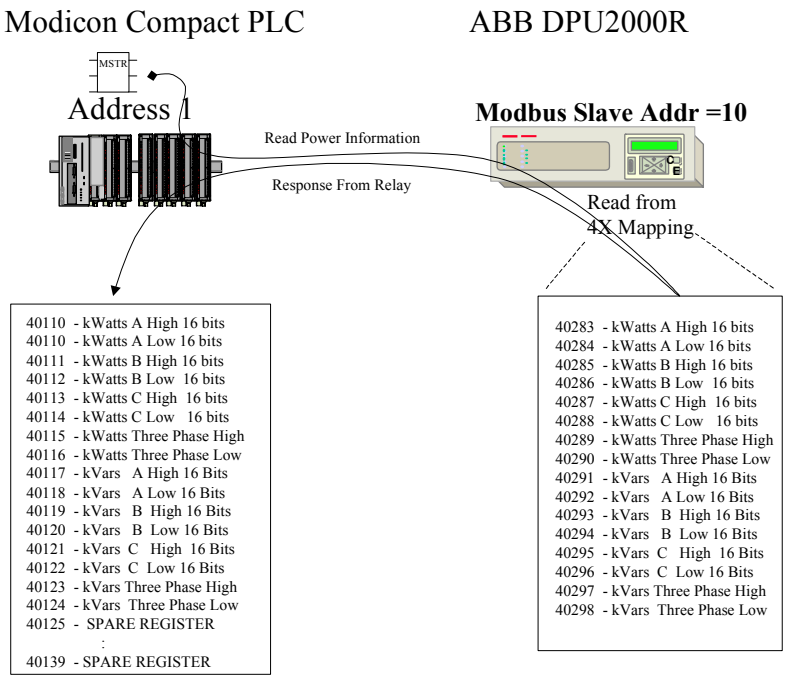


Figure 5. Modbus Plus Network Topology MSTR Read Instruction Example

A sample Ladder Logic Instruction network is given in Figure 6. The ladder logic is included for instruction purposes only. The MSTR instruction is energized by internal coil 00107. If the instruction is active, coil 00102 energizes to request the information from the ABB protective relay. If the block is parameterized incorrectly, coil 00103 will energize and register 400101 will contain a non-zero number indicating the fault type. If the Ladder Logic instruction obtains the information from the relay, output coil 00104 shall energize indicating completion of the network access. Also within this network example, an counter will increment each time a successful network communication occurs. This count, contained in the PLC memory 400109 can serve as a heartbeat counter to monitor continuous and successful communications.

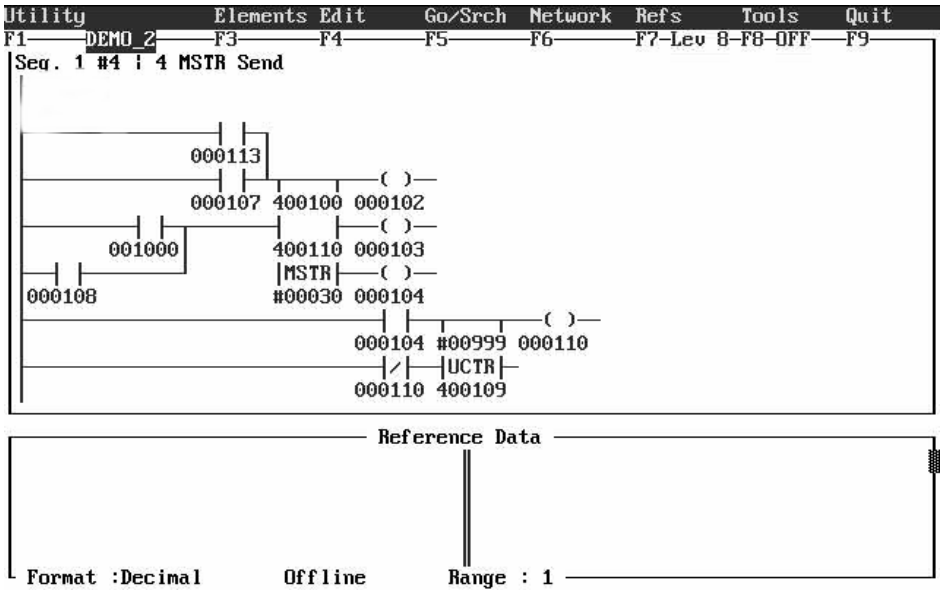


Figure 6. MSTR Ladder Logic Network Example

The MSTR is intended to access data from the ABB Protective relay. Figure 7 illustrates the Registers 400100 through 400108 which must be parameterized in order to obtain relay data. Figure 7 shows the MSTR configuration screen containing the parameters required for the Ladder Logic to operate correctly.

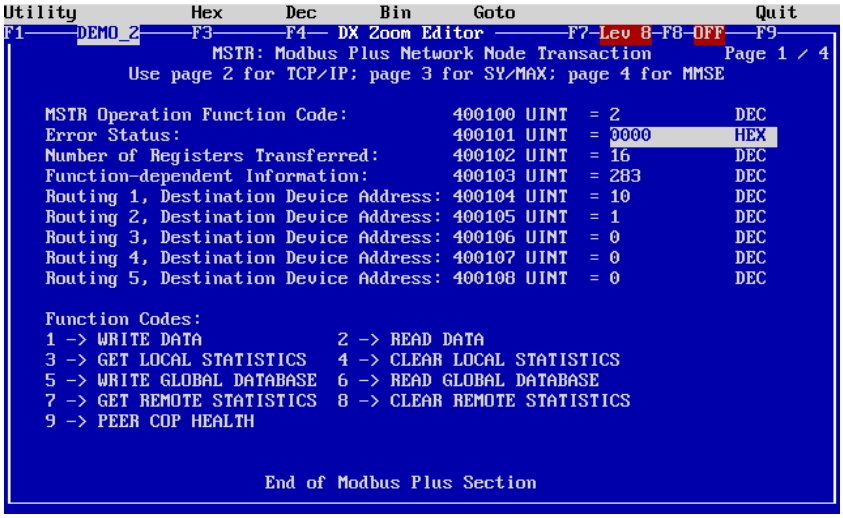


Figure 7. MSTR Configuration Parameters

This example illustrates the configuration of Reading (PLC Register 400100 = 2) sixteen registers (PLC Register 400102 = 16) representing KW phase A,B,C, Total KW, KVARS phase A,B,C, and Total KVARS (Function Dependent Information from ABB DPU2000R Modbus Address 40283), at Node number 10 (DPU2000R = Node 10 [Address = 00A HEX]). Note the RELAY address is specified as the configured address via the relay front panel (Register 400104 = 10) and the Modbus Plus Data Slave path (in this case Data Slave Path 1 as designated in Register 400105 = 1).

Each time the MSTR instruction is executed, the data as designated in the parameterization block of 400100 to 400108 shall be transferred from the DPU 2000R's address to the PLC's data buffer which in this case resides in addresses 400110 through 400139 (as designated by the length of 30 at the bottom of the MSTR instruction). As illustrated in Figure 5, the data is transferred from the ABB DPU2000R's register map to the PLC's registers as illustrated.

Ladder logic may be written to change the parameters within the MSTR block so additional values may be obtained from the ABB DPU2000R. A sample ladder logic construct is included in Figure 8 which energizes the MSTR instruction when its operation has terminated.

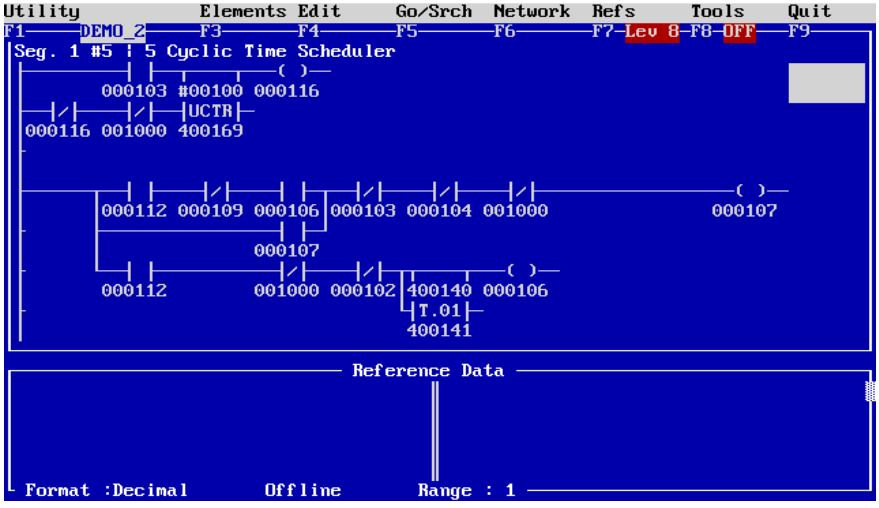


Figure 8. MSTR Cyclic Timer Ladder Logic

Figure 8 ladder constructs are as such:

01000 is a system reset contact which when energized resets the MSTR and counters.
00112 is a system start contact which when energized allows the MSTR to read network data over Modbus Plus.

If the network MSTR is idle (coil 00102 is de-energized or at a state of 0) then the timer energizes for the time indicated in Register 400140. Upon timeout, 00106 energizes and latches in 00107 which starts the MSTR instruction. Coil 00107 will be reset (or unlatched) when the MSTR terminates operation normally or through error. Upon reset, the MSTR instruction will not execute. The timer shall reset and when it times out, the entire sequence shall begin again.

The UCTR instruction contained in this logic counts the amount of Modbus Plus errors encountered when communicating to the relay. Its count is kept in Register 400169.

Additional ladder logic can be written to transfer different pointers to obtain additional information from the DPU2000R. The data would have to be transferred to Registers 400100 to 400108. The logic is relatively straightforward.

Conclusion

The ABB series of Protective relays have been designed and certified to operate seamlessly with Modicon Programmable Logic Controllers. The Ladder Logic is straightforward and easily implemented. Metering data, element status, fault/operation records, device settings, and other important and time-critical information is easily obtained from the relay using a programmable logic controller with Modbus Plus capability.

Reference Text

DPU/DPU2000R Modbus/Modbus Plus Implementation and Protocol Guide, Revision 1.5, August 18, 1998. ABB Company

INSTRUCTIONS – DPU2000R Distribution Protection Unit 1MRA587219-MIB (IB 7.11.1.7-4), REF 544, Issue B, October 1997, ABB Company

MODICON LADDER LOGIC BLOCK LIBRARY USERS GUIDE 840 USE 101 00, Version 1.1, July 1995, AEG Schneider Automation

MODICON MODSOFT Programmer Software User Guide, 840 USE 115 00, Version 1.1, June 1996, AEG Schneider Automation

MODBUS PLUS and SUBSTATION AUTOMATION, 8000BR9606R 11/97, REV C, Groupe Schneider

Appendix D - Telebyte RS232/485 Converter Connection to ABB Protective Relays

***ABSTRACT**: There are many RS232 to RS485 converters on the market. Although ABB cannot and does not endorser a particular manufacturer of product, it does document several manufacturers' products with their use in systems using ABB protective relays. This application note illustrates the setup and connection of the Telebyte Model 245 optically isolated RS232 to RS485 (2-wire/4wire) physical interface converter.*

Typical Installation

The ABB protective relay is designed with a variety of physical communication interfaces. The ABB distribution relays such as the MSOC, GPU2000R, TPU2000R, DPU2000R, DPU2000, and DPU1500R are available with an RS232, and/or RS485 port(s).

Other devices such as the PONI M card for the REL356 have only an RS485 port.

Many host devices only have an RS232 port(s). A method to connect such a device is required. Several converters are available to transform the physical interface on a device from RS232 to RS485. The advantages of RS485 are that many devices may be attached to a single host in a multi-drop topology. RS485 may communicate with up to 32 devices with an addressable protocol. An advantage of the Telebyte 245 converter is that, like the ABB protective relay, it is an isolated device.

General Information

Figure 1 illustrates the packaging of the Telebyte converter. The Telebyte Converter has two sets of red LED's indicating transmission and reception of information on its ports. One set of LED's indicates transmission/reception of data on its RS232 port. The second set of LED's indicates transmission/reception of data on its RS232/RS485 port. These LED's are invaluable in visual troubleshooting of communications.

The Telebyte converter has two sets of DB 25 connectors. One connector is a standard RS232 interface whereas the other connector is the RS485/RS422 interface. Switches 1 and 2 configure the RS485 interface. A DTE/DCE (Data Terminal Emulation/Data Communication Emulation) switch configures the RS232 pins determining where the data is expected (DTE = Data is Transmitted on Pin 2 and Data is Receive on Pin 3| DCE = Data is Transmitted on Pin 3 and Data is Received on Pin 2) on the RS232 interface. Furthermore, Switch 2 configures the RS485-control mode from the RS232 port. In two-wire emulation, data control may occur from the RS232 port's RTS (Request To Send) line or whether the data on the TD (Transmitted Data) pin is sensed. If the ABB device is a MSOC, GPU2000R, TPU2000R, DPU2000R, DPU2000, and DPU1500R, no data handshaking is permitted, thus the RS232/485 converter must be configured for TD (Transmitted Data) mode. However, if the device attaching to the RS232 port is a host which utilizes RTS/CTS (Request To Send/ Clear To Send) handshaking, the unit must be configured using the RTS dipswitch settings as illustrated in Figure 1. Additional information on the Telebyte 245 Optically Isolated converter is available on their website at www.telebyteusa.com.

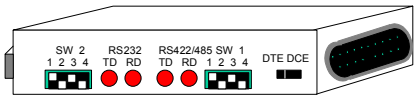
There are several steps required to successfully install a communication network using a physical interface converter. They are:

1. Knowledge of the RS232 interfaces. (What type of handshaking is employed? Is the port DCE or DTE emulation?, Does the program executing on the attached device require certain signals such as CTS [Clear To Send], RTS [Request To Send], CD [Carrier Detect], DTR [Data Terminal Ready])? What is the voltage of the RS232 interface signals?)
2. Knowledge of the available power required. (If the converter requires external power, what is the voltage required?)
3. Knowledge of the RS485 devices connected (2 Wire or 4 Wire?, Biasing Required?, Length of network?, Number of Devices Attached? Are the devices isolated?)
4. Proper installation of bias resistors.
5. Proper installation of termination resistors.
6. Proper selection and installation of the physical cable medium.

7. Proper configuration of the RS232/485 physical interface switches and dipswitches.

TELEBYTE 245 OPTICAL ISOLATOR CONVERTER

RS 232 RS485/RS422



The 245 uses Pin 2 (TX/RX -) & Pin 14 (TX/RX +), Pin 7 is Ground for its connections to the Two Wire RS-485 Relay.

RS 485 SWITCH MODE (2 wire)	SW 1				SW 2			
	1	2	3	4	1	2	3	4
TRANSMIT DATA CONTROL	UP	DOWN	UP	DOWN	X	DOWN	UP	Y
RTS DATA CONTROL	UP	UP	DOWN	UP	X	DOWN	UP	Y
X = TERMINATION RESISTOR , UP = INSERTED : DOWN = OUT					Y = DON'T CARE			

Figure1. Telebyte Dipswitch Settings

RS232 Configuration and Cabling

The Telebyte RS232 section of the converter uses the following pins:

Pin 2 - Transmit Data
Pin 3 - Receive Data
Pin 7 - Ground

The RS232 connector on the converter is a DB 25 male connector.

Depending upon the dipswitch settings, the following pins are used for transmit data control.

Pin 4 - Request To Send
Pin 5 - Clear To Send

Although the Telebyte converter does use handshaking and control of the DTR signal (Pin 20), its use is not covered in this application note.

The Telebyte converter is an actively powered device requiring attachment to a supplied power transformer. This transformer supplies power to both ports on the unit. No additional power supplies are required for this converter to operate.

The Telebyte converter has an additional dipswitch configuring the RS232 port for DCE or DTE configuration. Figures 2 and 3 illustrate cable pinouts to connect a PC or ABB to connect to a device. If the converter is attached to a PC Host device or an ABB IED, a straight through cable may be used (or a 9 pin to 25 pin cable) to attach the devices. The DTE/DCE switch must be placed in the DCE position due to the nature of RS232 connections. If additional discussions of RS232 are required, please consult the ABB Faxback System (610-877-0721) or the ABB website (www.abb.com/substationautomation). Several documents are available explaining RS232 communication. The Telebyte converter has a DB 25 connector whereas the ABB IED's and most personal computers have DB 9 connectors. Figures 2 and 3 illustrate the cable connections are handshaking is used (RTS/CTS) control or if no handshaking (data control using the Transmitted Data line) is employed. Configuration of the data control handshaking mode is performed via the dipswitches located at the side of the converter. Refer to Figure 1 of this document for dipswitch configuration.

Cable "A"- RS232 Cable for Connection from a NODE (DTE OR DCE) and the Telebyte converter configured correctly (DTE device and Telebyte switch in DCE mode --OR-- DCE device and Telebyte switch in DTE mode). Data control RTS/CTS handshaking employed.

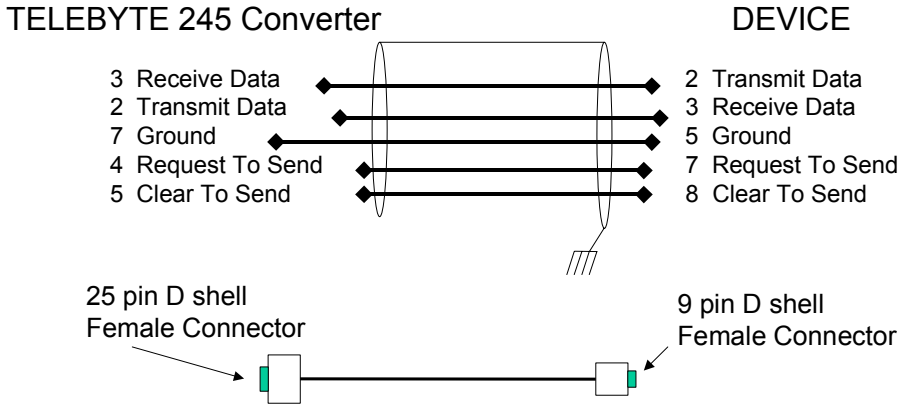


Figure 2. RS232 Cable Pinout with Handshaking Incorporated (See Figure 1 for Dipswitch Settings

Cable "A"- RS232 Cable for Connection from a NODE (DTE OR DCE) and the Telebyte converter configured correctly (DTE device and Telebyte switch in DCE mode --OR-- DCE device and Telebyte switch in DTE mode). No handshaking Data Control via the Transmitted Data (TD) line.

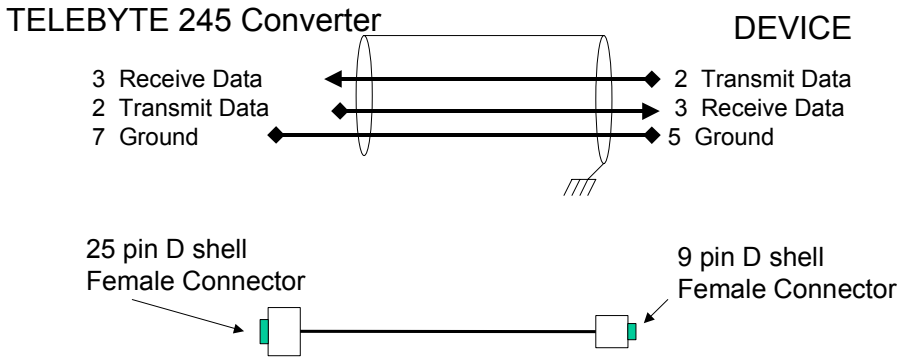


Figure 3. RS232 Cable Connections when no Handshaking is used. See Figure 1 for Dipswitch Settings

Power Requirements

The Telebyte converter is available using a variety of power supply options. The converter is supplied with a power converter, which attaches to which attaches to the device. For current options, please consult the Telebyte website.

RS485 Configuration and Cabling

The Telebyte converter supports RS422, 4 Wire RS485 and 2 Wire RS485 connectivity. The ABB line of protective relays supports 2 Wire RS485 connectivity. The dipswitch settings in Figure 1 are given only for the RS485 two wire options. If additional configuration information is desired for RS485, 4 wire or RS422 configuration please consult the Telebyte website.

The attractive feature of the Telebyte converter is the isolation of the RS232 and RS485/422 ports from external power supplies. This feature is important especially in utility applications where external noise is an issue.

RS485 cabling is usually the source of most communication issues. Several issues must be remembered when installing such a cable:

1. In attachment to ABB relays in a Utility installation, one must remember to use a cable with 3 wires and a shield. Refer to Figures 4 through 7 for ABB recommended cables.
2. Termination must be attached to the extreme ends of the cable. If ABB relays are at the extreme ends of the cable, internal termination resistors are available to provide termination. If the Telebyte converter is inserted at the end of the cable, Switch Bank 2, Dipswitch position 1 inserts or removes a 120 ohm resistor in the circuit.
3. The cable attaching the nodes must be daisy- chained. Drops, Taps and stubs of cables are not supported. The addition of terminals, drops, taps, and cable stubs increase the signal reflections thus increasing the possibility of communication errors.
4. The CABLE SHIELD is grounded at one place only. The cable shield is continuous through all nodes, but it is isolated from the ground potential at each device.
5. The ABB protective device RS485 ports are optically isolated, the ground wire must be attached to the shield ground at one place only. This is required to reference the field side of the device interface to a common reference.

RS485 Line Termination

RS485 2 Wire connection diagrams are referenced in Figures 4 through 7. Figures 4 and 5 use the internal resistors within the DPU, GPU, TPU and MSOC units. Figures 6 and 7 illustrate an alternate method of using external resistors to provide biasing and line termination.

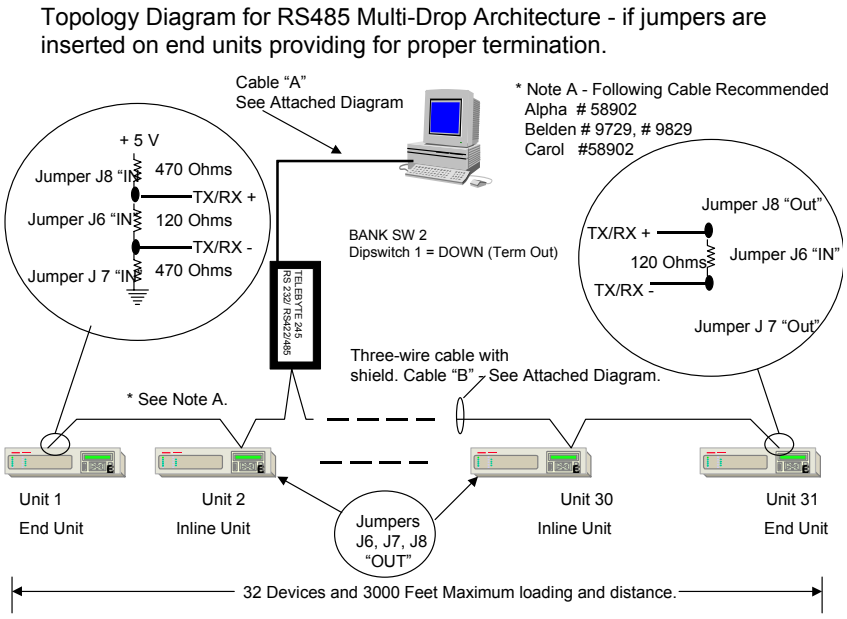


Figure 4. RS485 2 Wire Termination with the RS232/485 Converter In Line and ABB Protective Relays At End Of Line Locations

Topology Diagram for RS485 Multi-Drop Architecture - if jumpers are inserted on end units providing for proper termination and converter is at End Unit.

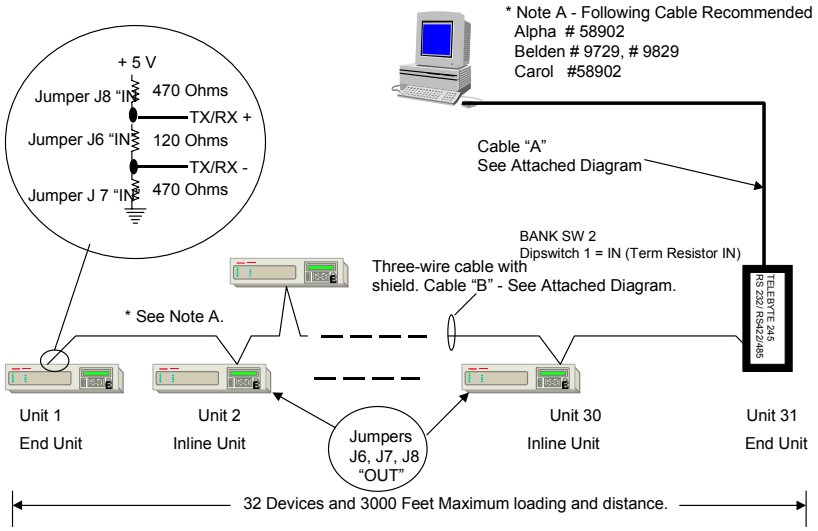


Figure 5. Termination Using Internal Jumpers and Converter as an End Unit

One should recognize that termination is at both extreme ends of the cable. Also Figures 4 and 5 have the cable daisy-chained, thus minimizing communication signal reflections.

Topology Diagram for RS485 Multi-Drop Architecture - if external resistors are installed providing proper termination. NOTE: Termination at end units.

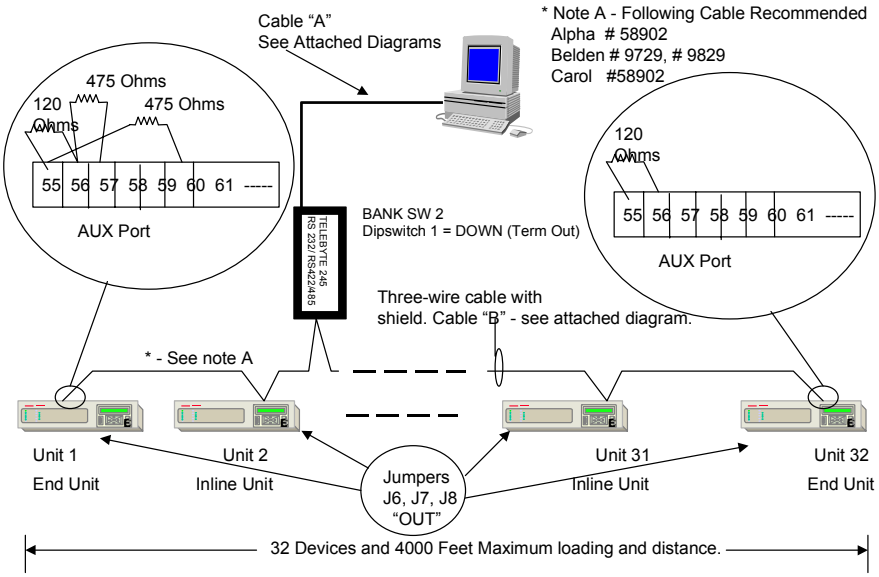


Figure 6. Termination Using External Resistors and the Telebyte Converter Being as "In-Line" Unit

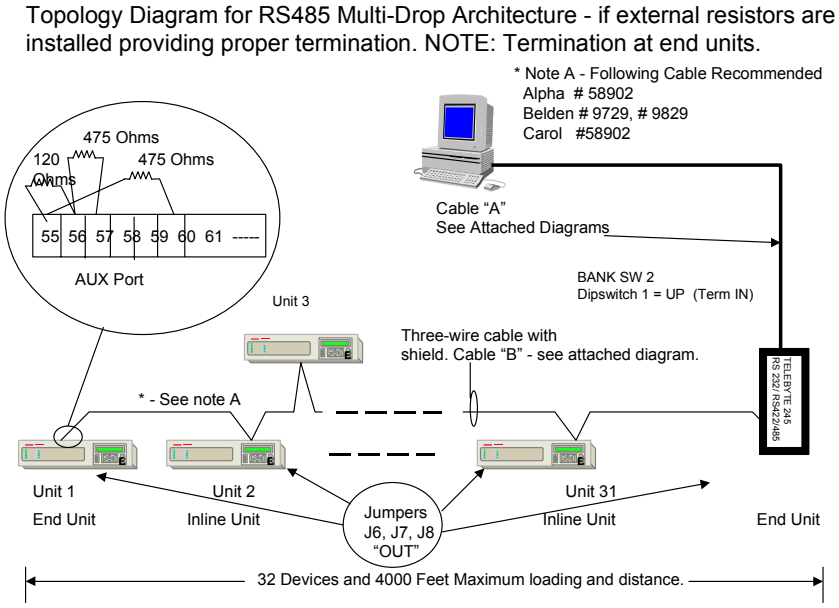


Figure 7. Termination Using External Resistors on the IED's and Using the Telebyte Converter as an End Unit

RS485 Biasing

Figures 4 through 7 illustrate the addition of resistors between the TX/RX (+) line and +V, and TX/RX (-) line and ground. These resistors are called bias resistors. Bias resistors are inserted at one node only, preferably at one extreme end of the network.

The Telebyte 245 is a "passive bias" unit in that when no device is communicating on the network, the data lines float. With the addition of the Pull-Up and Pull –Down resistors, the line is biased when no device is driving the lines. Biasing reduces the communication lines from being saturated with RFI or EMI induced noise from being coupled on the line. Addition of biasing on the network reduces the induced noise on the line.

The typical utility installation is an electrically noisy environment. Addition of data line biasing is recommended.

RS485 Conductor Connectivity

The Telebyte unit uses the following pins for RS485 communication:

PIN 2 - TX/RX (A) or TX/RX (-) or A
PIN 14 - TX/RX (B) or TX/RX (+) or B
PIN 7 - GROUND

The Telebyte interface is a DB 25 Female interface.

Figures 8 and 9 illustrate the individual conductor connectivity for attaching the ABB protective relays in the DPU/TPU/2000 and the DPU/TPU/GPU2000R. It is important to note that Figures 8 and 9 illustrate only the attachment of each device terminal. Each node must be daisy-chained as illustrated in Figures 4 through 7.

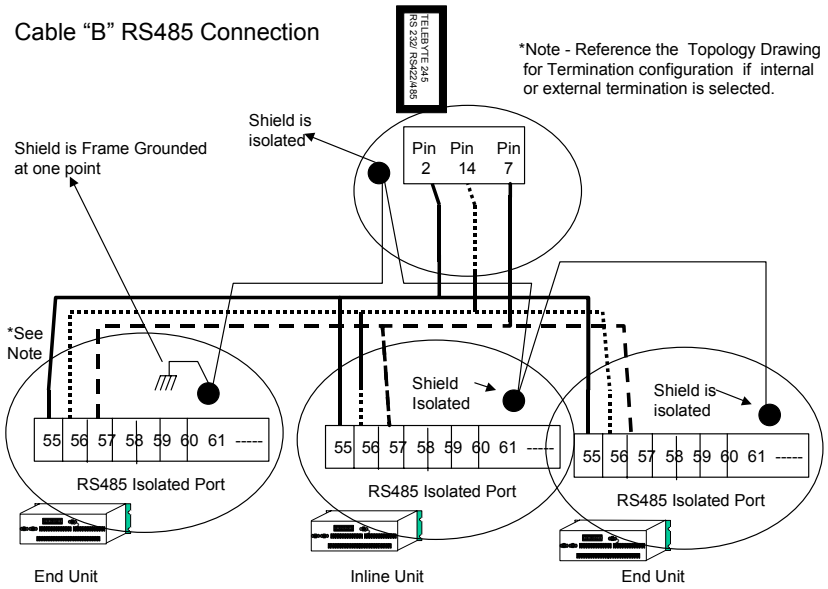


Figure 8. Conductor Connectivity Diagram for the 2000R Products and the Telebyte Converter “Inline”

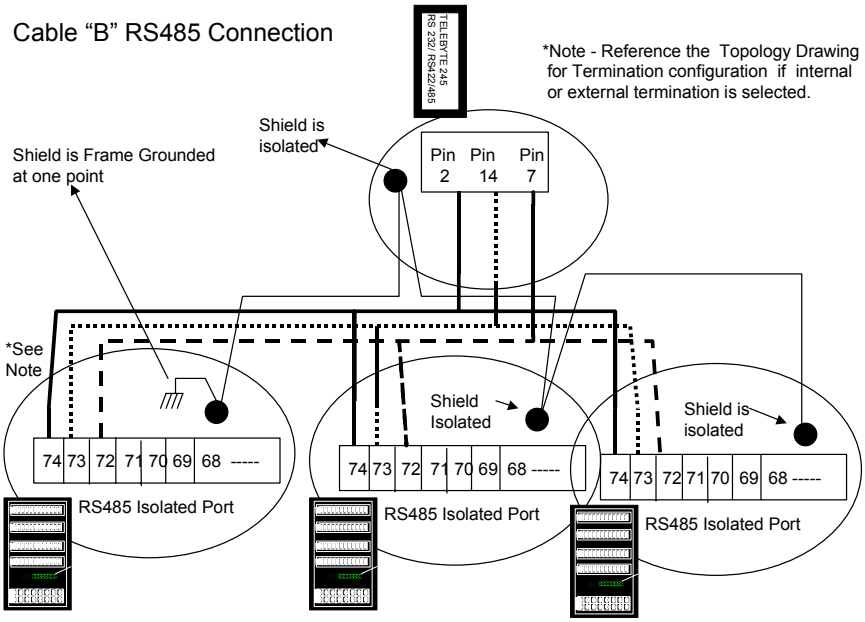


Figure 9. Conductor Connectivity Diagram for the DPU/TPU2000 Products

If an ABB relay uses a TYPE 8 card, COM Port 3 is actually an RS485 port presented in a DB 9 format. The Pin designation is presented in Table 1 and lists the cross listing for the AUX COM connector present on the 2000R product and 2000-product line. As illustrated in Figures 7 and 8, the AUX COM Port connections are given. If one is installing RS485 on a TYPE 8 card, both the AUX COM Port and COM 3 have RS485 connectivity available.

Table 1. RS485 Communication Card RS485 Cross-Reference List

PIN DESIGNATION	COM 3 TYPE 8 COM PORT (2000R Family)	AUX COM PORT (2000R Family)	AUX COM PORT (2000 Family)
+ 5 VDC	8	60	77
RS485 Common	7	57	74
RS-485 (-)	2	56	73
RS-485 (+)	1	55	72

Wire attachment on an RS485 TYPE 8 card's COM 3 DB 9 port can be tricky in an in-line installation. ABB has a special connector, which changes the female DB 9 port into a PHOENIX contact 9-pin connector (similar in format to the AUX COM Port). The ABB part number of this 9 Pin male to Phoenix Card Connector is ABB part 602133-009. The same part is also available from Phoenix Contact and the part number is 27 61 50 9.

Troubleshooting

The Telebyte RS232/RS485 converter Model Number 245 has the advantage of four LED's present at the side of the unit (as indicated in Figure 1) indicating RS232 port transmit data, RS232 port receive data, RS485 port transmit data and RS485 port receive data. Visual indication of these LED's should allow the implementor to troubleshoot a unit, which does not communicate at all.

If communication messages do not appear to be transferred from the RS232 port to the RS485 port, one should investigate wiring, DTE/DCE emulation switches, and the wiring on the RS232 and RS485 ports.

If the error rate of communication message transmission and reception is high, investigate wiring in the areas of:

1. Biasing of the cable in only one location.
2. Installation of termination resistors at two nodes only (at both remote ends).
3. Cable installation with three wires AND A SHIELD. REMEMBER SHIELD IS NOT GROUND.
4. Daisy-Chaining the RS485 wiring so no in-line stubs, taps, and junction strips are inserted in the unit.
5. Incorrect installation of the Shield (connected at in line nodes and isolated at ground).
6. Incorrect lengths of RS485 or RS232 cables (3000 feet = RS485 or 50 feet = RS232).
7. Incorrect selection of "handshake control" for operation with the IED or Host (ABB IED's do not employ handshaking. Some hosts require RTS/CTS handshaking or the CD and DTR signal must be looped back in the cable.)

Conclusion

There are many converters available on the market. Successful communication can result in using many manufacturers' physical interface converters. Success in implementing a physical interface relies on the implementor's knowledge of the software control of the physical interface, IED physical interface operation and knowledge of the particular brand of converter.

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