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Abstract

An analytical model has been proposed to describe the onset current for the initial snapback in the transistor on-state mode and in the blocking state of Reverse Conducting (RC)-IGBTs. The considered RC-IGBTs are vertical with soft punch-through (SPT) type buffer designs. The analytical model has been evaluated with the aid of 2-D device simulations and measurements. We have investigated the initial snapback phenomenon at different temperatures and also for different voltage class devices. From the analytical model as well as simulation and measurement results, we have found that for a given voltage class and technology (anode and buffer profiles), the p^+-anode width is the only remaining design degree of freedom which determines the initial snapback. The adjustment of the on-state losses can then be done with the proportion of the n^+-short region.

Keywords: IGBT, RC-IGBT, Power Semiconductor Device, Initial Snapback.

INTRODUCTION

Today the vast majority of IGBT applications are voltage source inverters. In such applications the IGBT conducts or blocks the current in forward direction, while an external diode, connected anti-parallel to the IGBT, conducts in reverse direction. The three different modes alternate throughout the operating cycle. With the advancements of modern IGBT and diode structures, more development effort is being aimed at reviving the RC-IGBT concept (monolithic integration of IGBT and diode in a single chip) to achieve high power handling capability of the inverter i.e. high power density for a given foot print of the power module.

Recently, the RC-IGBT has attracted much attention in power electronics, as semiconductor manufacturers started to integrate the diode into the IGBT structure [1-7]. This approach is advantageous because the diode, i.e. an extra chip, can be eliminated and the area as well as the additional fabrication cost can be saved. In addition, the temperature ripples of the chips can be reduced, which leads to improved reliability of the power modules [8-10]. Fig. 1 illustrates the schematic structure of an RC-IGBT in which the introduced n^+-type doped areas at the anode side act as a cathode for the internal integrated diode. However, due to the introduced anode shorts, RC-IGBTs show a large initial snapback and several secondary snapbacks as shown in Fig. 2. This initial snapback phenomenon is well known from Anode-Shorted Lateral-IGBTs [11-13]. The secondary snapbacks are of least concern as they can be completely eliminated with the radial layout design of anode shorts [14].

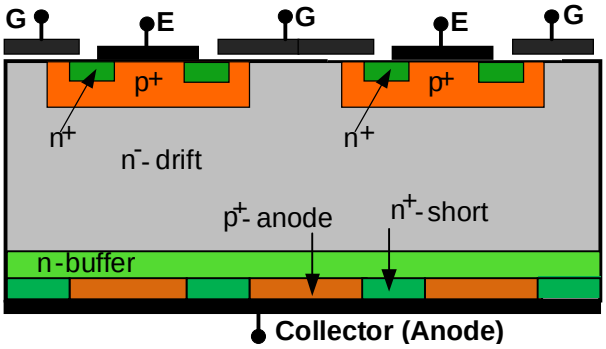


Figure 1: The schematic structure of an RC-IGBT.

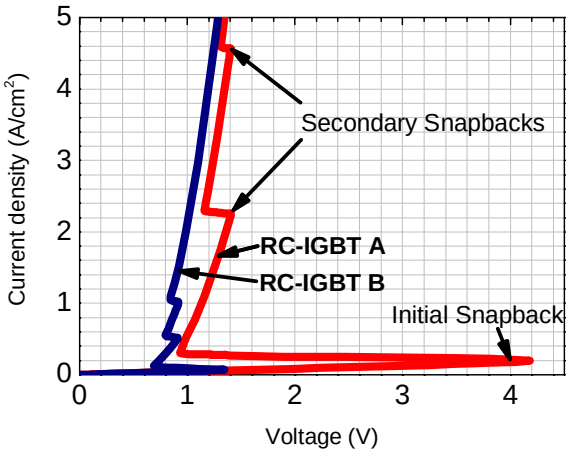


Figure 2: Simulated I-V characteristics of two RC-IGBTs (different widths of the anode shorts) in transistor on-state mode.

However, until today, no analytical model has been reported for the initial snapback phenomenon in vertical RC-IGBTs but many authors have published simulation and experimental results [1, 15-17].

SNAPBACK PHENOMENON

In the structure of the RC-IGBT as shown in Fig. 3, the MOS cells at the front side are replaced by equivalent n-source cells for the ease of the simulations.

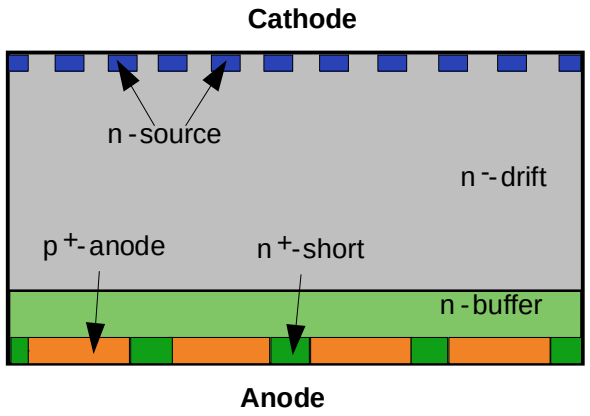


Figure 3: The schematic structure of RC-IGBT in which the MOS cells at the front side are replaced by n-source cells.

In the transistor on-state mode, i.e. when a positive voltage is applied to the anode (collector) with respect to the cathode (emitter), there is a unipolar current flow due to electrons (electrons flow from n-source at the cathode side to the n^+-short at the anode side via the drift and buffer regions) like in a MOSFET.

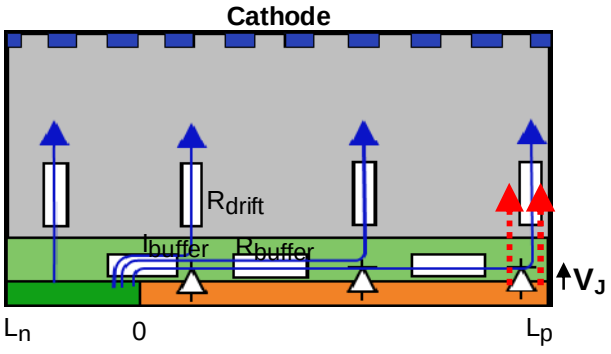


Figure 4: Single anode shorted structure showing the electron current flow with the solid arrow lines before the initial snapback (the device is represented with distributed resistances). The dotted arrow lines show the onset of carrier (hole) injection at/around L_P when there is a sufficient voltage drop (the junction between p^+-anode and n-buffer is represented with distributed diodes).

The solid arrow lines in Fig. 4 illustrate the unipolar current flow, i.e. the electron current flow, in the RC-IGBT. As the current increases, the lateral electron current flow through the buffer produces an increasing voltage drop (junction voltage V_J) across the junction between p^+-anode and n-buffer. The voltage drop is maximum at position L_p (at the middle of the p^+-anode region considering the mirroring effect due to the boundary condition in the simulation). The p^+-anode starts injecting carriers (holes) into the n^--drift region at/around position L_p when there is a sufficient voltage drop. The dotted lines in Fig. 4 illustrate the onset of minority carrier injection at/around position L_p. This happens just before snapback and the onset of snapback occurs when the hole concentration in the n^--drift region is comparable to the doping concentration or even higher (conductivity modulation of the drift region causes the significant reduction of the drift region resistance, which leads to a snapback in voltage).

ANALYTICAL MODEL

For the analytical model of the initial snapback phenomenon of the striped anode shorted design, the infinite small interval dx as shown in Fig. 5 has to be analyzed. The current $I_{buffer}(x)$ in the buffer layer decreases by the amount of dI_{buffer} while passing through the interval dx. Certainly, the difference dI_{buffer} appears as a current $J_{drift} \cdot b \cdot dx$ in the n^--drift region. The J_{drift} can be written in terms of electric potential φ and drift region differential resistance $r_{diff(drift)}$ [Ωcm^2]. The relation between dI_{buffer} and φ can be written as follows,

$$dI_{buffer} = -J_{drift} \cdot b \cdot dx = -\frac{\varphi}{r_{diff\,(drift)}} \cdot b \cdot dx \qquad (1)$$

where the minus sign indicates that I_{buffer} decreases by dI_{buffer} and the b is the width of the device as shown in Fig. 5. The electric potential φ decreases by dφ due to $I_{buffer}(x)$ flowing through the infinite small interval dx. The relation between dφ and I_{buffer} can be written as follows,

$$d\varphi = -r_{sheet(buffer)} \cdot I_{buffer} \cdot \frac{dx}{b} \qquad (2)$$

where $r_{sheet(buffer)}$ is the sheet resistance of the buffer [Ω/□] and the minus sign here indicates that the potential φ decreases by dφ. The above two equations can be rewritten as follows,

$$\frac{dI_{buffer}}{dx} = -\frac{b}{r_{diff\,(drift)}} \cdot \varphi \qquad (3)$$

$$\frac{d\varphi}{dx} = -\frac{r_{sheet(buffer)}}{b} \cdot I_{buffer} \qquad (4)$$

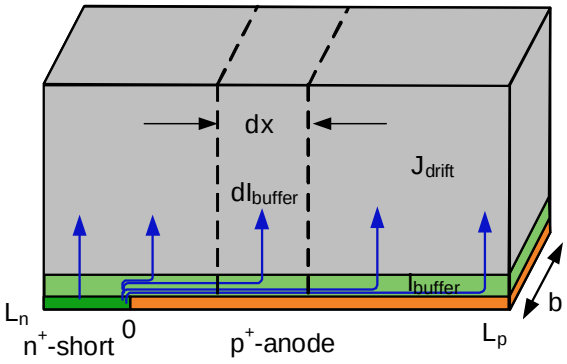


Figure 5: Single anode shorted structure (3D view) showing the electron current flow before initial snapback.

There are two variables I_{buffer} and φ in eq.(3) and eq.(4). However, one of the variables (say φ) can be eliminated by differentiating eq.(3) with respect to x and then substituting eq.(4) in the place of dφ/dx. Finally, one obtains a differential equation of the form y`` = αy:

$$\frac{d^2 I_{buffer}}{dx^2} = \frac{r_{sheet(buffer)}}{r_{diff(drift)}} \cdot I_{buffer} \qquad (5)$$

solving the above differential equation (using hyperbolic functions) with the boundary conditions such that the current through the buffer layer is maximum ($I_{buffer} = I_0$) at x = 0 and zero ($I_{buffer} = 0$) at $x = L_p$, one can obtain,

$$I_{buffer}(x) = I_0 \cdot \left[\cosh\left(\frac{x}{\lambda}\right) - \coth\left(\frac{L_p}{\lambda}\right) \cdot \sinh\left(\frac{x}{\lambda}\right) \right] \qquad (6)$$

where λ is the characteristic length given by sqrt($r_{diff(drift)}/r_{sheet(buffer)}$). By substituting eq.(6) in the first part of the eq.(1), the current density through the drift region can be obtained as follows,

$$J_{drift}(x) = J_{1D} \cdot \frac{L_p}{\lambda} \cdot \left[-\sinh\left(\frac{x}{\lambda}\right) + \coth\left(\frac{L_p}{\lambda}\right) \cdot \cosh\left(\frac{x}{\lambda}\right) \right] \qquad (7)$$

where J_{1D} is the one dimensional current density, i.e. the virtual current density if the current was flowing homogeneously ($J_{1D}=I_0/(b \cdot L_p)$). From eq.(7), the voltage across the device can be calculated at position x. The maximum potential difference $\Delta\varphi_{max}$ (this is equal to V_J) along the buffer from 0 to L_p is

$$\Delta\varphi_{max} = V_J = r_{diff(drift)} \cdot \left(J_{drift}(0) - J_{drift}(L_p) \right) \qquad (8)$$

where V_J is the junction voltage, across the junction between p^+-anode and n-buffer, which is necessary for the carrier injection and hence the snapback

$$V_J = \Delta\varphi_{max} = r_{diff(drift)} \cdot J_{1D} \cdot \frac{L_p}{\lambda} \cdot \tanh\left(\frac{1}{2} \cdot \frac{L_p}{\lambda}\right) \qquad (9)$$

So far we have considered that the width of the n^+-short region, L_n is negligibly small compared to the width of the p^+-anode region, L_p. For comparable width of the n^+-short region, L_n the maximum potential difference along the buffer is

$$V_J = r_{diff(drift)} \cdot J_{av} \cdot \frac{L_p + L_n}{L_p + L_n \cdot \frac{L_p}{\lambda} \cdot \coth\left(\frac{L_p}{\lambda}\right)} \cdot \frac{L_p}{\lambda} \cdot \tanh\left(\frac{1}{2} \cdot \frac{L_p}{\lambda}\right)$$

where $J_{av} = \dfrac{J_{1D} \cdot L_p + J_{drift}(0) \cdot L_n}{L_p + L_n}$ is the average current density, assuming a mean value of J_{1D} flowing in the area of the p^+-anode region and $J_{drift}(0)$ flowing in the area of the n^+-short region. For small L_p/λ values (which is usually the case for reasonable design of RC-IGBTs), the above equation can be simplified as follows,

$$V_J = \Delta\varphi_{max} = \frac{1}{2} \cdot r_{sheet(buffer)} \cdot J_{av} \cdot L_p^2 \qquad (11)$$

At a given temperature (V_J, $r_{sheet(buffer)}$ and $r_{diff(drift)}$ are temperature dependent) and for a given voltage class ($r_{diff(drift)}$) and technology ($r_{sheet(buffer)}$), the current density at which the snapback occurs is mainly dependent on the width of the p^+-anode L_p. The snapback phenomenon can be more pronounced at lower temperatures as the V_J increases and the resistance decreases with decrease in temperature.

The eq.(11) can also be used to find out the onset current for the initial snapback in the blocking state of the RC-IGBT. However, the sheet resistance of the buffer $r_{sheet(buffer)}$ is higher in the blocking state compared to the on-state (during blocking, the thickness of the buffer layer becomes smaller because of the penetration of the depletion layer into the n-buffer layer). Therefore, in the blocking state, the snapback occurs at even lower currents when compared to the on-state mode.

SIMULATION RESULTS

In this section, we present the simulation results of the 3.3 kV SPT type RC-IGBT in transistor on-state mode and blocking state for different widths (L_p and L_n) of the anode shorts.

Transistor On-State Mode

The structure of the RC-IGBT as shown in Fig. 4 is used in the simulations. Here the simulations are performed for different widths of the anode shorts, by varying the widths of L_p and L_n. Fig. 6 illustrates the on-state characteristics of the RC-IGBT in transistor mode at 400 K. In this RC-IGBT, the width of the p^+-anode, L_p is 500 µm and the width of the n^+-short, L_n is 60 µm. In this case, the snapback occurs at the current density of about 35 mA/cm^2. The calculated and simulated current density values are listed in Table 1 for corresponding maximum junction potentials (V_J) at different points which are shown in Fig. 6. It can be seen from the Table 1 that the current density values from the simulation are in good agreement with the calculated current density values up to the snapback point.

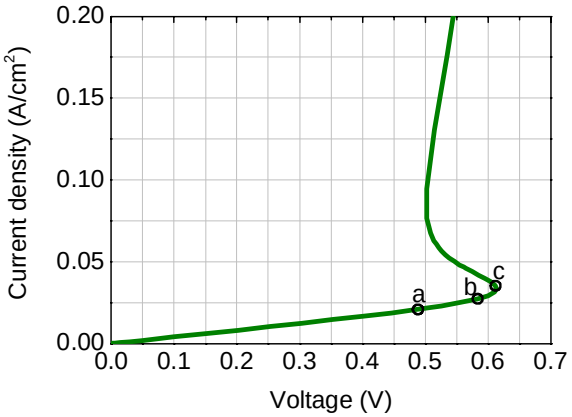


Figure 6: Simulated on-state characteristics of the RC-IGBT in transistor mode at 400 K. The widths of L_p and L_n are 500 µm and 60 µm respectively.

Point	From Simulation		Calculated J_{av} (mA/cm^2)
	V_J (V)	J_{av} (mA/cm^2)	
a	0.139	20.94	21.37
b	0.174	27.24	26.84
c	0.210	35.64	32.29

Table 1: Comparison of simulated and calculated current density values for corresponding junction potentials at different points.

Fig. 7 illustrates the on-state characteristics of the RC-IGBT for different widths of the anode shorts. Here the width of L_n is fixed to 60 µm and the width of L_p is varied (the different L_p values are 260, 340, 500, 900 and 1620 µm). The on-state characteristics of a "pure" IGBT (without anode shorts) are also plotted in Fig. 7 for the comparison. It can be seen from Fig. 7 that the onset of the snapback indeed depends on the width of L_p. If the width of L_p is small, the snapback occurs at higher voltages and at higher currents.

Fig. 8 also illustrates the on-state characteristics of the RC-IGBT for different widths of the anode shorts but here the width of L_p is fixed to 500 µm and the width of L_n is varied (the different L_n values are 60, 140, 460 and 620 µm). It can be seen from Fig. 8 that the onset of snapback occurs nearly at the same voltage and current for all the cases. Therefore, it can be concluded from Fig. 7 and Fig. 8 that the onset of snapback is mainly determined by the width of L_p.

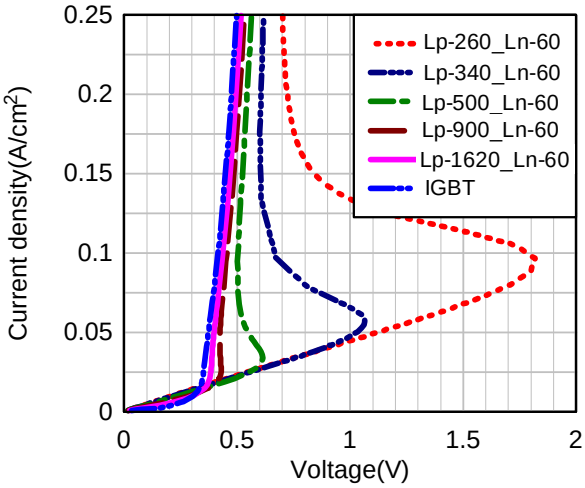


Figure 7: Simulated on-state characteristics of the RC-IGBT in transistor mode at 400 K for different widths of the anode shorts. Here the width of L_n is fixed to 60 µm and the width of L_p is varied.

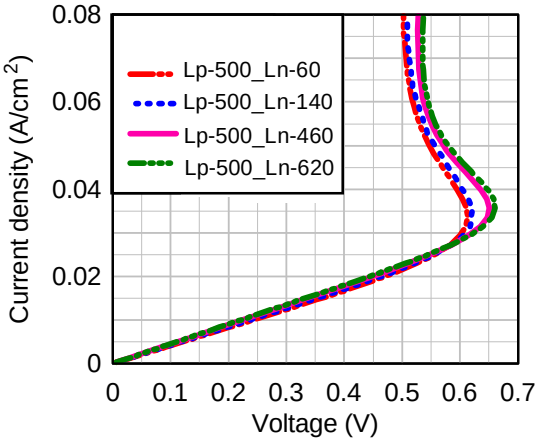
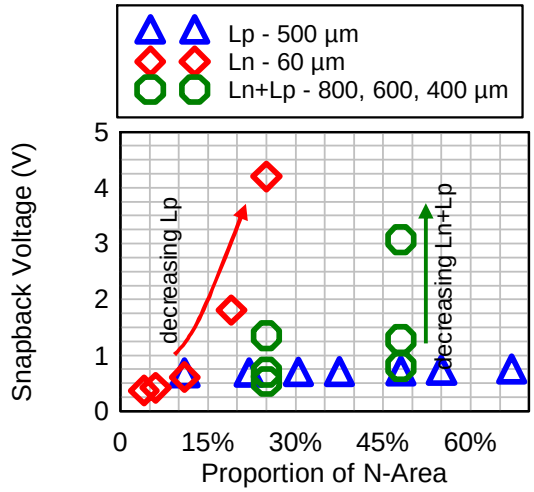


Figure 8: Simulated on-state characteristics of the RC-IGBT in transistor mode at 400 K for different widths of the anode shorts. Here the width of L_p is fixed to 500 µm and the width of L_n is varied.

The snapback voltage of the RC-IGBT for different widths of the anode shorts is plotted against the proportion of the n^+-short region, L_n as shown in Fig. 9 at 400 K. In Fig. 9, for the case of L_p 500 µm (here the width of L_p is

fixed to 500 µm and the width of L_n is increased from 60 to 1020 µm), the snapback voltage is nearly constant and does not depend on the width of L_n. In Fig. 9, for the case of L_n 60 µm (here the width of L_n is fixed to 60 µm and the width of L_p is decreased from 1620 to 180 µm), the snapback voltage increases with the decrease of the width of the L_p. In Fig. 9, for the case of L_n+L_p 800, 600, 400 µm (here both L_n and L_p are varied but proportion of L_n is constant for all the widths), the snapback voltage increases with the decrease of the width of L_n+L_p (for the same proportion of L_n, the width of L_p decreases with the decrease of the width of L_n+L_p) and does not depend on the proportion of L_n. It has been found out that the onset of the snapback is mainly determined by the width of L_p and is dependent neither on the width of L_n nor the proportion of L_n.



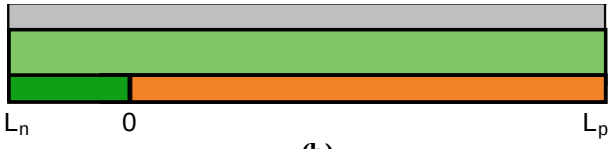
(a)

For the description of the legend, only anode side of the RC-IGBT has been shown here. For the case of

L_p-500 µm: *Here the width of L_p is fixed to 500 µm and the width of L_n is varied*

L_n-60 µm: *Here the width of L_n is fixed to 60 µm and the width of L_p is varied*

L_n+L_p-800, 600, 400 µm: *Here the widths of both L_n and L_p are varied but proportion of L_n is maintained constant (25% and 47%)*



(b)

Figure 9: (a) Simulated snapback voltage versus proportion of N-area (n^+-short region, L_n) at 400 K (b) Description of the legend of Fig. 9(a)

The on-state losses of the RC-IGBT for different widths of the anode shorts are plotted against the proportion of the n^+-short region, L_n as shown in Fig. 10 at 400 K.

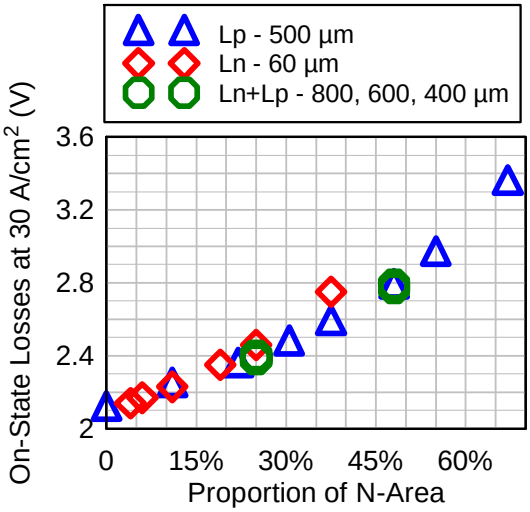


Figure 10: Simulated on-state losses versus proportion of N-area (n^+-short region, L_n) at 400 K

It can be seen from Fig. 10 that the on-state losses increase with the proportion of L_n. In Fig. 10, for the case of L_n+L_p 800, 600, 400 µm, the on-state losses are nearly the same for all the three cases for the same proportion of L_n, though they have different widths of L_n and L_p. It has been found out that the on-state losses are mainly dependent on the proportion of the n^+-short region, L_n.

Temperature Dependency of the Snapback. In this section we have investigated the snapback phenomenon of the RC-IGBT at room temperature, 300 K and compared the simulation results to that of the RC-IGBT at 400 K.

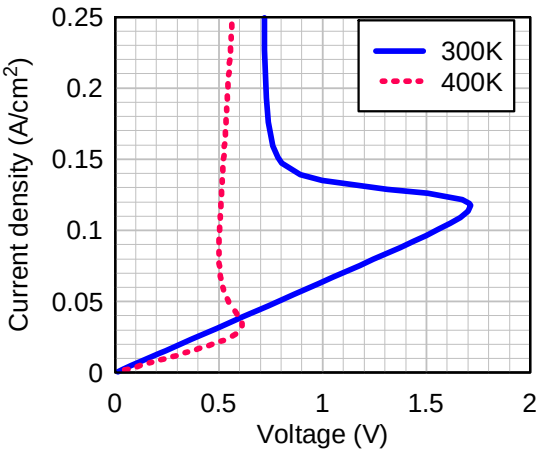


Figure 11: The comparison of the simulated on-state characteristics of the RC-IGBT at different temperatures.

Fig. 11 illustrates the comparison of the on-state characteristics of the RC-IGBT at different temperatures. In this RC-IGBT, the width of the p^+-anode, L_p is 500 µm and the width of the n^+-short, L_n is 60 µm. As explained in the analytical model section, the snapback phenomenon is more pronounced at lower temperatures. The reason being that the junction voltage V_J increases with decrease in temperature and the resistance decreases (as the mobility of the electrons increases) with decrease in temperature and this can be clearly seen in Fig. 11 from the slope of the current before snapback.

Snapback Phenomenon in Different Voltage class Devices. In this section we have investigated the snapback phenomenon in 6.5 kV RC-IGBT and compared the simulation results to that of the 3.5 kV RC-IGBT at room temperature, 300 K.

Fig. 12 illustrates the comparison of the on-state characteristics of 3.3 kV and 6.5 kV RC-IGBTs at room temperature. We have used same anode shorts (L_p and L_n are 500 µm and 60 µm respectively) and also used the same technology (the buffer and anode profiles) for both the devices but the drift region resistance is different (the resistivity and thickness of the drift regions are different).

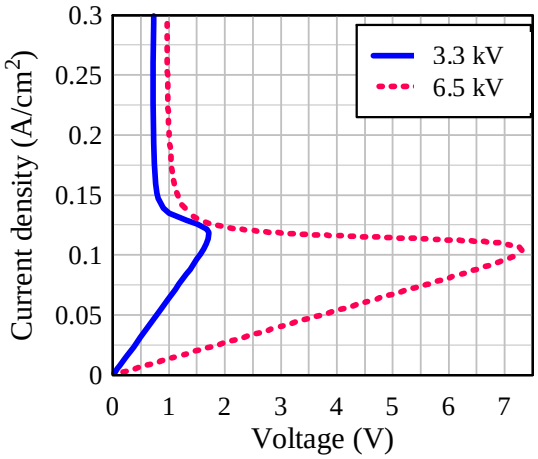


Figure 12: The comparison of the simulated on-state characteristics of 3.3 kV and 6.5 kV RC-IGBTs at room temperature.

It can be seen from Fig. 12 that the current density for the onset of snapback is nearly the same in both the devices due to the existence of the same doping profiles of p^+-anode and n-buffer (and also the width of the p^+-anode is same). Therefore, they start injecting carriers at the same junction potential, V_J and cause same current density for the onset of snapback. However, the voltage at which the snapback occurs is different in both the devices. This is simply due to the differential resistance of the drift region, which is different in both the devices. The total on-state voltage drop (V_{total}) across the device can be expressed as

$$V_{total} = V_{drift} + V_J$$

where V_{drift} is the voltage drop across the drift region. For the same current density, the voltage drop across the drift region is high as the differential resistance of the drift region is high in 6.5 kV device when compared to that of the 3.5 kV device. Therefore, the snapback occurs at higher voltages in 6.5 kV, though the snapback current density is the same in both the devices.

RC-IGBT in Blocking State

In this section, we present the simulation results of the RC-IGBT in blocking state and compare the results to that of the MOSFET and IGBT at 400 K.

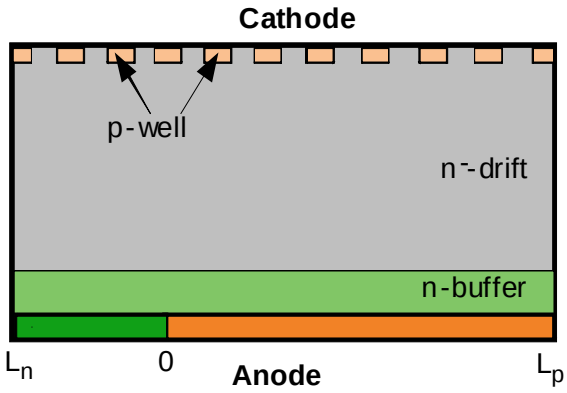


Figure 13: The structure of the RC-IGBT which is used in the blocking simulations.

To simulate the blocking characteristics of the RC-IGBT, the n-source cells at the front side of the device (shown in Fig. 4) have to be replaced by the p-source cells as shown in Fig. 13. The blocking characteristics of the RC-IGBT for different widths of the anode shorts (here the width of L_n is fixed and the width of L_p is varied) have been investigated and the results compared with that of the MOSFET and IGBT at 400 K as shown in Fig. 14. The leakage current in the RC-IGBT is nearly the same as in MOSFET due to the anode shorts, which strongly reduce the p-n-p gain of the transistor. As shown in Fig. 14, the leakage current is very low in RC-IGBTs when compared to IGBT but the RC-IGBTs also show a malicious snapback behaviour in the blocking. The snapback phenomenon is the same as it is explained in the on-state but here the electrons which are generated in the depletion layer flow to the n^+-short via the buffer region. As the leakage current increases, the lateral electron current flow through the buffer produces an increasing voltage drop (junction voltage V_J) across the junction between p^+-anode and n-buffer. The p^+-anode starts injecting

carriers (holes) into the n$^-$-drift region at/around position L_p when there is a sufficient voltage drop and causes a current localization in the device, which leads to a snapback in voltage.

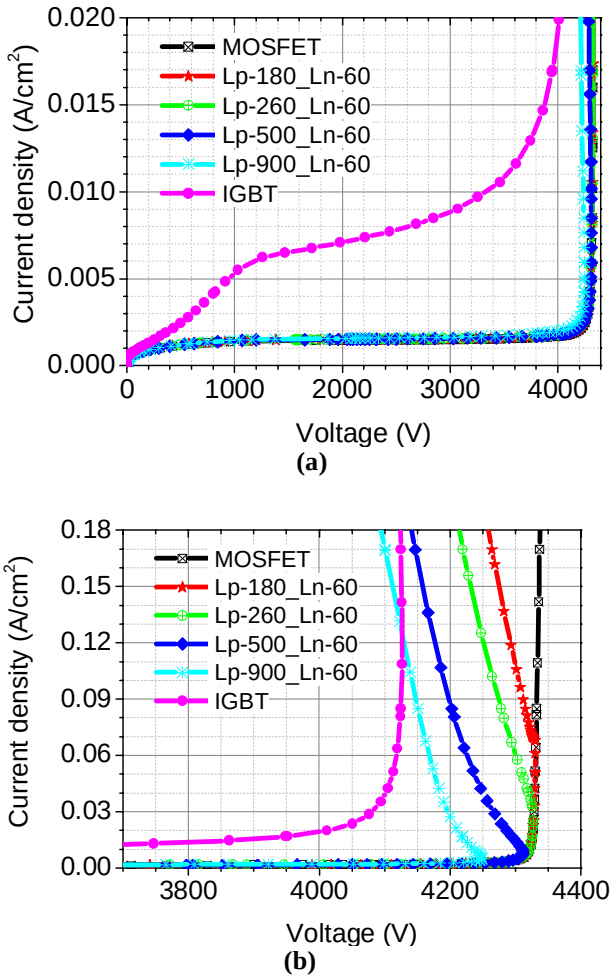


Figure 14: (a) The comparison of the simulated blocking characteristics of the MOSFET, IGBT and RC-IGBT at 400 K (b) Zoomed version of the figure at higher voltages and currents.

MESURMENT RESULTS

In this section, we present the measurement results of the 3.3 kV RC-IGBT for different widths of the anode shorts at different temperatures and compare the results with that of the simulation results.

Fig. 15 illustrates the comparison of the measurement and simulation results of the 3.3 kV IGBT and RC-IGBT in transistor on-state mode at 400 K. Here the solid lines represent the measurement results and dotted lines represent the simulation results.

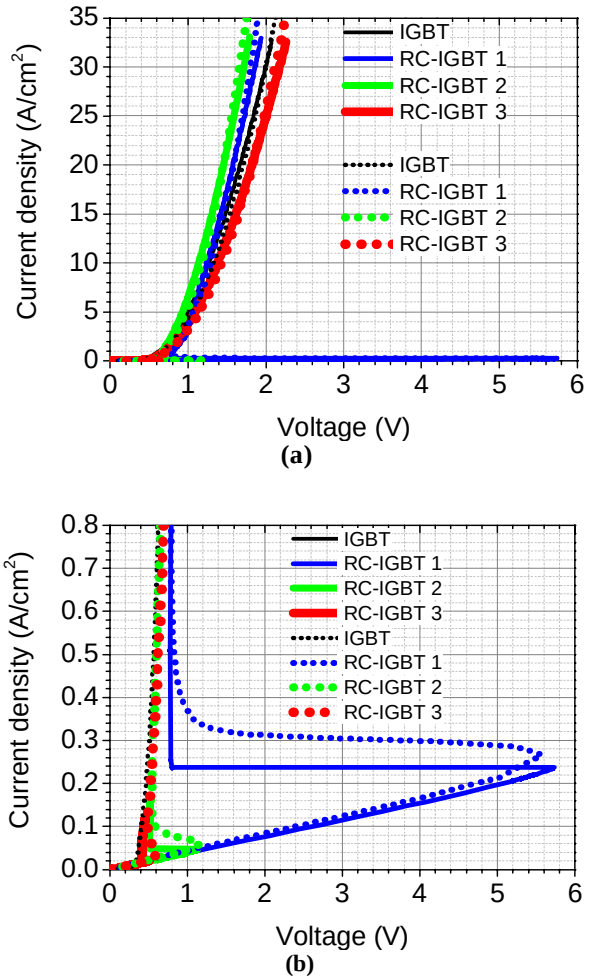


Figure 15: (a) The comparison of the measurement and simulation results of the IGBT and RC-IGBT in transistor on-state mode at 400 K (b) Zoomed version of the figure at low current densities. Here the solid lines represent the measurement results and dotted lines represent the simulation results.

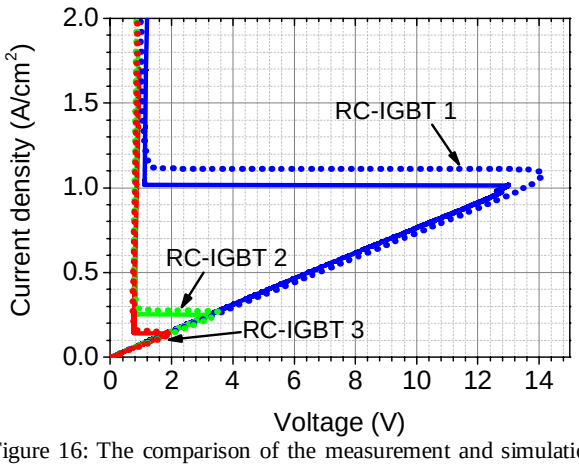


Figure 16: The comparison of the measurement and simulation results of RC-IGBT in transistor on-state mode at 300 K. Here solid lines represent the measurement results and dotted lines represent the simulation results.

The widths of L_p and L_n in RC-IGBT 1 are 200 µm and 50 µm, in RC-IGBT 2 and RC-IGBT 3 are 400 µm and 100 µm respectively. However, the RC-IGBT 3 has a weaker buffer (high sheet resistance of the buffer) compared to that of the RC-IGBT 2. It can be seen from Fig. 15 and Fig. 16 that the simulation results nearly match to the measurement results for all the cases. It can also be seen from the measurement results that for a given technology (RC-IGBT 1 and RC-IGBT 2), the onset of snapback is mainly determined by the width of the p^+-anode, L_p. In case of RC-IGBT 3, the snapback occurs at lower current density as the sheet resistance of the buffer is high when compared to that of the RC-IGBT 2. It can also be seen from the measurement results that the snapback is more pronounced at lower temperatures as shown in Fig. 16.

CONCLUSIONS

An analytical model has been proposed to describe the onset current for the initial snapback in the transistor on-state mode and in the blocking state of Reverse Conducting (RC)-IGBTs. The analytical model is in good agreement with simulation results as well as with the measurement results. From the analytical model as well as simulation and measurement results, we have found that for a given voltage class and technology (anode and buffer profiles), the p^+-anode width is the only remaining design degree of freedom which determines the initial snapback. The adjustment of the on-state losses can then be done with the proportion of the n^+-short region, which is not affecting the snapback.

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