Module and Application Description

Application

The input module for counter states is used to scan the states of one or two counters installed in the process.

It is possible to scan either one 32 bit counter or two 16 bit counters.

The counter states may be available in the Aiken code, BCD code or binary code.

The module is available in two versions which differ only in terms of hardware.

The software used is the same for both module versions.

81 EZ10-E/R1010 suitable for connection of electronic pulse counters with a counter frequency f ≤ 100 Hz

81 EZ10-E/R1210 suitable for the connection of contact pulse counters with a counter frequency f ≤ 20 Hz

Features

The module can be plugged into every multi-purpose processing station of the PROCONTROL bus system.

It requires 2 divisions and four successive addresses on the IO-bus.

It incorporates a standard interface SEA to the IO-bus.

The counter states received as binary coded information are transferred in unchanged form as data telegrams to the IO-bus.

The counter states received as Aiken and BCD coded information are converted module internally into binary coded information with twos complement representation and transferred as data telegrams to the IO-bus.

The counter states can be taken over in either of two ways which can be set by means of a configuration switch.

The voltage for the counter can be supplied by the module.
Description

Basically, the module consists of three functional blocks:

- Acquisition of the counter inputs and conversion of the signals available in parallel form into serial form.

- Conditioning and checking of the incoming signals as well as sequential control of the acquisition function by means of a microprocessor.

- Bus adaptation with output of the respective counter state to the IO-bus after the module has been called.

INPUT - OUTPUT ON PROCESS SIDE

The module is suitable for scanning 2 counters in 16 bit mode or 1 counter in 32 bit mode.

- In 16 bit mode, the maximum counter word length for binary-coded counters is 14 bits, and for Aiken- or BCD-coded counters it is 16 bits (4 decades).

- In 32 bit mode, the maximum counter word length for binary-coded counters is 30 bits, and for Aiken- or EIC-coded counters it is 32 bits (6 decades).

Each of the two counters has its own control lines.

The input module is not suitable for presetting or resetting counters.

The choice of the module version is dependent on the design of the connected counters, i.e. whether they are provided with electronic or mechanical outputs.

The two versions differ by the fact that the process-side input circuits are differently rated.

The negative bias voltage UV can be supplied to the module either through the standard interface SEA to the IO-bus, incorporated in X1, or through the process connector.

- If this negative bias voltage UV is supplied through the standard interface SEA, the voltage is fed via a module-internal jumper to contact b02 of the process connector X3.

In addition to this, a connection must be made on the wiring side between contact b02 of process connector X3 and contact b02 of process connector X2.

- If this negative bias voltage UV is supplied through the process connector, the module-internal jumper between the standard interface and the process connector must be removed.

The connection between contacts b02 of connectors X2 and X3 is retained.

The counters installed in the process can also be connected to the power supply of the module.

The power supply for the counters is protected by a fuse US1 provided on the module front. This fuse is monitored, its state being indicated by light-emitting diode ST1.
To ensure that a counter value is correctly taken over, certain minimum requirements as regards pulse duration and pulse-off times, bounce times as well as edge rise and fall times of the counter signals must be satisfied.

Basically, the following input voltage-time curves are required, irrespective of the way the counter state is taken over.

Voltage-time curves at module inputs E1.10 to E2.15 for counters with electronic outputs (version R1010).

**Bit 0 (E1.0 or E2.0)**

Signal values version R1010
- Pulse duration $t_i$: $\geq 9$ ms
- Pulse-off time $t_p$: $\geq 9$ ms
- Delay time $t_v$: $\leq 0.2$ ms
- Signal rise time $t_{\text{an}}$: $\leq 1$ ms
- Signal fall time $t_{\text{af}}$: $\leq 1$ ms
- Permissible frequency for bit 0: $\leq 50$ Hz
- Max. counter frequency of preceding counter: $\leq 20$ Hz

**Bit 1**

Signal values version R1210
- Pulse duration $t_i$: $\geq 40$ ms
- Pulse-off time $t_p$: $\geq 40$ ms
- Delay time $t_v$: $\leq 1$ ms
- Bounce time $t_{\text{prell}}$: $\leq 10$ ms
- Permissible frequency for bit 0: $\leq 10$ Hz

WIRING OF UNUSED FUNCTION UNITS
It is not necessary to wire unused function units.
Open data and sign inputs are detected as logic "0" by the module.
Signal processing

The counter signals arriving from the process are conditioned by the module-internal processor. Therefore the counter state can be taken over by the module in two different ways.

- Counter state take-over by comparison (take-over mode 1)

- Counter state take-over by request and acknowledgment signal (take-over mode 2)

The take-over mode can be set by means of configuration switches; counter state take-over is effected as follows:

- Counter state take-over by comparison (take-over mode 1).

The counter state is scanned continuously and taken over if the counter value between two successive scans has not changed by more than 2.

If there is a difference between the counter states including sign, a new scan is performed.

The new counter state is compared with the previously scanned counter state.

This process is continued until plausibility is reached.

If the number of unsuccessful counter state scans and comparisons exceeds 10, a disturbance annunciation 391 is output to the 16-bus.

- Counter state take-over by request and acknowledgment signal (take-over mode 2)

The module transfers a request signal to the counter to be read out via output DA (data request), and waits for the release signal from the counter via line DG (data valid).

During the time interval the data and sign are taken over from the counter, the data and sign are scanned twice in succession and checked for plausibility.

Plausibility is assumed to exist when the counter state does not change between the two scans, and when it is valid at the time the scanning operations are performed.

A new scanning operation is not performed by the module until the counter cancels the "Data valid" signal.

As with the counter signals, minimum and maximum time periods have to be observed for the control signals "Data request" and "Data valid".

Input voltage-time curves for control signals of module version R1UL0:

Data request DA by module 81 EZ10

Data and sign from the counter, present at module 81 EZ10

"Data valid" signal DG from the counter, present at module 81 EZ10

Take over of data and sign by 81 EZ10

Data request time \( t_{DA} \): > 100 ms
Pulse-off time \( t_{p} \): > 200 ms
"Data valid" time \( t_{DG} \): > 15 ms
Signal rise time \( t_{an} \): < 1 ms
Signal fall time \( t_{ab} \): < 1 ms
Take-over time delay \( t_{v} \): < 1 ms
Input voltage-time curves for control signals of module version R1210:

Data request DA by module 81 EZ10

Data and sign from the counter, present at module 81 EZ10

"Data valid" signal DG from the counter, present at module 81 EZ10

Take over of data and sign by 81 EZ10

<table>
<thead>
<tr>
<th>Data request time</th>
<th>$t_{DA}$:</th>
<th>$&gt;$ 100 ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse-off time</td>
<td>$t_{p}$:</td>
<td>$&gt;$ 200 ms</td>
</tr>
<tr>
<td>&quot;Data valid&quot; time</td>
<td>$t_{DG}$:</td>
<td>$&gt;$ 30 ms</td>
</tr>
<tr>
<td>Bounce time</td>
<td>$t_{prell}$:</td>
<td>$\leq$ 10 ms</td>
</tr>
<tr>
<td>Take-over delay time</td>
<td>$t_{V}$:</td>
<td>$\leq$ 1 ms</td>
</tr>
</tbody>
</table>
Formations of telegrams

For the transfer of the binary data in the data telegrams, binary representation in the two's complement code has been chosen.

The module forms two data and two specification telegrams and transfers these to the 10-bus, after having been called, during four successive transfer cycles.

The data content of the data telegrams transferred to the 10-bus differs, depending on the word width of the connected counters.

For the 32 bit mode, a data telegram is not sufficient, with respect to the data format, for the transfer of the counter state. Therefore, different transfer sequences have been chosen for the two operating modes.

TRANSFER SEQUENCE 16 BIT MODE

After the first call by the bus control module, the module transfers the data telegram of the first function unit to the 10-bus during the subsequent transfer cycle (specification bit of the address telegram = logic 0).

The specification telegram of the first function unit is transferred under the second address (specification bit of the address telegram = logic 1).

The data and specification telegrams of the second function unit are transferred under the next two addresses (see connection diagram).

TRANSFER SEQUENCE 32 BIT MODE

After the first call by the bus control module, the module transfers the higher-order part of the counter word to the 10-bus during the subsequent transfer cycle (specification bit of the address telegram = logic 1).

The specification telegram follows under the second address (specification bit of the address telegram = logic 1).

The lower-order part of the counter word and another specification telegram are transferred under the third and fourth addresses.
DATA TELEGRAMS 32 BIT MODE

The data telegrams transferred by the module are as follows:

32 bit mode 2 data telegrams

31 30 29... 17 16 15 14... 2 1 0

Specifying telegram format

Sign
0 = positive
1 = negative

higher-order part of counter word transferred under FL1

lower-order part of counter word transferred under FL2

Counter word 30 bit

SPECIFICATION TELEGRAM

The module transfers a specification telegram to the 10-bus when the specification bit of the address telegram is set to logic 1.

The specification telegram specifies (bits 11...15) which type of transmitter has been set by the configuration switches.

The specification telegrams are as follows:

16 bit mode:

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

32 bit mode:

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0

The specification telegram specifies, in the section for the type of transmitter, whether counters with 16 bit word width or 32 bit word width are connected.

Bits 6 to 10 of the specification telegram are always set to logic "0".
Data communication with the module

The module is provided on its front with 3 hex. code address switches, which serve to set the module starting address.

When the module is called by its starting address defined by the hex. code address switches it transfers its data and specification telegrams to the 10-bus during the next four transfer cycles.

When the module is called by an address telegram with its module starting address, it transfers the data telegram of its first function unit during the next transfer cycle.

The 3 subsequent addresses are recognized module-internally and output to the 10-bus in the following transfer cycles.

FORMATION OF ADDRESS

The bus control module transfers address telegrams with 16 bit length to call the individual modules connected to the 10-bus.

In the module every incoming address telegram is compared with its own module starting address.

This comparison takes place in parallel mode.

Address comparison takes place by means of the following bit positions in connection with the hex. code address switches.

![Diagram](image)

After bit positions 2 to 11 have been evaluated (on the basis of the wired bits of the hex. code address switches S1, S2 and S3) and the transferred address agrees with the module starting address, evaluation of the total address telegram is made.

By this complete address telegram the data telegram of the respective function unit is triggered and then transferred.

The complete address telegram has the following format:

```
  15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 P
```

- **P** Function unit address
- ** specifications (0 or 1)**
- **wire and bits of the module starting address**
- **Parity bit** always 000

When the addresses are the same, a check for odd parity and for assignment of 0 to bit positions 13 to 15 is performed.

The memories of the individual function units are addressed directly via bit position 1.

The 0 address bit is the so called specification bit.

Depending on the state of the specification bit, a specification or data telegram is transferred.

- 0 = data telegram
- 1 = specification telegram

Annunciation functions

Disturbances in the module, the process peripherals and in the communication with the 10-bus are detected and signalled by the module.

Disturbances can be signalled by the module in the following three ways:

- Visual disturbance annunciation on the module by the light-emitting diodes S3 and S1 visible on the module front.
- Annunciation via the bus line SME of the 10-bus.
- Annunciation by setting the disturbance bit SB in the data telegram of the corresponding function unit.
ANNUNCIATIONS ON THE MODULE

Two red light-emitting diodes are provided on the module front.

The red light-emitting diode ST1 is connected with the bus line SME. It emits a steady light signal when a disturbance annunciation is transferred via bus line SME.

Light-emitting diode ST1 emits a steady light when fuse US1 is blown.

ANNUNCIATION FUNCTIONS TO THE IG-BUS

Depending on the disturbance, the module sets a disturbance bit SB in the data telegram and/or outputs a disturbance annunciation signal SME to the BUS. In addition, the disturbance annunciation SME is visually signalled by light-emitting diode ST on the module front.

A disturbance annunciation is output in the following cases:

- If the module is not addressed by a valid address telegram within 7 s.
  Only disturbance annunciation signal SME is set. If the module is called again by the bus control module, SME is reset after 200 ms.

- If the monitor of the bus drivers responds as a result of a short circuit.
  Listurbance annunciation signal SME and the disturbance bit SB are set as long as disturbances are present.

  After the disturbances have been removed, the disturbance bit is set immediately while the disturbance annunciation signal is reset after 200 ms.

- If the fuse for the power supply of the counters fails.
  The disturbance annunciation signal SME and the disturbance bit SB are set as long as disturbances are present.

  After the disturbances have been removed, the disturbance bit is reset immediately while the disturbance annunciation signal is reset after 200 ms.

- If the watch dog of the sequential control responds (i.e. the sequential control does no longer work according to program).

  The disturbance annunciation signal SME and the disturbance bit SB are set. When the watch dog is set back, the disturbance bit is reset immediately, while the disturbance annunciation signal is reset after 200 ms.

- If the watch dog of the sequential control is disturbed.

  The disturbance annunciation signal SME is set. When the watch dog returns to its normal working condition, the disturbance annunciation signal is reset after 200 ms.

- If, during counter state take-over, the plausibility check has scanned and compared the counter states more often than 10 times without any success.

  The disturbance annunciation signal SME and the disturbance bit SB are set. The disturbance bit is reset after reception of the first plausible counter state, while the disturbance annunciation signal is reset after 200 ms.

- If, during counter state take-over by "Data request", the counter fails to transfer "Data valid" within 1 second after the data request, or if the module has canceled the data request and the counter continues to transfer "Data valid" for more than 1 second, or if no plausible counter states were found within 2 data request cycles.

  The disturbance annunciation signal SME and the disturbance bit SB are set. The disturbance bit is reset immediately whenever a plausible counter state is taken over. In addition, the disturbance bit is reset immediately when the counters signal "Data valid."
Setting of the module

The settings on the module are performed using address switches S1, S2 and S3 as well as configuration switches S4:1 to S4:8.

SETTING OF ADDRESS

The module starting address is to be set by means of address switches S1, S2 and S3.

The address is set with the module withdrawn.

Possible settings of the hex. code address switches:

<table>
<thead>
<tr>
<th>1.Addr. switch S1</th>
<th>2.Addr. switch S2</th>
<th>3.Addr. switch S3</th>
</tr>
</thead>
<tbody>
<tr>
<td>adjustable</td>
<td>adjustable</td>
<td>0</td>
</tr>
<tr>
<td>O - F</td>
<td>U - F</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C</td>
</tr>
</tbody>
</table>

Other settings are not accepted by the module. In this case, the module outputs an disturbance announciation signal SME after 7 s and signals a disturbance via light-emitting diode ST.

The address set on the address switches is the address of the first function unit (module starting address) of the module. It can be read on the module front.

When the module is used in connection with a bus coupling module 88 QT02, value 1 must be set on address switch S1.

By setting the first address switch to "1", the bus coupling module 88 QT02 is notified that specification telegrams are transferred by the module.

MEANING OF THE CONFIGURATION SWITCHES

S4
ON

Counter state take-over
Code conversion
Operating mode
Type of transmitter
Setting optional

The setting of the individual switch contacts is explained in the description of the respective function.

The take-over mode is set on switch S4:1:

Take-over mode 1:

<table>
<thead>
<tr>
<th>S4</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>:1</td>
<td>:2</td>
</tr>
<tr>
<td>:3</td>
<td>:4</td>
</tr>
<tr>
<td>:5</td>
<td>:6</td>
</tr>
<tr>
<td>:7</td>
<td>:8</td>
</tr>
</tbody>
</table>

Take-over mode 2:

<table>
<thead>
<tr>
<th>S4</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>:1</td>
<td>:2</td>
</tr>
<tr>
<td>:3</td>
<td>:4</td>
</tr>
<tr>
<td>:5</td>
<td>:6</td>
</tr>
<tr>
<td>:7</td>
<td>:8</td>
</tr>
</tbody>
</table>
OPERATING MODES

The module is suitable for taking over the counter states of two 16-bit counters (representation: +/-9,999) or the counter state of one 32-bit counter (representation +/-99,999,999).

The control lines for the counters are provided twice on the module, so that every 16-bit counter has its own control lines.

When a 32-bit counter is connected, only the control lines of the first function unit will be used.

It is possible to connect counters with or without sign output.

The operating mode can be set on configuration switches S4:4 and S4:5.

Operating mode

| 32 bits | S4 | ON
|---------|----|---
|         | :1 | :2 |
|         | :3 | :4 |
|         | :5 | :6 |
|         | :7 | :8 |

<table>
<thead>
<tr>
<th>2 times</th>
<th>S4</th>
</tr>
</thead>
</table>
| 16 bits | ON

1 time 16 bits
(Only function unit 1 connected)

| S4 | ON
|----|---
| :1 | :2 |
| :3 | :4 |
| :5 | :6 |
| :7 | :8 |

1 time 16 bits
(Only function unit 2 connected)

| S4 | ON
|----|---
| :1 | :2 |
| :3 | :4 |
| :5 | :6 |
| :7 | :8 |

VZ = sign
positive sign ▲ logic 0
negative sign ▼ logic 1

If no sign inputs are connected or used, the transferred value is considered to be positive.

TYPE OF TRANSMITTER

The type of transmitter must be set for every module version. The two types of transmitters differ in the module-internal process cycle by the fact that they have different scanning and delay times, depending on the input voltage time curves of version R1010 and version R1210.

If the type of transmitter is not set as specified, the module may no longer be able to take over plausible values, and disturbance annunciation is initiated.

The type of transmitter is set via contact S4:6 of the configuration switch:

Counter with electronic outputs R1010:

| S4 | ON
|----|---
| :1 | :2 |
| :3 | :4 |
| :5 | :6 |
| :7 | :8 |

Counter with contact outputs R1210:

| S4 | ON
|----|---
| :1 | :2 |
| :3 | :4 |
| :5 | :6 |
| :7 | :8 |
CODE CONVERSION

The module can process BCD-coded, Aiken-coded and binary-coded counter outputs.

Within the module, the counter states are converted from BCD-coded information to binary-coded information (twos complement representation with sign) and from Aiken-coded information to binary-coded information (twos complement representation with sign).

If the counter states to be taken over are already in the binary code, no code conversion will take place.

The counter states are transferred to the IO-bus in twos complement representation.

The code conversion to be performed is set by configuration switches S4:2 and S4:3:

No code conversion

<table>
<thead>
<tr>
<th>S4</th>
<th>:1 :2 :3 :4 :5 :6 :7 :8</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td></td>
</tr>
</tbody>
</table>

No code conversion

<table>
<thead>
<tr>
<th>S4</th>
<th>:1 :2 :3 :4 :5 :6 :7 :8</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td></td>
</tr>
</tbody>
</table>

BCD code to binary code

<table>
<thead>
<tr>
<th>S4</th>
<th>:1 :2 :3 :4 :5 :6 :7 :8</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td></td>
</tr>
</tbody>
</table>

Aiken code to binary code

<table>
<thead>
<tr>
<th>S4</th>
<th>:1 :2 :3 :4 :5 :6 :7 :8</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td></td>
</tr>
</tbody>
</table>
Functional diagrams

MODULE VERSION 81 EZ10-E/R1010

Terminal designations:
The module consists of two printed circuit boards (see "Mechanical design"). Printed circuit board (1) is equipped with connector X2 for the counter inputs of function unit 2. Printed circuit board (2) is equipped with connectors X1 and X3. Connector X1 incorporates the IO-bus interface SEA and the operating voltage supply for the module, connector X3 incorporates the counter inputs of function unit 1.

Module version R1010 differs from module version R1210 by the additional negative bias voltage for the counter contacts.
Module version 81 E210-E/R1210

Terminal designations:
The module consists of two printed circuit boards (see "Mechanical design"). Printed circuit board (1) incorporates connector X2 for the counter inputs of function unit 2. Printed circuit board (2) incorporates connectors X1 and X3. Connector X1 incorporates the I0-bus interface SEA and the operating voltage supply for the module, connector X3 incorporates the counter inputs of function unit 1.

* If necessary, connector contacts b02 (negative bias voltage UV) of connectors X2 and X3 must be interconnected externally.
Connection diagrams

Transfer sequence 16-bit mode

Operating mode: binary code

**For module version 81 EZ10/R1010 no bias voltage UV is required**

**Allocation or non-allocation of DA and DG, depending on the take-over mode**
Transfer sequence 16-bit mode

Operating mode: code conversion

Counter 1

Aiken or BCD code

Decade 1...4

Counter 2

Aiken or BCD code

Decade 1...4

Code conversion: Aiken or BCD code to binary code with two's complement notation

IO-BUS ADDRESS

DATA, SPEC. TELEGRAMS

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 0 0 0 P X X X X X X X X X X X X X X 0 0

VZ 2^3...... 2^2 2^1 2^0 SB

0 0 0 0 P X X X X X X X X X X X X X X 0 1

1 0 0 0 0 of no importance, generally logic 0

0 0 0 0 P X X X X X X X X X X X X X X 1 0

VZ 2^3...... 2^2 2^1 2^0 SB

0 0 0 0 P X X X X X X X X X X X X X X 1 1

1 0 0 0 0 of no importance, generally logic 0

81 EZ10/R1010/R1210

S1 S2 S3

81 EZ10/R1010/R1210

* For module version 81 EZ10/R1010 no bias voltage UV is required

** Allocation or non-allocation of DA and DG, depending on the take-over mode
Transfer sequence 32-bit mode

Operating mode: binary code

Counter

Binary code

---

**For module version 81 EZ10/R1010 no bias voltage UV is required**

**Allocation or non-allocation of DA and DG, depending on the take-over mode**
Transfer sequence 32-bit mode

Operating mode: code conversion

Counter

Aiken or BCD code
Decade 1...4

2^0 2^1 2^2 2^3 ... 2^2 2^2

not used

E1 E2 E3 E4 E5 E6 E7 E8

Aiken or BCD code
Decade 5...8

2^1 2^2 2^3 2^4 ... 2^2 2^2

** Allocation or non-allocation of DA and DG, depending on the take-over mode

Code conversion: Aiken or BCD code to binary code with two's complement notation

IO-BUS ADDRESS

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DATA, SPEC. TELEGRAMS

0 0 0 0 X X X X X X X X X X 0 0

VZ 2^1 2^2 2^3 ...

0 0 0 0 X X X X X X X X X X 0 0

0 1 1 1 1 of no importance, generally logic 0

0 0 0 0 X X X X X X X X X 1 0

2^2^2 2^3 ...

0 0 0 0 X X X X X X X X X X 1 1

0 1 1 1 1 of no importance, generally logic 0

81 EZ10/R1010/R1210

* For module version 81 EZ10/R1010 no bias voltage UV is required
Mechanical design

The mechanical design is the same for all module versions.

Board size: 60U, 2 T, 160 mm deep

Connector: to DIN 41 612

- 1 x for IO-bus connection,
  48-pole, Edge-connector type F
  (connector X1)

- 2 x for process connection,
  32-pole, Edge-connector type F
  (connector X2, X3)

Weight: approx. 0.84 kg

The printed circuit boards 1 and 2 are connected with each other mechanically and electrically.

The exact contact allocation of the individual connectors can be seen from the operating principles description "Connectors of the IO-bus modules" GKE 705 321, the connection diagram or the functional diagram of the module.
POSITIONS OF THE ADJUSTABLE COMPONENTS AND VISUAL DISPLAYS ON THE FRONT

The front panels of the two module versions as well as the functions of the components shown are the same.

- Light-emitting diode for disturbance annunciation
- ST

- Disturbance annunciation for fuse US1
- Fuse for counter power supply

IG-bus address

<table>
<thead>
<tr>
<th>Significance</th>
<th>Hexadecimal</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>100</td>
<td>256</td>
</tr>
<tr>
<td>S2</td>
<td>10</td>
<td>16</td>
</tr>
<tr>
<td>S3</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
POSITIONS OF THE ADJUSTABLE COMPONENTS ON PRINTED CIRCUIT BOARD (1)

The printed circuit board incorporates the signal adaption of inputs E1.00 to E1.15, address switches S1, S2, S3 as well as the plug-in jumpers specified below.

Positions of the plug-in jumpers on the printed circuit board:

<table>
<thead>
<tr>
<th>Version</th>
<th>R1010</th>
<th>R1210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jumper</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-2</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>3-4</td>
<td>4-5</td>
<td></td>
</tr>
<tr>
<td>6-7</td>
<td>6-7</td>
<td></td>
</tr>
<tr>
<td>8-9</td>
<td>8-9</td>
<td></td>
</tr>
<tr>
<td>10-11</td>
<td>10-11</td>
<td></td>
</tr>
</tbody>
</table>

* Installation of this bridge depends on whether the counter is supplied with UV via contact z32 of connector X1 (standard interface SEA) or via contact b02 of connector X2 (process connector).
POSITIONS OF THE ADJUSTABLE COMPONENTS ON PRINTED CIRCUIT BOARD (2)

The printed circuit board incorporates the signal adaption of inputs E2.00 to E2.15, the processor unit, switch S4, as well as the plug-in jumpers mentioned in the following.

<table>
<thead>
<tr>
<th>Version</th>
<th>R1010</th>
<th>R1210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jumper</td>
<td>22-23</td>
<td>22-23</td>
</tr>
<tr>
<td></td>
<td>32-33</td>
<td>32-33</td>
</tr>
<tr>
<td></td>
<td>42-43</td>
<td>42-43</td>
</tr>
</tbody>
</table>

Memory modules:
(1) = bus and module program, A507
Order number (component):
Order number (PROM programmed):

GJTN160145P1
GJR2339250PXXXX

Note:
The mounting position of the component is specified by an imprint on the printed circuit board.
XXXX = Position numbers corresponding to the appropriate revision.
Technical data

In addition to the system data, the following values apply:

**MODULE VERSION:**

| Operating voltage US: | R1010 24 V | R1210 24 V |
| Negative bias voltage UV: | - | -24 V |
| Current consumption $I_{typ}$: | 300 mA | 300 mA |
| Power dissipation $P_{vtyp}$: | 9 W | 8 W ... 17 W |

The values specified for $I_{typ}$ and $P_{vtyp}$ apply for unloaded inputs. To obtain an exact value, the input loads must be added.

Reference potential IO-bus Z: 0 V 0 V

**POWER SUPPLY OF THE COUNTER REGISTERS**

| Operating voltage US1: | 24 V | 24 V |
| Negative bias voltage UV: | - | -24 V |
| Operating current $I_s$: | 300 mA | 300 mA |
| Fuse US1: | 500 mA | 500 mA |
| $I_V$: | 160 mA | |

**INPUTS**

Number of counters to be connected: One counter with 32-bit or two counters with 16-bit word length

Line length of the counters to be connected: $\leq 250$ m

Input designations: E1.00 to E2.15, DG1, DG2, VZ1 and VZ2

**INPUT VALUES**

| Input voltage $U_E$: | 24 V | 48 V |
| Input current $I_E$: | 1.6 mA | 5 mA |
MODULE VERSION

INPUT PULSE TIMES FOR COUNTER INPUTS E1.00 to E2.15

<table>
<thead>
<tr>
<th>Parameter</th>
<th>R1010</th>
<th>R1210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse duration ( t_d )</td>
<td>( \geq 9 \text{ ms} )</td>
<td>( \geq 40 \text{ ms} )</td>
</tr>
<tr>
<td>Pulse-off time ( t_p )</td>
<td>( \geq 9 \text{ ms} )</td>
<td>( \geq 40 \text{ ms} )</td>
</tr>
<tr>
<td>Delay time ( t_v )</td>
<td>( \leq 0.2 \text{ ms} )</td>
<td>( \leq 1 \text{ ms} )</td>
</tr>
<tr>
<td>Signal rise time ( t_{an} )</td>
<td>( \leq 1 \text{ ms} )</td>
<td>-</td>
</tr>
<tr>
<td>Signal fall time ( t_{ab} )</td>
<td>( \leq 1 \text{ ms} )</td>
<td>-</td>
</tr>
<tr>
<td>Bounce time ( t_{prell} )</td>
<td>-</td>
<td>( \leq 10 \text{ ms} )</td>
</tr>
<tr>
<td>Permit. frequency of LSB ( f_{LSB} )</td>
<td>( \leq 50 \text{ Hz} )</td>
<td>( \leq 10 \text{ Hz} )</td>
</tr>
<tr>
<td>Permit. frequency of counter ( f_z )</td>
<td>( \leq 100 \text{ Hz} )</td>
<td>( \leq 20 \text{ Hz} )</td>
</tr>
</tbody>
</table>

INPUT PULSE TIMES FOR DATA REQUEST

<table>
<thead>
<tr>
<th>Parameter</th>
<th>R1010</th>
<th>R1210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data valid time ( t_G )</td>
<td>( \geq 15 \text{ ms} )</td>
<td>( \geq 30 \text{ ms} )</td>
</tr>
</tbody>
</table>

OUTPUTS

Output designations | DAI, UA2 |

OUTPUT VALUES PER OUTPUT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>R1010</th>
<th>R1210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage ( U_A )</td>
<td>( \geq 13.7 \text{ V} )</td>
<td>( \geq 13.7 \text{ V} )</td>
</tr>
<tr>
<td>Output current ( I_A )</td>
<td>( \geq 100 \text{ mA} )</td>
<td>( \geq 100 \text{ mA} )</td>
</tr>
</tbody>
</table>

PERMISSIBLE AMBIENT CONDITIONS

Effect of supply voltage variations: none at 16.8 V ... 33 V supply voltage
Total voltage dip: \( \leq 1 \text{ ms} \)
Operating temperature: \( 0 \text{ °C} ... 70 \text{ °C} \)
Storage temperature: \( -40 \text{ °C} ... 85 \text{ °C} \)

ORDERING DATA

Complete module

1. Type designation: 81 EZ10-E/R1010
   81 EZ10-E/R1210
   Order number: GJR2339200R1010
   GJR2339200R1210

2. Memory components: see "Mechanical design"

Technical data are subject to change without notice.