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DYNAMICAL PERFORMANCE OF TCSC SCHEMES

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Summary: *The paper describes a control method, Synchronous Voltage Reversal (SVR), which can be applied to Thyristor Controlled Series Capacitors (TCSC). SVR is characterised by a hierarchical structure of the control. From the lowest to the highest level the layers contribute with apparent impedance characteristics at subsynchronous frequencies, apparent reactance at mains frequency and power-system related control objectives. The paper describes how such a control scheme can be derived based on a conceptual description of the TCSC operation.*

Keywords: *series capacitor, thyristor controlled series capacitor, apparent impedance, subsynchronous resonance, synchronous voltage reversal, TCSC, SSR, SVR*

1. INTRODUCTION

The Thyristor Controlled Series Capacitor (TCSC) seems to be one of the members within the FACTS family, beside the SVC that was established long ago, which has attracted the most interest so far. One reason may be that a distinctive quality of the TCSC concept is that it uses an extremely simple main circuit topology. The capacitor is inserted directly in series with the transmission line and the thyristor controlled inductor is mounted directly in parallel with the capacitor. Thus no interfacing equipment like e.g. high voltage transformers is required. This makes TCSC much more economical than some other competing FACTS technologies.

The present status of development is that hardware for the TCSC has been developed by several manufacturers and that field experience has been gained since 1991 [1], when the first valve was put into service in a high-voltage transmission system. Thus one important obstacle for the introduction of this new technology has been removed as field experience shows that it is possible to design and operate thyristor valves that are installed outdoors in high-voltage switchyards with good operational records.

2. TCSC APPLICATIONS IN POWER SYSTEMS

Several studies on the use of controllable devices connected in series with the line (TCSC, PAR, UPFC) show that they have some advantageous control properties when compared with shunt devices [2-6]. The control offered by TCSC is an 'impedance' type control, i.e. the inserted voltage is proportional to line current. This type of control normally is best suited to applications in power flow corridors, where a well-defined phase angle difference exists between the ends of the transmission line to be compensated and controlled.

The concept of controlled series compensation can be used for a wide range of objectives in the power system control technology. Naturally the power flow pattern can be influenced by changes of the impedances in the network. Similarly series compensation may be used as a means for adapting the loadability of certain critical lines that would risk to be operating with too large angle separation or amplitude deviations during contingencies. This kind of applications often requires a substantial rating of the controllable inserted reactance but do not require very high speed of control. Therefore an economical solution many times can be achieved using

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mechanically switched capacitor modules.

Controlled series compensation also can be used to provide additional damping of electromechanical (0.5-2 Hz) power oscillations. Then thyristor control may be motivated, as TCSC provides fast speed of response and executes any switching patterns without such restrictions that might apply for mechanical breakers. A significant improvement of damping often can be achieved even if the rating of the controllable reactance is small.

Beside the applications mentioned above TCSC offers a unique possibility to apply series compensation in networks where the risk for Sub Synchronous Resonance (SSR), between the transmission system and generators in thermal power stations, is a concern. In such systems hitherto series compensation has been avoided or limited to a lower degree of compensation than what is desirable from a system operation standpoint. Inserting a TCSC may alleviate such limitations thereby increasing the transfer capability of the transmission system.

It is likely that installations of controllable series compensation will include both fixed or mechanically switched modules (MSSC) and thyristor controlled modules (TCSC) in a variety of combinations.

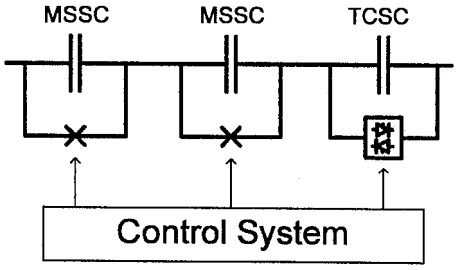


Figure 1: Outline of CSC with MSSC and TCSC

Thereby an economical equipment can be designed to meet the specific requirements of every certain installation. Therefore, in design of TCSC control system, an essential consideration is that it must possess the flexibility to be adapted to a wide range of different applications. The scope of this paper is to present an approach to this task which is based on modular concept, where different layers in a control hierarchy provide the TCSC with the necessary characteristics.

3. CONCEPTUAL CONTROL STRUCTURE FOR TCSC

The control system for a TCSC has to take into account a number of requirements that each is influenced by the control system response in certain time ranges:

- SSR behaviour, influenced by the TCSC response to line current changes within 10 ms
- inserted reactance control at the power frequency, influenced by TCSC response to line current amplitude changes during 50-100 ms
- power system control, e.g. adding damping to electromechanical power swings, influenced by the TCSC response during several cycles i.e. 100-500 ms

A natural approach would be to implement the control system as a layered control structure where each layer acts with a certain time horizon and where the layer with the shortest 'memory' is located closest to the TCSC. A major advantage with this approach is that it becomes possible to treat the different control objectives separately.

The performance of the TCSC at subsynchronous frequencies is a feature of specific interest as was pointed in section 2. Sometimes it may be the main reason for installing the TCSC. The SSR behaviour of TCSC reflects how it reacts on injected line current deviations caused by torsional vibrations in the generator shaft in a frequency range from 10 to 40 Hz (50 Hz systems) or to 50 Hz (60 Hz systems). One way of describing the TCSC characteristics is to specify its small-signal apparent impedance as indicated in figure 2 b). This apparent impedance is defined as the quotient between the phasors representing the voltage deviation across the TCSC and the injected line current deviation at the subsynchronous frequency.

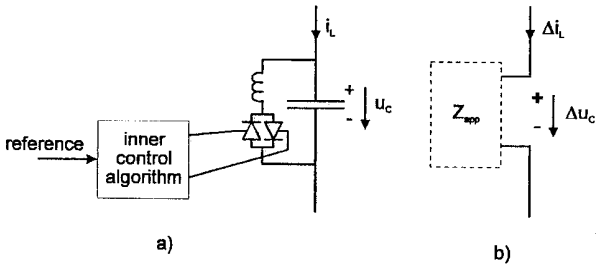


Figure 2: TCSC inner loop
a) outline
b) apparent impedance at subsynchronous frequency

It is natural that the dynamical performance of the TCSC at such high frequency is closely associated with the thyristor triggering algorithm in use. Therefore it is desirable that this very inner control loop provides the basic SSR immunity. It will be shown in section 5.2 that it is possible to design the inner loop so that the apparent impedance of the TCSC becomes resistive-inductive in the whole subsynchronous frequency range. By doing so no electrical resonance can occur between the transmission line and the TCSC and the prerequisite of SSR will be eliminated.

However, the TCSC should not appear inductive close

to the rated frequency of the power system as it is supposed to compensate the inductive reactance of the line at mains frequency. Therefore a second layer of control is implemented on top of the inner loop as shown in figure 3.

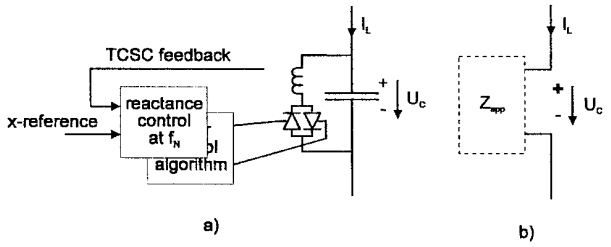


Figure 3: TCSC reactance control loop
a) outline
b) apparent impedance at power frequency

The reference for this new loop relates to the apparent reactance, x, at network frequency. The reactance value can be boosted by the TCSC to a value exceeding the reactance of the physically inserted capacitor. The maximum reactance boost depends on the actual line current and the duration of the boosting action, as the voltage handling capability of the capacitor and the TCSC valve is limited and depends on the duration of the voltage stress.

The possibility to control the apparent reactance of the TCSC at network frequency can be utilised to improve the power system performance. One objective may be to provide additional damping of electromechanical oscillations. Another may be to temporarily increase the degree of compensation of one line in order to alleviate the voltage drops in nodes that do not have sufficient reactive power support in cases of contingencies. Other applications can be oriented towards power flow control objectives. The principal arrangement is illustrated by figure 4. The outer loop provides functionality in the power system in terms of damping, voltage boosting, power flow control etc and needs to be programmed specifically for each application.

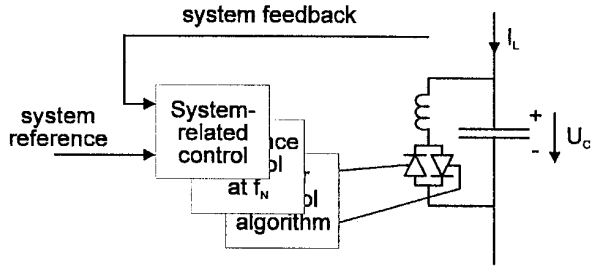


Figure 4: TCSC power system related control

In the layered structure of the control system outlined above, it has been an objective for the inner loops to provide a control mode of SSR immunity that is independent of the power system parameters. The independence from the power system parameters is essential to guarantee a safe and reliable operation under varying network conditions. The outer loop, which is specific to each installation, does not require a high speed of response in order to obtain an adequate SSR behaviour, since this feature is provided by the inner loops. The outer loop can be tuned with respect to the power system requirements only.

4. ANALYSIS OF THE THYRISTOR ACTION IN TCSC

The theoretical description of the TCSC naturally will form the base for the design of the control system. Basically two approaches could be followed, one originating from a description of steady-state conditions, the other one from a description of transient conditions.

4.1 Steady-state approach

Traditionally thyristor converters have been described using the trigger angle, α, as the control variable. This angle indicates the delay in electrical angle from the earliest instant when the thyristor obtains forward blocking voltage until it is fired. The steady-state characteristics of the apparent reactance of the TCSC at rated frequency versus the trigger angle often is illustrated as in figure 5 b). The angle range immediately below 180° is used to provide controllable capacitive reactance, i.e. the normally used 'reactance boosting' area.

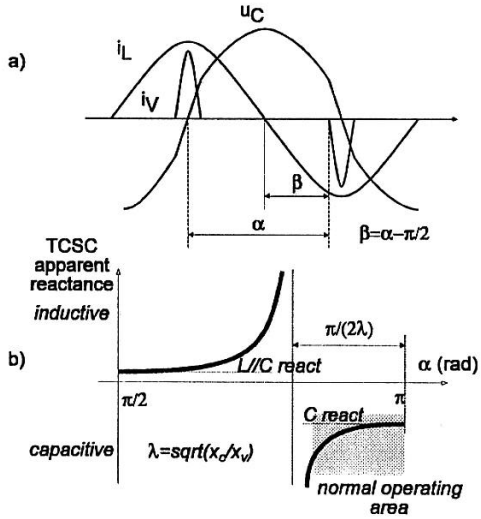


Figure 5: Steady-state power frequency characteristics of TCSC
a) definition of trigger angle
b) apparent reactance at power frequency

The steady-state characteristics is strongly non-linear and exhibits an asymptotic behaviour for at least one control angle. This asymptote corresponds to the triggering angle for which the apparent reactance of the

thyristor controlled inductive reactance equals the reactance of the capacitor. At this point the apparent reactance of the TCSC becomes infinite. The control angle close to the asymptote must be avoided by the controller. The steady-state description of the TCSC only involves the factor λ, that describes the ratio between the power frequency and the resonance frequency of the combination of the thyristor branch inductor and the capacitor in the TCSC. However, in transient conditions the capacitor voltage of the TCSC depends on the disturbance in a rather complicated way. An example is shown in figure 6. A TCSC (λ=5) is simulated, which is triggered at a fixed angle relative the line current (α=165°). 10 percent amplitude change of the line current is imposed at varying phase angles within a half-cycle of the mains frequency. The associated changes of the capacitor voltage are shown.

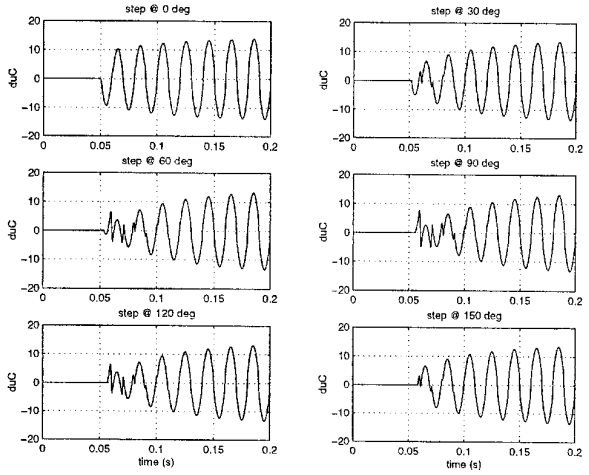


Figure 6: Change of capacitor voltage caused by line current amplitude changes
at different phase relative the line current

It can be seen from the curves that the dynamical response of the TCSC involves time constants in the range of 100 ms and that it is influenced significantly by the phase of the line current change. Other parameters, like the boost level etc also impacts on the response. Therefore it appears that a generally applicable theory, valid in a wide frequency range, can not be derived using the trigger angle as the control variable.

4.2 Transient approach, Synchronous Voltage Reversal

An alternative description of the TCSC can be derived starting from the transient occurring when a thyristor is fired in the TCSC. Using a new control variable it is possible to describe the TCSC in transient conditions in a way that is much easier to conceptually understand. It becomes possible to describe the TCSC, also transiently, decoupled from the external parameters. The method is the 'Synchronous Voltage Reversal' (SVR), which shall be described below.

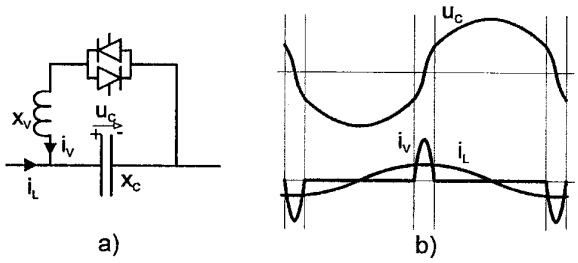


Figure 7: TCSC in steady-state
a) circuit, b) waveforms

Figure 7 shows the waveforms associated with a TCSC when operating in steady-state. The thyristor conduction intervals are substantially shorter than the network frequency half-cycle time and they occur around the peak values of the line current. Accordingly the variation of the line current during the thyristor conduction interval is rather small and the line current can be approximated by a constant current. With this approximation the capacitor voltage varies linearly before and after the conduction interval as shown in figure 8.

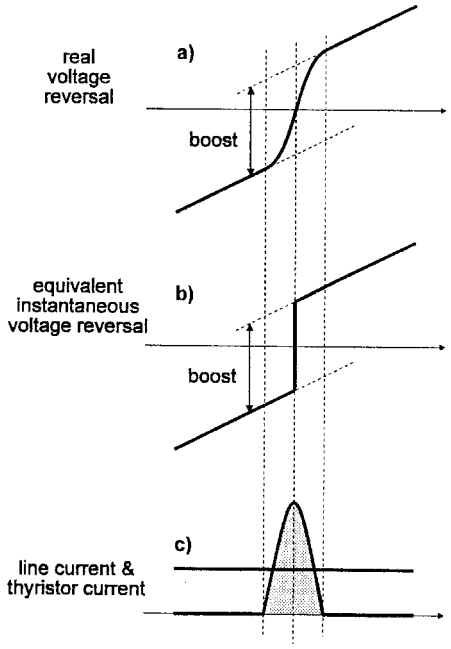


Figure 8: Capacitor voltage reversal
a) real transient
b) equivalent instantaneous voltage reversal
c) currents

When the thyristor is fired a current pulse passes through the thyristor and the capacitor voltage is repolarized. Ideally, with no losses, the thyristor ceases to conduct exactly when the capacitor voltage magnitude is equal to the initial magnitude at turn-on. In other words a capacitor voltage reversal occurs during the

thyristor conduction interval. The charge passing through the thyristor branch brings about a parallel displacement of the lines representing the capacitor voltages before and after the conduction interval. This displacement represents the boost that is achieved by the thyristor action. From the power system point of view the amount of boost (i.e. the parallel displacement) is of particular interest, but the exact waveform of the transient is not. Figure 8 b) shows that the correct amount of boost can be obtained by an equivalent, instantaneous reversal of the capacitor voltage in the middle of the thyristor conduction interval.

It can be concluded that the capacitor voltage can be described adequately if the instants of these equivalent, instantaneous reversals of the capacitor voltage are known. It shall be noted that the length of the thyristor conduction interval varies depending on initial conditions so the delay between thyristor turn-on and the equivalent reversal also varies. The idea of the Synchronous Voltage Reversal (SVR) scheme is to directly control the timing of the equivalent, instantaneous voltage reversals, since this provides some desirable features

- eliminates non-linearity in boost control (section 5.1)
- inductive apparent impedance at subsynchronous frequencies (section 5.2)

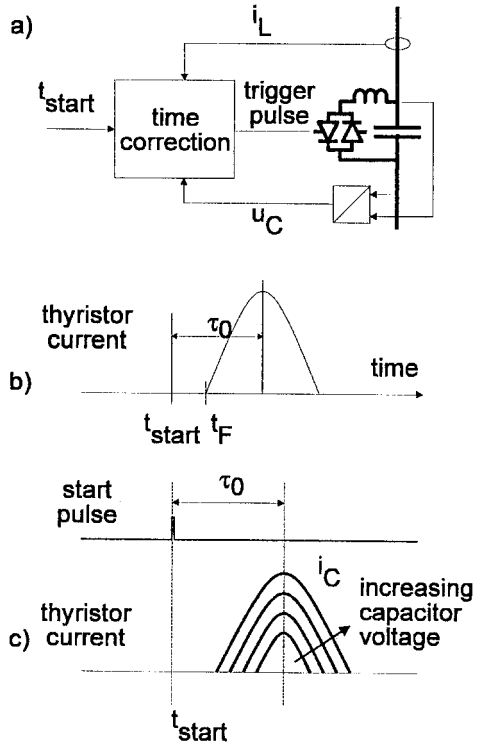


Figure 9: TCSC with time-correction circuit
a) time correction circuit outline
b) thyristor triggering
c) thyristor currents for varying conditions

In practice this task can be achieved by the use of a time-correction circuit as shown in figure 9 a).

When a start pulse is given to the time-correction circuit at t_{start}, it fires the thyristor at t_F, which is selected so that the thyristor current reaches its peak (capacitor voltage crosses zero) with a fixed delay, τ_0, after the start pulse. The time-correction circuit determines the firing instant, t_F, depending on the measured instantaneous values of capacitor voltage and line current. Depending on the actual capacitor voltage and line current different thyristor firing instants will be selected by the time correction circuit. The amplitude of the thyristor current varies as shown in figure 9 c) depending on the initial conditions but it always peaks with a constant delay, τ_0, after the start pulse.

5. THE SVR METHOD IN A LAYERED CONTROL STRUCTURE FOR TCSC

The number-one objective of the TCSC is to provide a capacitive reactance at power frequency to compensate the inductive reactive voltage drop in the lines. It will be shown that the direct control of the capacitor voltage zero-crossings, which is a characteristic property of the SVR method, is an excellent means to control the capacitor voltage boost level. This control corresponds to the second layer in the control hierarchy discussed in section 3.

5.1 Boost control

The capacitor voltage is approximated as in figure 10.

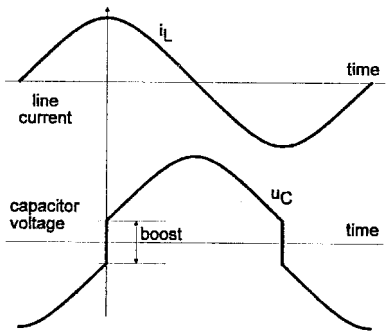


Figure 10: Idealized waveform of TCSC

In steady-state the capacitor voltage zero-crossings are equidistant, separated by the line current's half-cycle time. Then the zero-crossings must appear at well-defined time instants which are determined by the condition that the charge received from the line current in the time interval between two consecutive zero-crossings must vanish. Namely, if this condition is fulfilled, the capacitor voltage before the next reversal will be identical with the voltage after the preceding one and the boost remains constant. This is illustrated in figure 11 a). In figure 11 b) the reversal instants have been advanced relative the equilibrium positions in a). Then the net

charge received by the capacitor increases between the consecutive reversals and the boost level increases at each reversal. Contrary, in figure 11 c) the reversals have been retarded relative the equilibrium and the boost voltage reduces between each reversal.

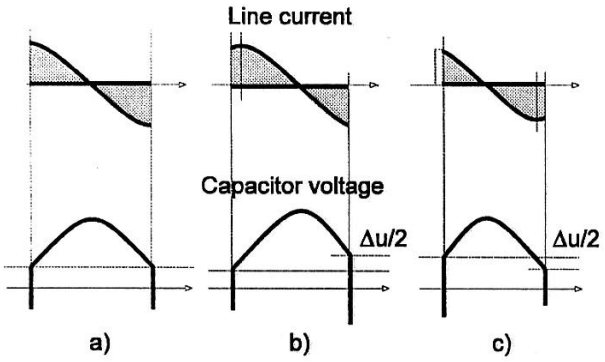


Figure 11: Boost voltage
a) steady-state
b) increasing boost
c) decreasing boost

Thus the TCSC boost level can be described from a control point of view as an integrating system that increases or decreases the boost proportionally to the time displacement of the zero-crossings of the capacitor voltage from their positions relative to the line current. The external network parameters have no impact on the control system except for the amplitude of the line current and the reactance of the capacitor in the TCSC. The boost level can easily be controlled by a simple feedback loop using measured capacitor voltage.

Figure 12 presents a time-domain simulation of a TCSC circuit (λ=5) using the EMTDC program. It illustrates the nature of the TCSC when the timing of the equivalent reversals is controlled to remain equidistant at their steady-state equilibrium positions during a line current disturbance. I.e. the start-pulses to the time-correction circuit are not influenced by the line current change at all. The thyristor triggering is achieved with the time correction circuit according to the SVR principle. The two upper plots to the left in figure 12 a) and b) show the change of capacitor voltage components in a rotating frame that is aligned with the steady-state line current vector. The lower left plot shows the change of scalar zero-sequence capacitor voltage. The right-hand plots are the thyristor currents in the three phases of the TCSC. In figure 12 a) the line current amplitude is changed. It can be seen that the triggering of the thyristors will be modified by the SVR algorithm so that the capacitor voltage remains constant. The thyristor current will be changed by the transient, but the circuit's characteristic behaviour is to keep the capacitor voltage unchanged. In figure 12 b) a phase shift occurs in the line current. If the line current is phase retarded, as in figure 12 b), the magnitude of the capacitor voltage (negative component in steady-state) increases.

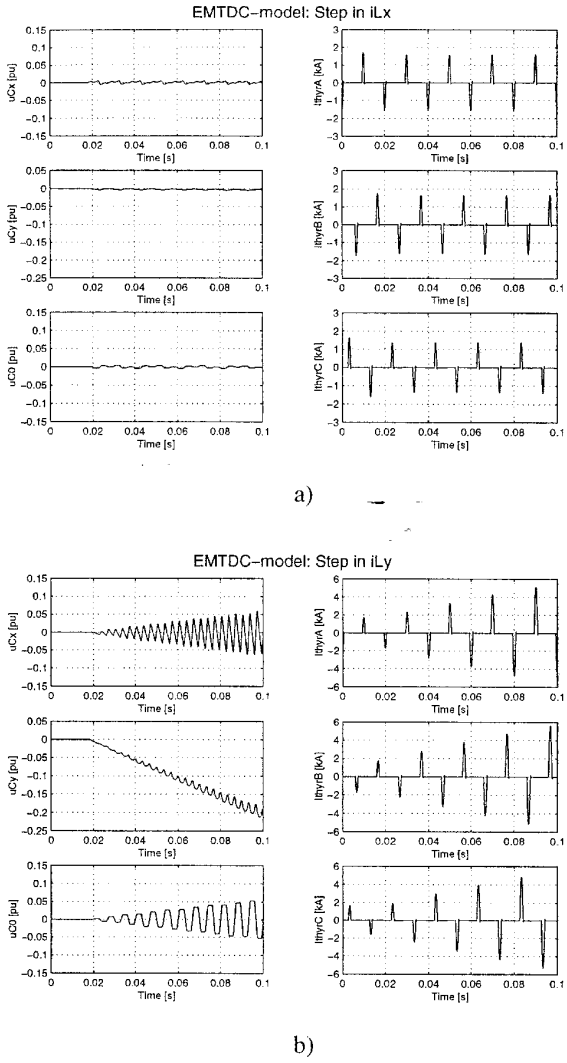


Figure 12: EMTDC simulation on current-source system
a) current amplitude change
b) current phase shift

By using the timing of capacitor voltage zero-crossings as control variable instead of the trigger angle the system describing capacitor voltage boost becomes linear and independent of the boost level. The problems caused by the non-linearity of the characteristics using the trigger-angle as a control variable thereby has been eliminated. In the SVR scheme a capacitor voltage controller is implemented in the control. This practically eliminates the risk of generating excessive capacitor voltages.

5.2 SVR characteristics at subsynchronous frequencies

It was mentioned earlier that a basic property of the TCSC inner loop relates to its performance at subsyn-

chronous frequencies. Figure 13 shows a generator that is connected to an electric network via a TCSC.

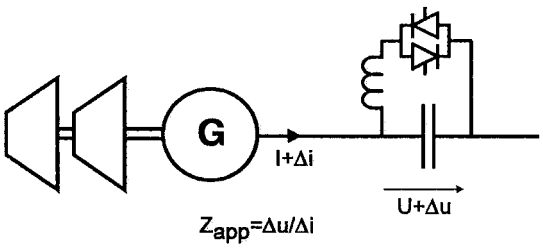


Figure 13: Definition of apparent impedance of TCSC

The small-signal apparent impedance of the TCSC is defined in the figure. As has been discussed in section 3 SSR can not exist at frequencies where there is no electrical resonance. Therefore it is interesting to investigate the apparent impedance of the TCSC at subsynchronous frequencies. Again, when the TCSC operates with the SVR control, it can be approximated by equivalent, instantaneous reversals of the capacitor voltage, and a very simple model can be presented. Namely, assume that the capacitor voltage zero-crossings occur at their steady-state positions and that these instants are not influenced by a small superimposed subsynchronous line current. Then a recursive formula for the deviation voltage caused by the superimposed current can easily be calculated by integrating the superimposed line current for a half cycle, calculating the corresponding capacitor voltage change and then reversing the capacitor voltage. The losses in the TCSC circuit can be modelled using a reversal factor, D_f, defined by the ratio of capacitor voltage magnitudes after and before the thyristors conduction interval. In a discrete system, where the capacitor voltages are sampled in the midpoints between the reversals the following formula will be obtained:

$$Z_{app}(j\Omega) = (-jx_C)\frac{\omega_N}{\Omega}\frac{\left(e^{j\frac{\Omega\,\pi}{\omega_N\,2}} - D_f\right)\left(e^{j\frac{\Omega\,\pi}{\omega_N\,2}} - 1\right)}{\left(e^{j\frac{\Omega\pi}{\omega_N}} + D_f\right)} \qquad (1)$$

where Ω and ω_N are the angular frequencies of the subsynchronous injected current and the steady-state line current respectively. x_C is the reactance of the physical capacitor of the TCSC. Figure 14 illustrates the calculation method. The dashed line is the injected 25 Hz subsynchronous current, which should have an infinitesimal amplitude, but which has unity amplitude in the calculation. The solid curve represents the additional capacitor voltage, produced by the subsynchronous line current, across a unity capacitor. The capacitor operates with a steady-state 60 Hz line current which causes it to reverse its voltage with a 120 Hz repetition frequency. The vertical solid lines indicate the voltage reversals. Finally the midpoints in the voltage curve segments between the reversals are indicated and connected. They will fall on a sinusoidal that leads the current by 90°, showing that the apparent impedance of the TCSC is an *inductive* reactance. The quotient between the phasors representing the sinusoidals in figure 14 is the apparent impedance given in (1).

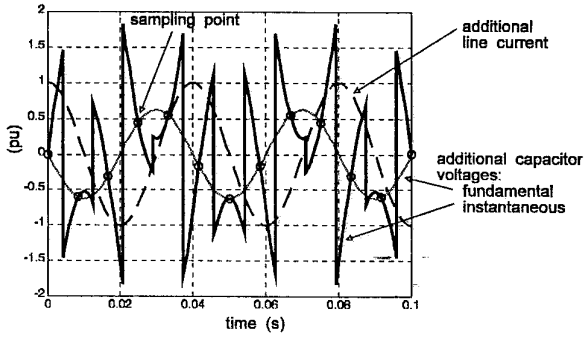
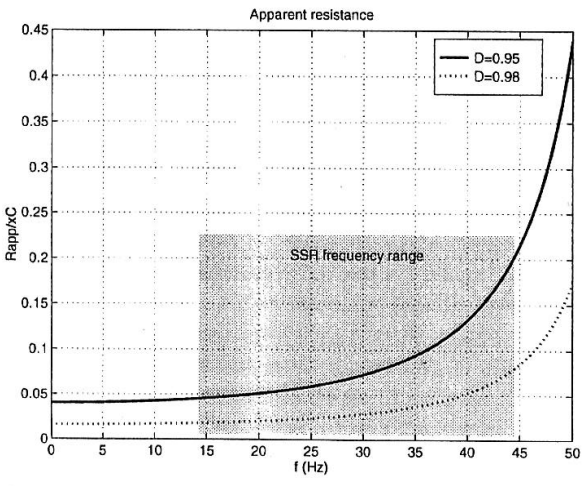
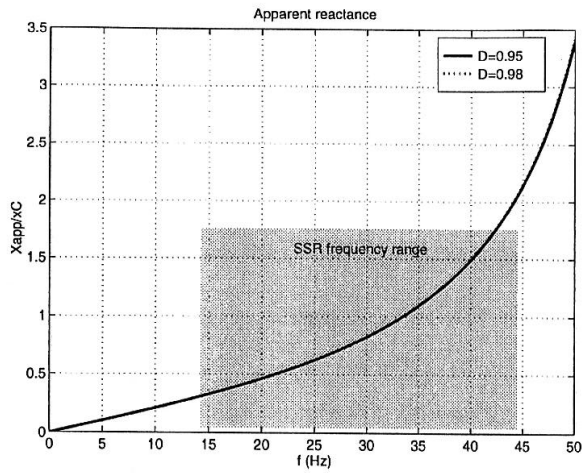


Figure 14: Deviation current integration/reversal process in TCSC. 25 Hz current injected into 60 Hz TCSC.

Evaluating the formula (1) for different frequencies and loss factors yields the curves in figure 15. It can be seen that the apparent impedance remains resistive-inductive in the whole subsynchronous frequency range. The reactance increases asymptotically when the subsynchronous frequency approaches the line current frequency. It can be concluded that if the bandwidth of the controllers outside the inner control loop is not too high the TCSC characteristics of the apparent impedance eliminates the risk of SSR. The impedance characteristics of the TCSC was derived without the use of any parameters in the power system and they really are characteristics of the TCSC itself.



a)



b)

Figure 15: Ideal SVR characteristics
a) apparent resistance
b) apparent reactance

A reactance controller according to section 5.1 introduces a transfer of the apparent impedance characteristics from the ideal curve in figure 15 into a controllable reactance around the power frequency. This is shown in figure 16.

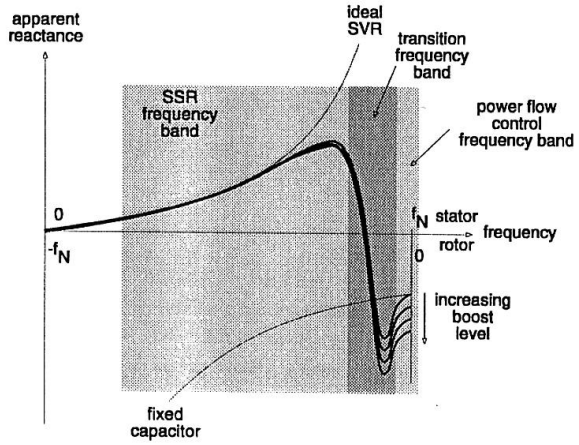


Figure 16. Impedance characteristics of TCSC

5.3 Power system related control

So far the two layers closest to the thyristor control have been described. They provide the TCSC with its SSR mitigating characteristics and its capability to control the inserted reactance at power frequency. These properties are determined by control parameters only (except λ, which is used in the time-correction circuit) and the parameters of the external network do not appear. The power system control objectives normally are related to electromechanical transients. As such dynamics is slow compared to the dynamics of the TCSC, a quasi-stationary description can be used in system studies, and the TCSC can be represented by a controllable reactance at power frequency. The characteristics of the TCSC at subsynchronous frequencies remain unchanged if the bandwidth of the outer loop is limited.

6. WIDE BANDWIDTH MODELLING OF TCSC

Studies related to SSR and reactance control of the TCSC require a correct description of the TCSC in the frequency range from DC to rated frequency. The approximation of the TCSC behaviour with the equivalent, instantaneous voltage reversals offers a possibility to derive simple linearized, small-signal models of the TCSC. These models take no parameters beside the reactance of the capacitor in the TCSC (x_C), the loss factor (D_f), and the line current frequency and amplitude in the steady-state point around which the system is linearized. In three-phase systems it is suitable to use a sampling interval that is one sixth of a power cycle i.e. 3.33 ms in a 50 Hz network or 2.78 ms at 60Hz.

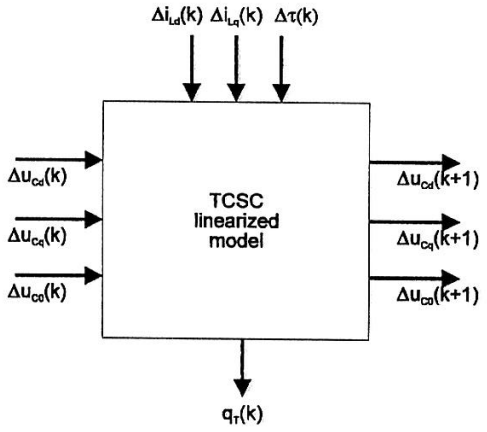
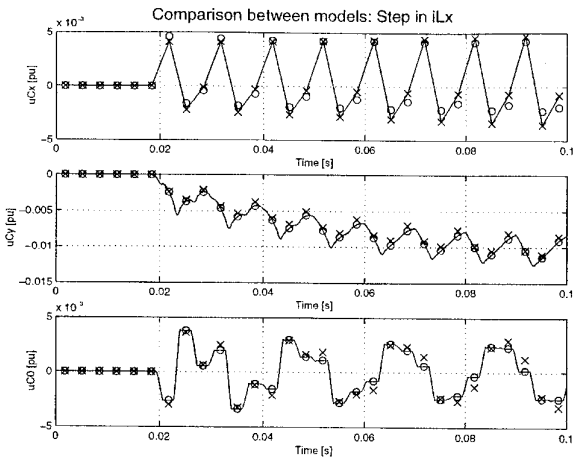
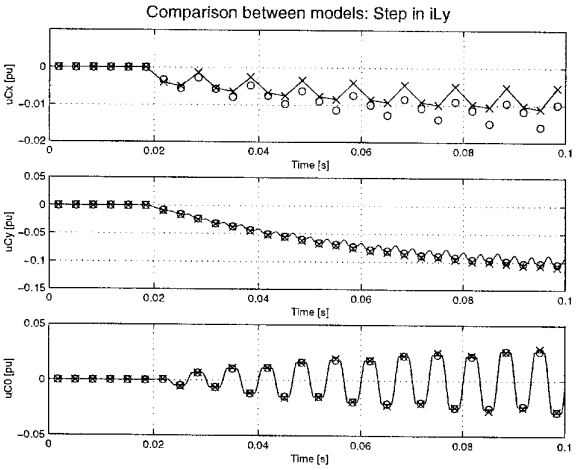


Figure 17: Linearized model of TCSC

Figure 17 indicates that the model has three states corresponding to the two components of the voltage vector in a rotating frame (aligned with the steady state current vector) and the scalar zero-sequence voltage. The input signals considered are the components of the line current vector in the same rotating frame and the control timing signal for the equivalent reversals. In figure 18 a comparison is presented between a discrete model using the equivalent, instantaneous capacitor voltage reversal approximation and a time-domain simulation. The system is a SVR controlled TCSC with equidistant start-pulses. The transient that is simulated is a line current change in amplitude and in phase. In figure 18 the circles indicate the midpoint of the analogue traces obtained by the time-domain simulator, while the x-marks indicate the states in the discrete model based on the approximation of instantaneous voltage reversals.



a)



b)

Figure 18: Comparison between discrete linearized model (x) and analog circuit simulation (o)
a) line current amplitude step
b) line current phase step

These models describe the TCSC as a dynamical system in its [A,B,C,D] form. Such a representation provides a versatile link to incorporate the TCSC model into programs that can linearize the power system around a steady state point obtained by a power flow program. This approach is very suitable for power control system development and tuning.

7. POTENTIAL IMPACT OF SVR ON SERIES COMPENSATION

The SVR method introduces a universally applicable control structure for the TCSC control. It offers a SSR-immune series compensation, which means that higher degrees of series compensation can be envisioned when power systems are being planned. In many cases the large investment for the construction of an additional transmission line can be postponed for a number of years if the power system expansion is optimised taking the possibility of series compensation into account.

8. CONCLUSIONS

In this paper a control structure for TCSC has been discussed. The concept of equivalent, instantaneous reversals of the capacitor voltage was introduced. This concept is the origin of the Synchronous Voltage Reversal scheme that has been described. It has been shown that this concept is applicable to a layered structure control system, where the inner loop provides SSR immunity to the TCSC. The SVR concept also eliminates non-linearities in the control system and prevents the TCSC from boosting the capacitor voltage to excessive levels. The theoretical concepts behind the SVR method also provides a base for simple small-signal models that can be interfaced into simulating packages that generate a linearized [A,B,C,D]-representation of the power system.

9. REFERENCES

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