

## A New Synthetic Test Circuit For the Operational Tests of HVDC Thyristor Modules

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**Abstract** — Modern power thyristor valves have a high power rating and are difficult to test in a back-to-back test circuit in the test laboratory. Verification of thyristor valve design with synthetic test circuits is an alternative. The core to design a synthetic test circuit is to correctly reproduce the stresses applied on the thyristor valves. Voltage and current stresses on the thyristors under four operational states are highlighted in this paper. A new synthetic test circuit has been developed by ABB Power Systems. This new circuit reproduces the correct stresses applied on the high voltage direct current (HVDC) thyristor valves in service. Verifying tests reveal that the circuit design was a success.

Keywords:

HVDC, thyristor modules, operational tests, synthetic test circuit, high power laboratory, type testing

### I. INTRODUCTION

To test thyristor valves, it has been the custom in ABB Power Systems to use a back-to-back test plant (referred as the direct test circuit in this paper) in which generators are used to supply the power for the tests. The rating of this direct test circuit is 8.0 kV / 4000 A or 15 kV / 1500 A ( $U_{dio} / I_{dc}$ ).

The power handling capability of modern thyristors has seen a significant progress in the past twenty years. Modern thyristor valves have a high power rating per thyristor level. The direct testing power is sufficient only for testing maximum three thyristor levels. Testing of thyristors up to three levels in series per valve could cause controversy on the representation of voltage distribution on the thyristor levels during the test. Studies show that valve sections with five or more thyristor levels can be considered an adequate representation [1] [3]. As a consequence of the increment of the number of thyristor levels under test the power rating of the test plant has to be proportionally increased.

To increase the direct testing power is neither an economical nor a very practical solution. Synthetic testing is recommended by CIGRE [3] as an alternative to the direct testing.

Synthetic testing methods are based on the fact that the HVDC thyristor valve is stressed by current and voltage at different time intervals. The current stress occurs during the conducting interval followed by the voltage stress during the

blocking interval of the valve. It is, therefore, possible to apply different stresses by two separate sources at different time intervals.

To ensure the equivalence of synthetic testing of HVDC thyristor valves a complete understanding of current and voltage stresses on the thyristor valve is necessary. In a synthetic test circuit these stresses should be correctly reproduced. The turn-on and turn-off are the two most critical operating for the thyristor valves. A close representation of these two states in a synthetic testing circuit ensures the testing equivalence.

A joint project group between ABB Power Systems and ABB Switchgear was set up to develop and implement the new synthetic test circuit. The design of the synthetic test circuit, its operating principle, and operational tests conducted with the synthetic test circuit are described in this paper.

### II. VALVE STRESSES

Voltage and current stresses on a thyristor valve during operation can be analyzed separately in four operational states: off-state and reverse voltage, turn-on, on-state and turn-off state[4] [5] [6].

Off-state and reverse voltage: Voltage – current characteristics determines the maximum permissible operational voltage. Under steady-state operating conditions the valves endure transient voltage excursions at turn-off. Another voltage stress on the valves will be the transient forward voltage during the recovery period. The thyristors must be adequately protected against the effects of these transients without unacceptably affecting the performance.

Voltage jumps in the off-state and reverse voltage contribute to the losses of valve damping resistors and valve reactors. To apply the correct stress on these components the value of the complete off-state and reverse voltage waveform should equal or exceed these in service.

Turn-on: A high initial di/dt passes through the thyristors due to the stray capacitance and the damping capacitor of the thyristor valve after firing. This high di/dt can give rise to excessive power density in the silicon which can cause failure through local melting.

To produce the right  $di/dt$  after firing correct stray capacitance and voltage on the stray capacitance before firing have to be fulfilled. Direct test circuits meet these requirements easily by scaling the valve's operational parameters to test sections. However, in a synthetic test circuit attention has to be paid to the circuit layout to achieve the real turn-on stress.

**On-state:** At turn-on the thyristors become conducting and produce conduction losses. The conduction losses will result in an increase of the junction temperature, which may deteriorate the voltage blocking capability of the thyristor. To verify the thermal performance of thyristors, correct amplitude and duration of conducting current are of special importance.

**Turn-off:** After turn-off the valve withstands a transient recovery voltage with a voltage overshoot and subsequently power frequency recovery voltage. The transient recovery voltage is not only controlled by the main circuit and damping circuit but is also influenced by the recovery charge of the thyristors. The overshoot is the result of interaction between the main circuit, damping circuit and recovery charge in thyristors.

It is fundamental to correctly reproduce the current and voltage stresses on the test object in all four operational states above. By adjusting test circuit parameters the conditions for above four operational states should be achieved. Special consideration has to be paid to the  $di/dt$  at turn-off since it affects the recovery charge of the thyristors.

### III. THE SYNTHETIC TEST CIRCUIT

#### A. Circuit Description

The diagram of the synthetic test circuit is given in Figure 1. Two sources (current source and voltage source) supply the test current and voltage alternately to the test object ( $V_t$ ) by the help of several auxiliary thyristor modules ( $V_{a1}$  to  $V_{a5}$ ).  $C_t$  represents the stray capacitance and  $L_1$  represents the commutation inductance in service. Both  $C_t$  and  $L_1$  are scaled from service condition.

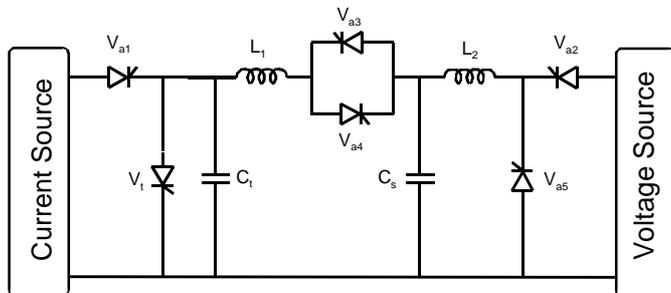


Fig. 1. The synthetic test circuit



Fig. 2. View of six-pulse back-to-back bridges and test object



Fig. 3. Capacitor banks of the voltage section

The current section consists of two six-pulse bridges connected in back-to-back mode (one bridge as rectifier and the other as inverter). Two six-pulse bridges, valve units for short circuit testing, auxiliary valve  $V_{a1}$  and test object  $V_t$  are assembled in one mechanical structure as shown in Figure 2. The whole structure is suspended from the ceiling of the test hall and the test object  $V_t$  is located at the bottom of the structure. Auxiliary valve  $V_{a1}$  and the test object  $V_t$  are one

arm of the rectifier. A low bridge voltage is used in the current source. Corresponding to this low bridge voltage a low commutation inductance is selected in order to keep the right commutation overlap. The current source voltage is high enough to generate the requested short-circuit current.

The voltage section comprises of a DC voltage source, one capacitor bank  $C_s$ , two reactor banks  $L_1$  and  $L_2$  and auxiliary valves  $V_{a2}$  to  $V_{a5}$  as shown in Figure 1. The capacitor banks used to configure the voltage section of the synthetic test circuit are shown in Figure 3. The DC source is continuously adjustable up to 70 kV. The inductance of reactor bank  $L_2$  can be adjusted between 0.2 mH to maximum 211 mH. The capacitance of capacitor bank  $C_s$  can be adjusted between 0.9  $\mu$ F to 72  $\mu$ F. Forward and reverse voltages are formed by firing auxiliary valves at specific instants. The output voltage level of the DC source controls the voltage amplitude. An impulse generator is also included in the voltage section (not shown in Figure 1). The impulse generator is connected to the high potential terminal of test object when tests of transient voltage during the recovery period are performed.

### B. The Operating Principle of the Synthetic Test Circuit

The operating principle of the synthetic test circuit is illustrated in Figure 4 and described as follows:

As one arm of the six-pulse bridge,  $V_{a1}$  and  $V_t$  conduct a current representing the service current ( $t_0$  to  $t_2$  in Figure 4). The current source has a reduced driving voltage.

Shortly before the load current  $I_d$  (from the current source) in  $V_t$  reaches its zero ( $t_2$ ) the positive charge in  $C_s$  is released by firing  $V_{a3}$  at  $t_1$ . The injection current of the voltage circuit extinguishes  $V_{a1}$  at  $t_2$  and isolates the current source until firing  $V_{a1}$  in the next period.  $V_t$  conducts the injection current alone about 600 $\mu$ s (adjustable) after the main current zero.

The injected current is of a sinusoidal waveshape.  $L_1$  is a key component and is selected to be representative of the phase-to-phase commutating inductance of the real circuit.  $C_s$  in conjunction with  $L_1$  is selected to have the half wave injection time ( $t_1$  to  $t_3$ ) equal to or higher than 600  $\mu$ s [3]. The pre-charged voltage on  $C_s$  together with the inductance of  $L_1$  will give a close representation of the service current in the interval 200  $\mu$ s before current zero ( $t_3$ ).

$V_t$  blocks at the injected current zero. The voltage on  $C_s$  has been reversed to a value  $U_1$  (slightly lower than  $U_3$ , due to losses, Figure 4) after the half wave injected current. This reversed voltage charges  $C_t$  through the loop  $C_s - V_{a4} - L_1 - C_t$  by firing  $V_{a4}$  to form the transient recovery voltage and reverse recovery voltage ( $t_3$  to  $t_5$ ).

$V_{a5}$  and  $V_{a3}$  are fired at  $t_4$  after the transient recovery voltage has been damped out to reverse the voltage on  $C_s$ . The voltage applied on  $C_t$  and  $V_t$  changes its polarity correspondingly from  $U_1$  to  $U_2$  ( $t_4$  to  $t_6$ ).

$V_{a2}$  is fired at  $t_7$  in order to allow current ( $I_{ch}$  in Figure 4) from the DC charger to compensate the voltage drop on  $C_s$ .  $V_{a2}$  is blocked by the reverse oscillating current after  $C_s$  is fully compensated at  $t_8$ .

$V_t$  is fired at  $t_9$  from the forward voltage  $U_3$ . The capacitor  $C_t$ , which was charged to the same voltage level, will then be discharged through  $V_t$  to produce the early inrush current as in service. The firing of  $V_t$  collapses the voltage between its terminals and results the current source voltage apply on the  $V_{a1}$ .

Following the firing of  $V_t$  the isolation valve  $V_{a1}$  is fired to release the output of the high current source through  $V_{a1}$  and the test object  $V_t$ .

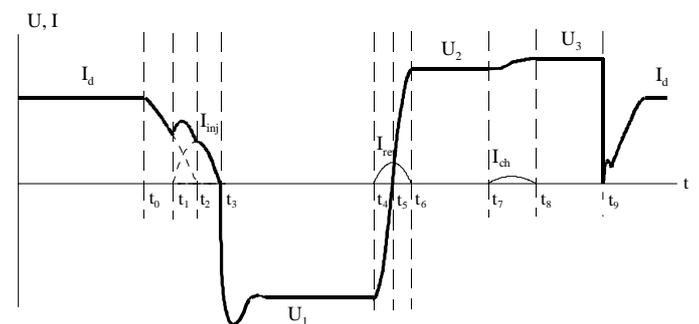


Fig. 4. Current and voltage relationship on the test object

### C. Control of Synthetic Test Circuit

The control and protection of the synthetic test circuit are governed by ABB's MACH 2 system. A number of firing timings of the test object and auxiliary valves are pre-defined in the firing sequences. The firing sequence and each individual timing are continuously adjustable during the tests if necessary. The width of the firing pulse is adjustable from 10  $\mu$ s to 20 ms. The firing timing has an accuracy of 10  $\mu$ s.

The programmed test sequences combine the current and voltage order with the firing sequences of the test object and the auxiliary valves, together with the test duration. The control system includes also the control/monitoring of the temperature and flow of the cooling media in each individual valve.

A graphical operator interface of MACH 2 provides an easy access to utilize above functions and to make the connection of main circuit permissible remotely.

## IV. VERIFYING TESTS

In order to verify the synthetic test circuit the following tests have been performed: Periodic firing and extinction tests, intermittent direct current, minimum a.c. voltage tests, transient forward voltage test during thyristor recovery period

and fault current test with re-applied forward voltage. The test object  $V_t$  consists of two complete thyristor modules (twelve thyristor levels) and two saturable reactors.

A general current and voltage waveshape under periodic firing and extinction tests is shown in Figure 5. With this basic waveshape, operational tests corresponding to different service conditions could be realized by adjusting the output voltage level of the DC source. To represent the operational mode of  $\alpha=90^\circ$  the test object has to be fired twice in one cycle as shown in Figure 6. One extra injection current will pass through the test object by this double firing. This extra injection current gives the test object extra conduction losses. These extra losses are negligible compared to the total losses.

The reverse and forward voltages are of the same value (under no losses assumption) in the test circuit. This gives a higher reverse voltage under maximum continuous firing voltage test or a higher forward voltage under maximum continuous recovery voltage test. When heat-run test is performed, attention has to be paid to the determination of voltage level of the voltage source. The voltage should be equal or higher than the value that could result in the same losses as in service.

With separated current and voltage sources in the synthetic test circuit, the efficiency of impulse generator is greatly increased. This technical merit gives the feasibility of applying the impulse transient voltage on the test object by a conventional impulse generator. The front time of impulse can be adjusted from 1  $\mu$ s to 700  $\mu$ s in the test circuit.

Figure 7 is the test record of transient forward voltage test during thyristor recovery period. Transient impulse voltage has a front time of 1  $\mu$ s in this test.

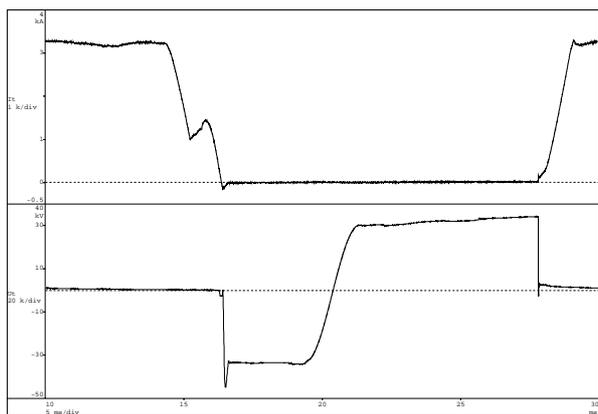


Fig. 5. Periodic firing and extinction tests

A test oscillogram of one-loop fault current with re-applied forward voltage test is given in Figure 8. No transit time is necessary from normal to short-circuit operation in the synthetic test circuit.

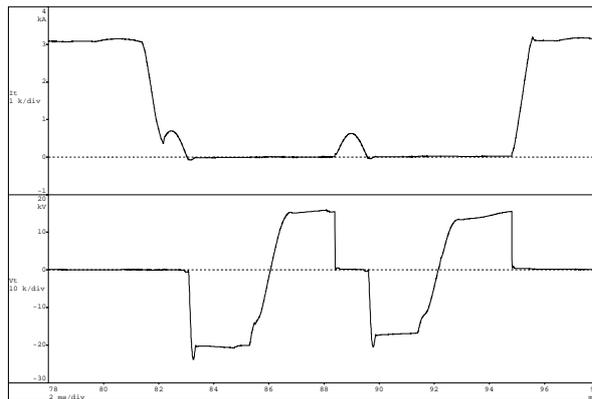


Fig. 6. Periodic firing and extinction test ( $\alpha = 90^\circ$ )

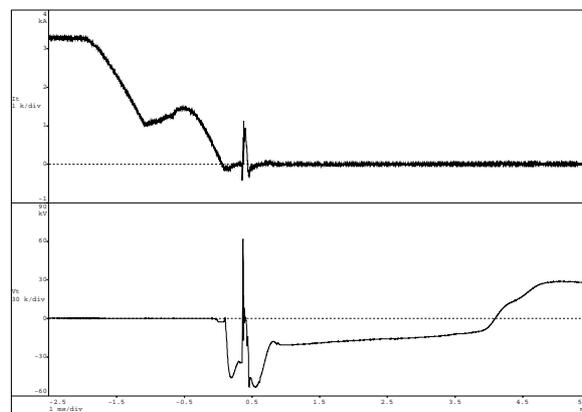


Fig. 7. Test with transient voltage during the recovery period

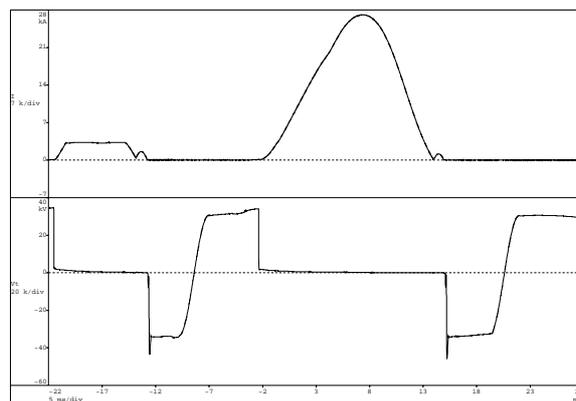


Fig. 8. One-loop fault current with re-applied forward voltage

The capabilities of the synthetic test circuit to perform other operational test duties have been verified in the verifying tests too. These test duties include multiple-loop fault current test without re-applied forward voltage, intermittent direct current and minimum AC voltage tests.

The tests show that the synthetic test circuit, in conjunction with direct test circuit, can cover all the test duties specified in the operational tests of HVDC thyristor valves by IEC and IEEE Standards [1] [2]. The test circuit correctly supplies the direct current in the current interval and applies the recovery voltage in the voltage interval on the test object.

## V. CONCLUSIONS

Synthetic testing method is an economical and efficient way to verify modern HVDC thyristor valves. The possibility of test circuit parameter adjustment of the synthetic circuit gives more flexibility to perform different HVDC valve tests. Independent control of test current and voltage by two different sources provides close and flexible stress reproduction. By proper design the synthetic test circuit can correctly reproduce the current and voltage stresses on the thyristor valve.

As a result of the theoretical and laboratory investigations, a new synthetic test circuit for the operational tests of HVDC thyristor valves is introduced. This circuit shows its superiority by:

- test current from a six-pulse bridge
- correct stress reproduction, especially at two critical instants (turn-on and turn-off), of valve operation
- no transit time from normal to short-circuit operation
- large number of series connected thyristor levels under test
- simplicity in circuit configuration

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